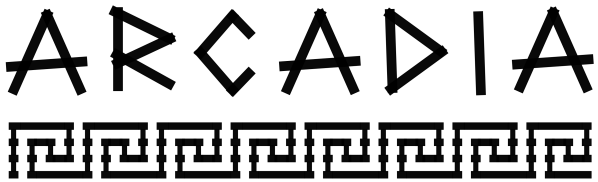
ARCADIA

… and Future Vertex Detector R&D

RD_FCC collaboration meeting
December 15th - 16th, 2021

Istituto Nazionale di Fisica Nucleare



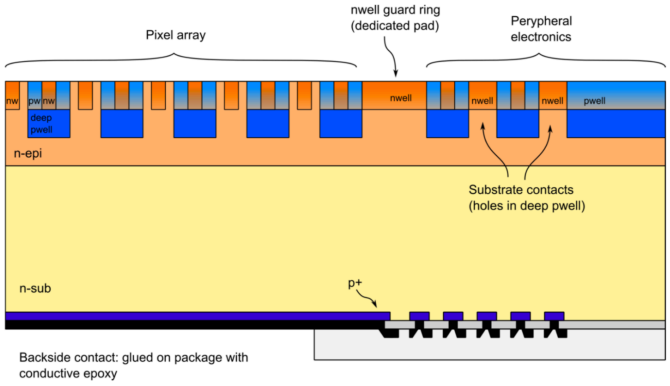
Manuel Rolo (INFN),
on behalf of the ARCADIA Collaboration

ARCADIA (INFN CSNV Call Project)

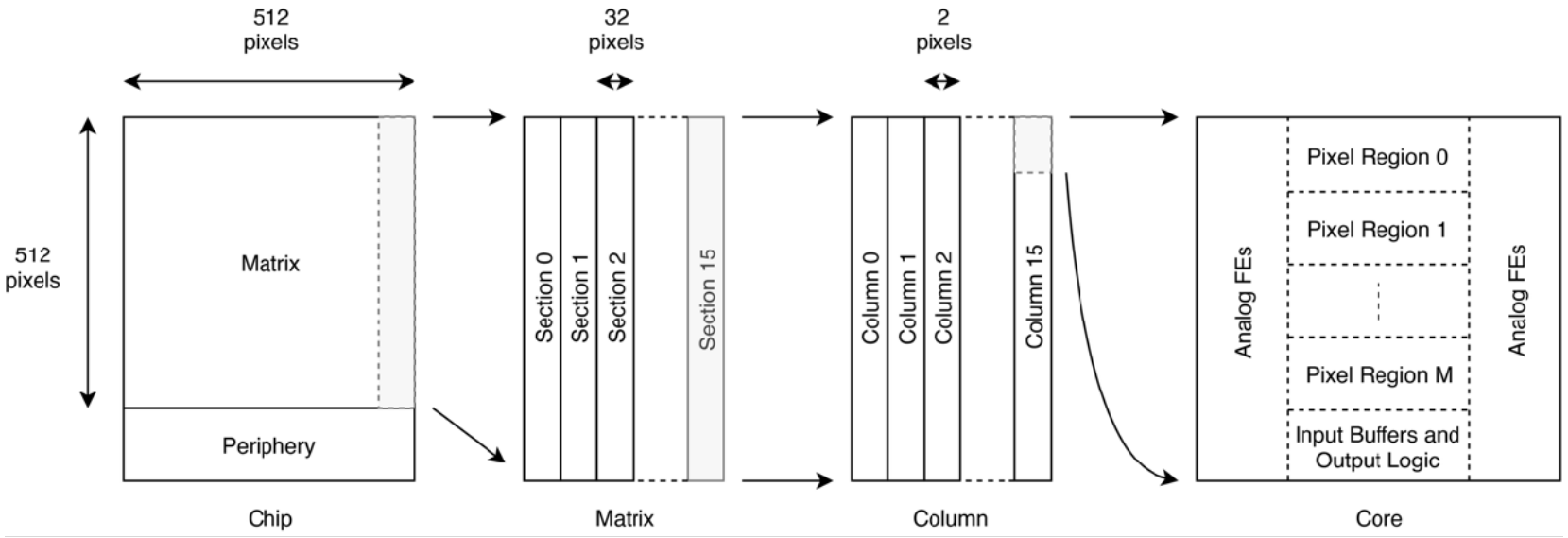
Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Creation of a novel platform for the implementation of innovative monolithic sensors compatible with standard CMOS fabrication processes

- Challenge: deployment of large-area system-grade CMOS sensors implementing scalable readout architectures with ultra-low power capability (O(10 mW/cm2))
- Technology: LFoundry 110nm CMOS node, quad-well, high-resistivity bulk
- Active sensor thickness in the range 50 µm to 500 µm
- Operation in full depletion with fast charge collection only by drift
- Small charge collecting electrode for optimal signal-to-noise ratio

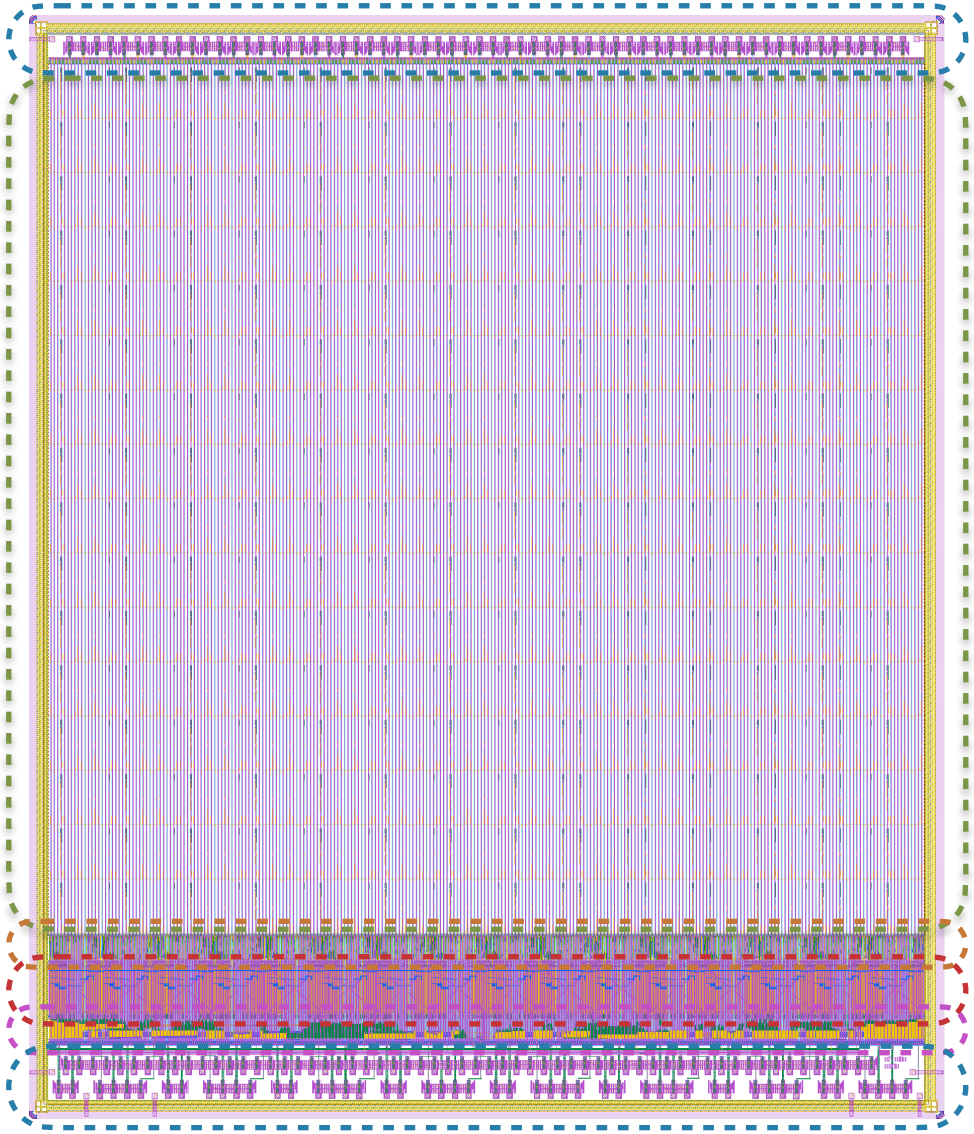


ARCADIA-MD1: Main Demonstrator Chip



- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm^2 silicon active area, "side-abuttable"
- Triggerless binary data readout, event rate up to 100 MHz/cm^2
- **First Engineering Run** (SPW incl. *MD1*) tapeout 11/2020, **silicon being tested**
- **2nd full CMOS maskset** mid-2021 (incl. *MD2*) currently on last metal BEOL, fab out expected January 2022
- **3rd SPW mid-2022** with design fixes (incl. *MD3*), explorative sensor and CMOS designs, new architectures with higher data throughput, test chips for fast timing (R&D on sensors and electronics already started with 2nd SPW)

ARCADIA-MD1: Chip Floorplan



Top Padframe

Auxiliary supply, IR Drop Measure

Matrix

512x512 pixels, Double Column arrangement

End of Sector (x16)

Reads and Configures 512x32 pixels

Sector Biasing (x16)

Generates I/V biases for 512x32 pixels

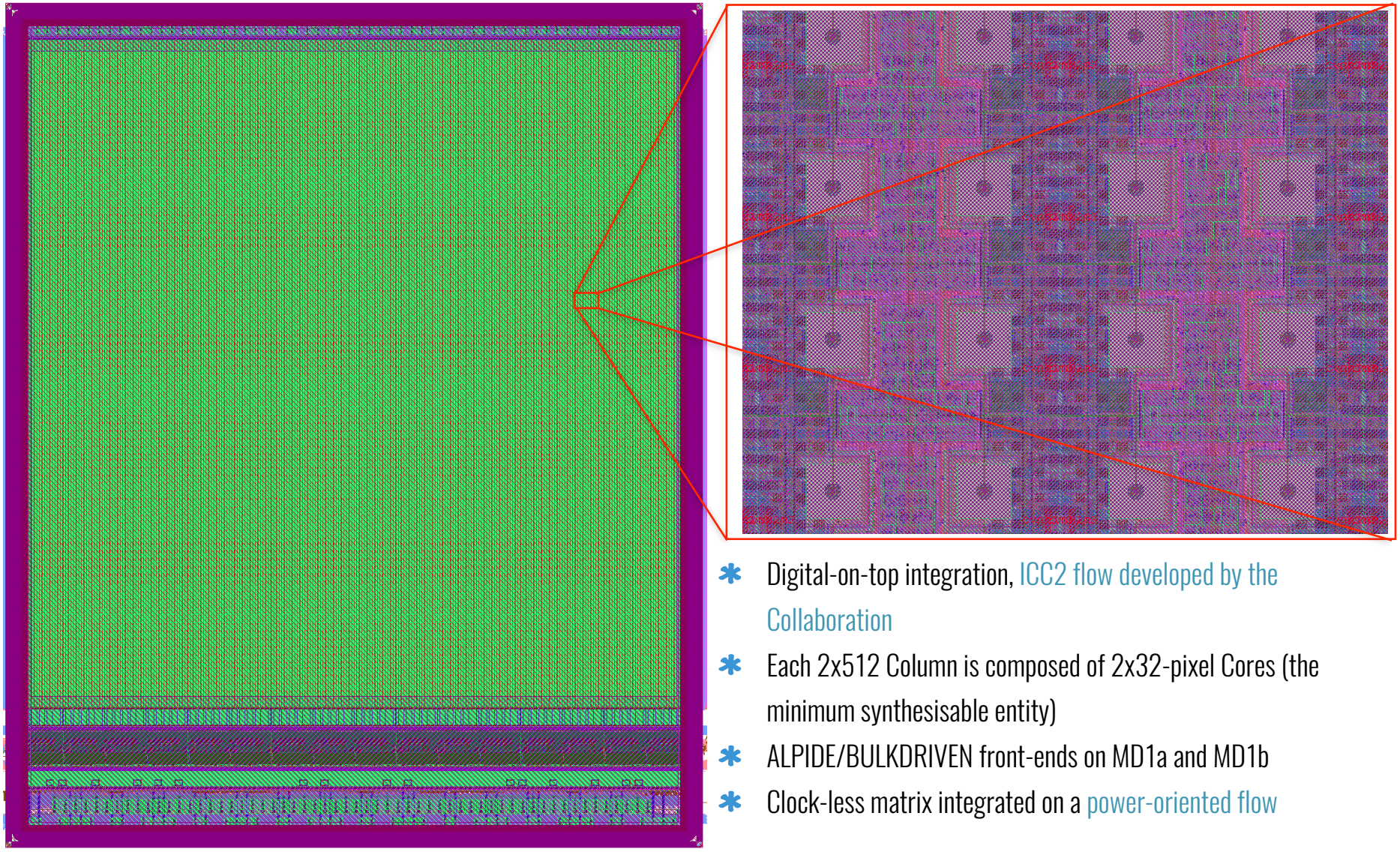
Periphery

SPI, Configuration, 8b10b enc, Serializers

Bottom Padframe

Stacked Power and Signal pads

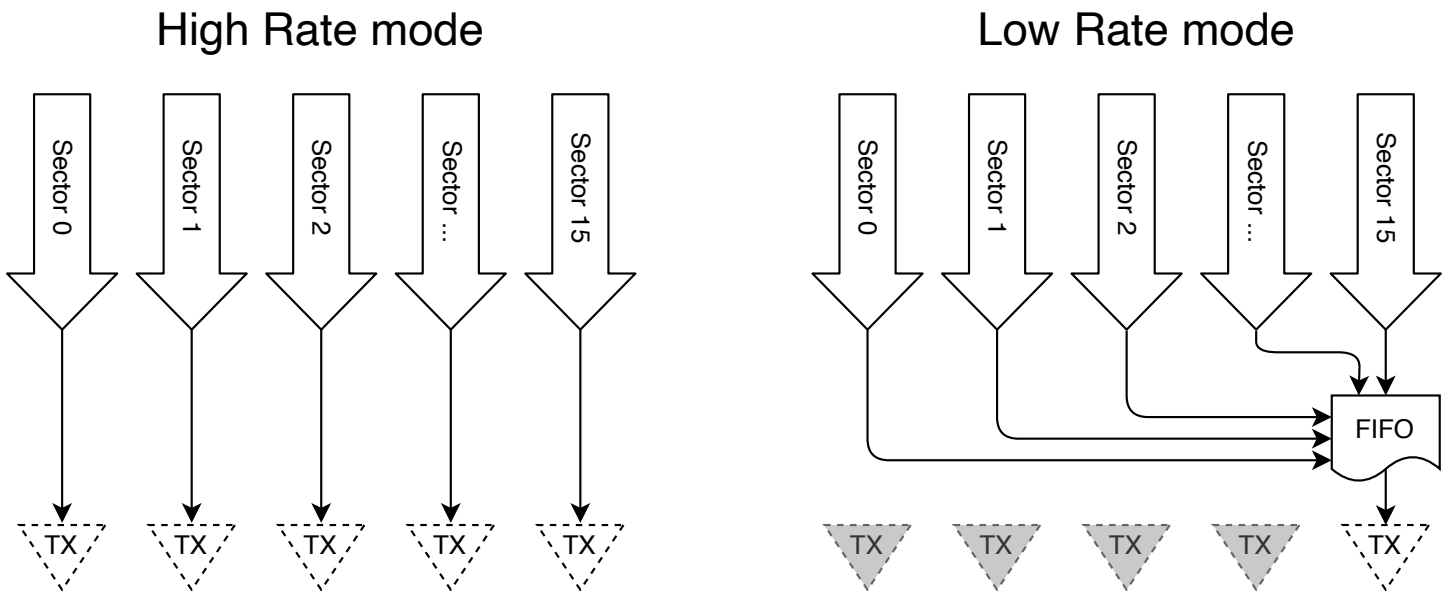
ARCADIA-MD1: Integration



- Digital-on-top integration, ICC2 flow developed by the Collaboration
- Each 2x512 Column is composed of 2x32-pixel Cores (the minimum synthesisable entity)
- ALPIDE/BULKDRIVEN front-ends on MD1a and MD1b
- Clock-less matrix integrated on a power-oriented flow

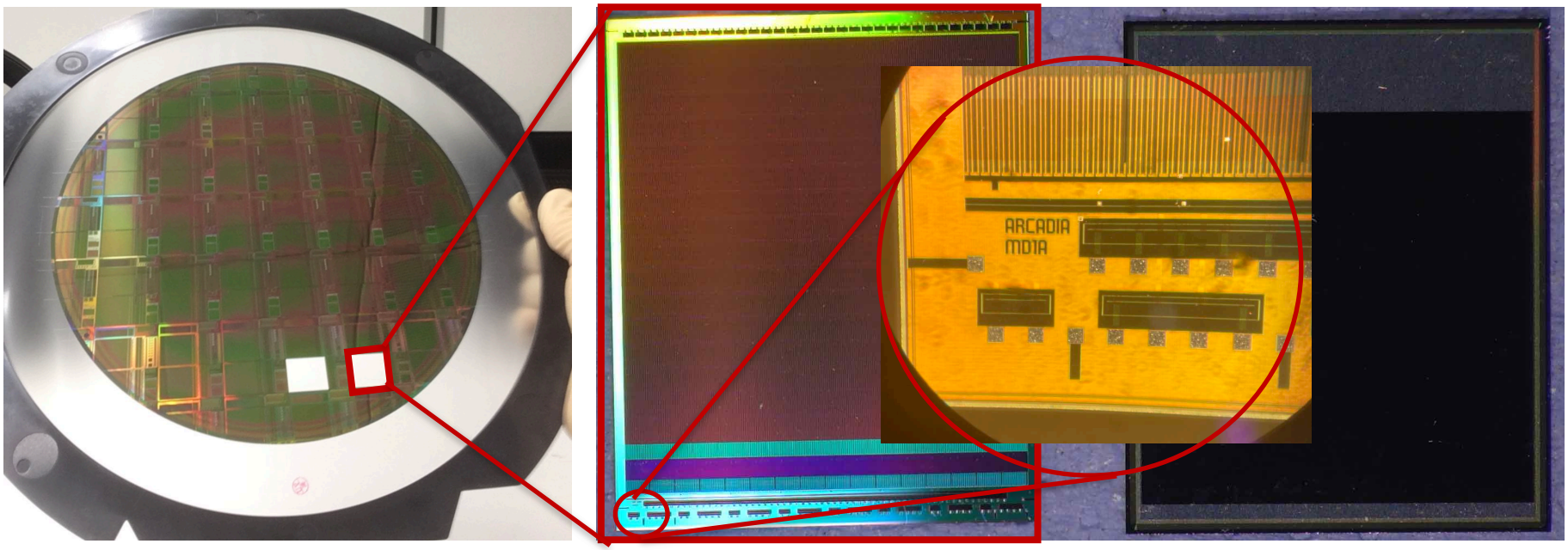
ARCADIA-MD1: Peripheral Dataflow

- Each Column (32x512 pixels) has a dedicated readout link in High Rate Mode
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.

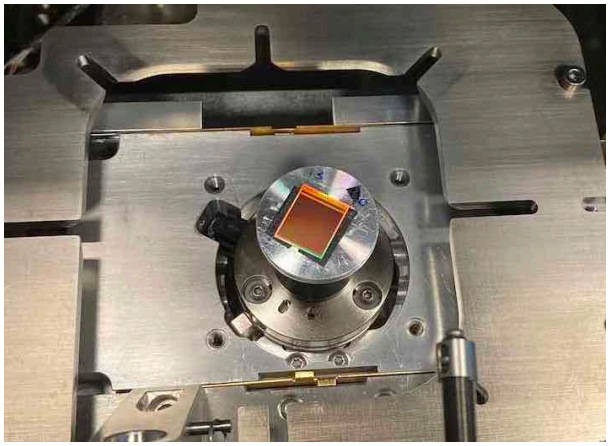


* "A 2 Gbps custom LVDS transceiver for the ARCADIA project", talk at IEEE NSS-MIC 2021

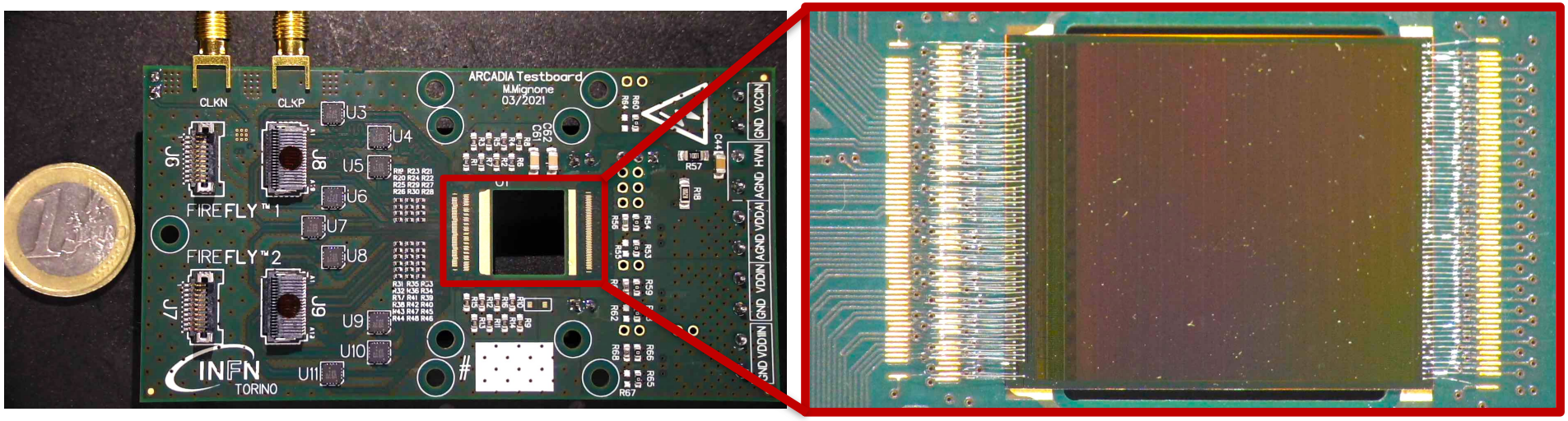
ARCADIA-MD1: silicon from 1st run

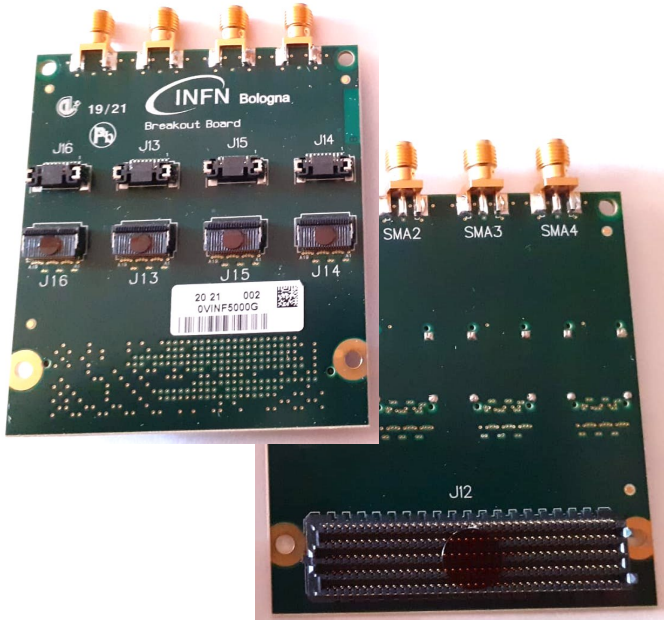


- First samples of **ARCADIA-MD1 powered-on** this summer
- Later-than-tapeout simulations identified bug on pad frame connections, simple to solve with FIB
- First data looks good & sensor depletion OK



Front-end FEB-MD1 and breakout boards



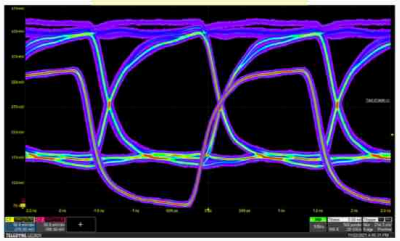


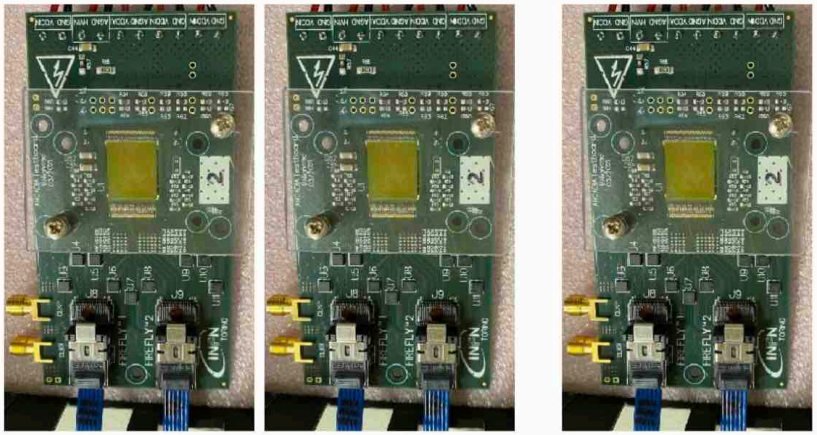
- 2 Samtec FireFly connectors for ASIC signals (Clock, SPI, Data)
- Connection to external low jitter Clock (via SMA connectors)
- High voltage to the DMAPS backside or (wirebonded) to pads on top
- Independent LDOs for IO Buffers, Analog Core, Digital Core
- PCB through-hole for matrix BSI
- custom FMC-to-Firefly breakout board

G. Balbi [INFN-BO]
M. Mignone [INFN-TO]

DAQ Hardware for the MD1 E-Kit

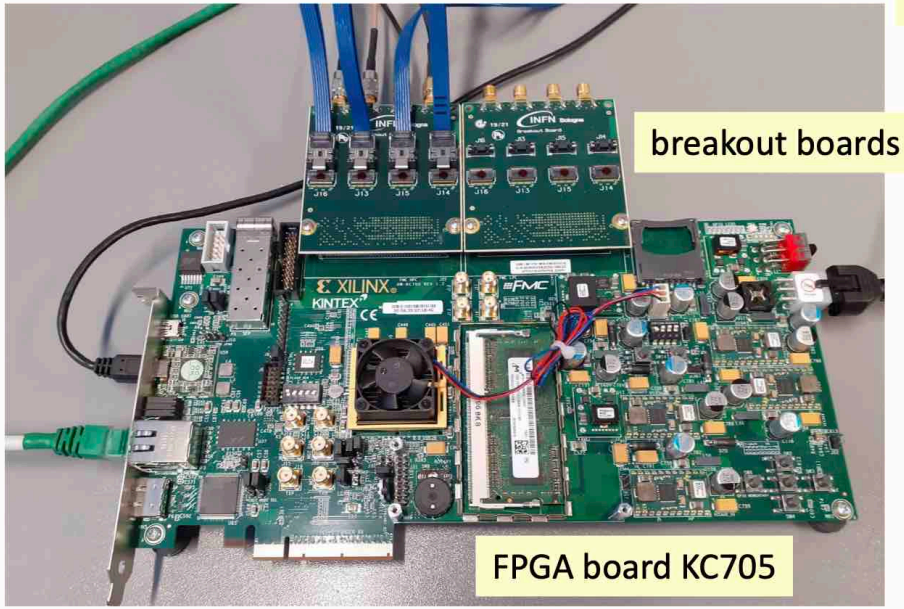
oscilloscope





FEB cards

Samtec Firefly cables
(20 cm – 50 cm – 100 cm - 200 cm)



breakout boards

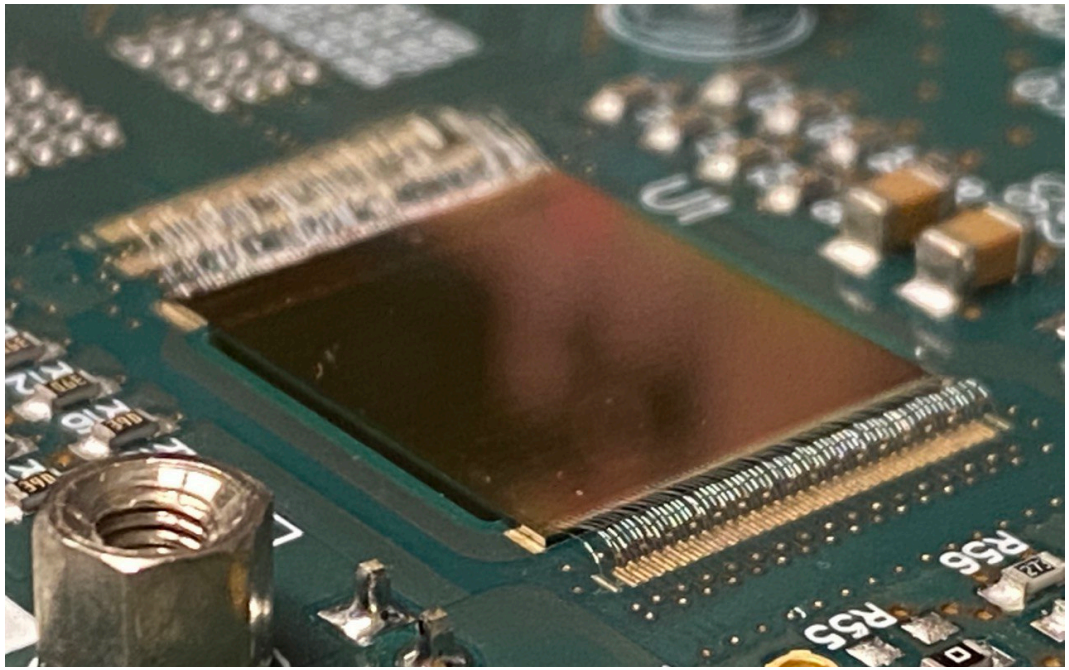
FPGA board KC705

1 Gb ETH

D. Falchieri [INFN-BO]

MD1: check-list from electrical tests

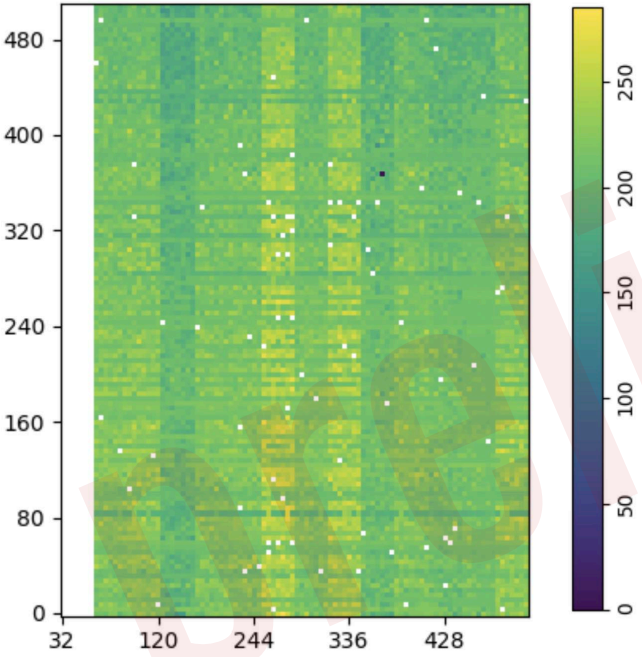
- ☑ Chip configuration write/readback
- ☑ Space Mode enable/disable
- ☑ Clock Gating and Clock Dividers
- ☑ Digital Injection
- ☑ LVDS SER1-15 enable/disable
- ☑ Test Pulse connectivity
- ☑ Analog FE bias and threshold scan
- ☑ Soft (SPI-enabled) and Hard (through Ext pin) Resets



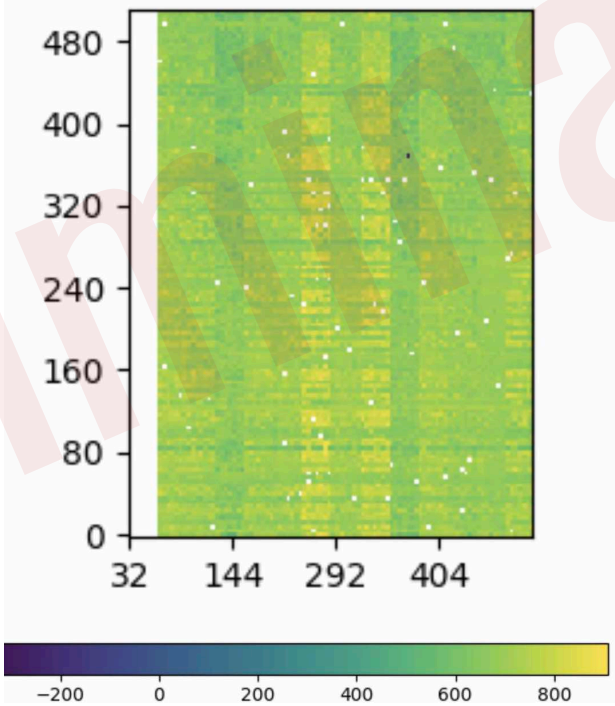
- **tests with analogue front-end ongoing:**
  - test pulse charge injection with FE, s-curves, FE baseline map, noise measurements, depletion studies
  - next: characterisation with radioactive sources and laser

MD1: first very preliminary data

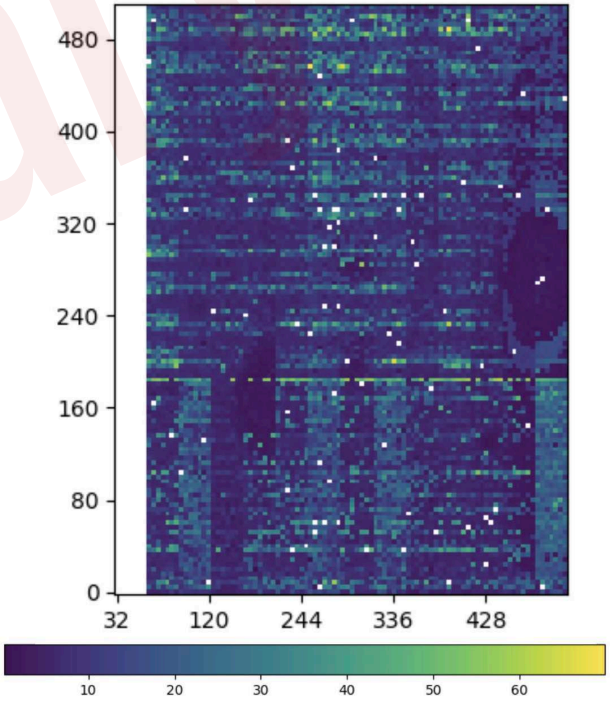
FEB3 Baseline (mV)



FEB3 Gain (mV/fC)

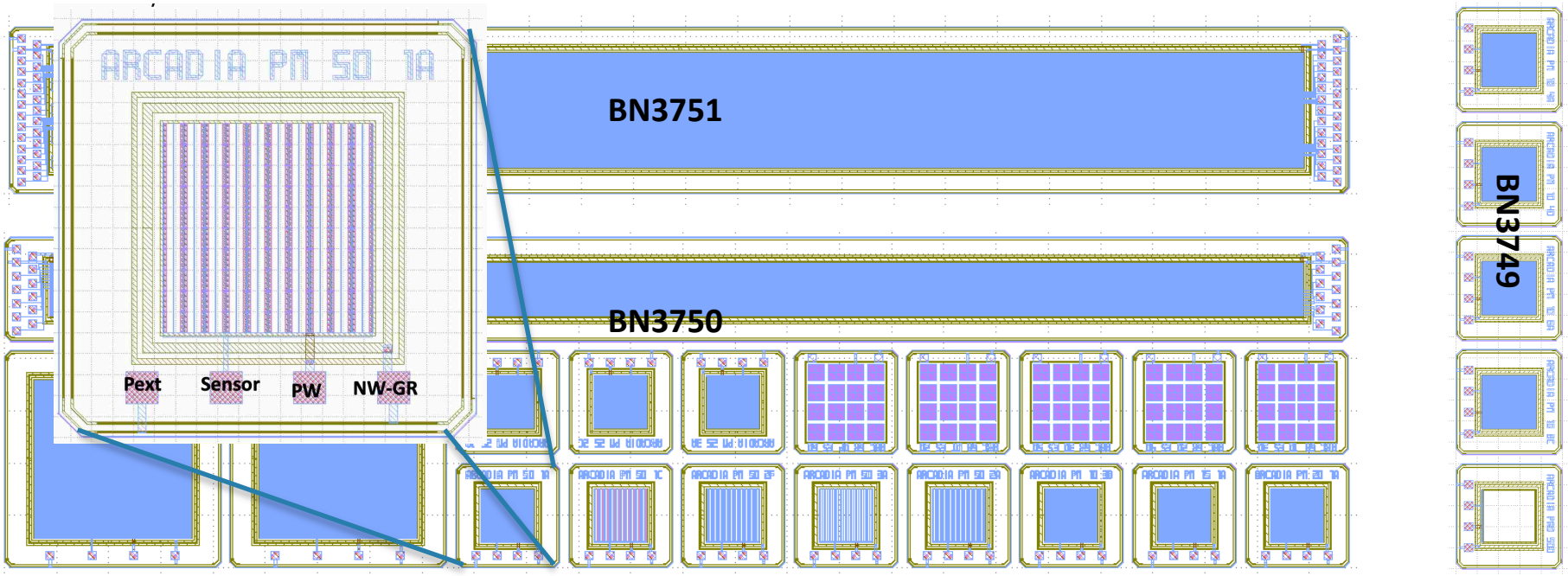


FEB3 Noise (mV)



S. Garbolino, A. Paternò [INFN-TO]

Pixel/Strip Test Structures



- strips come in different flavours:
  - 25 μm pitch pixelated + 25 μm continuous (10+10) [2 variants]
  - 10 μm pixelated (4 groups of 12 strips connected to pads) [4 variants]

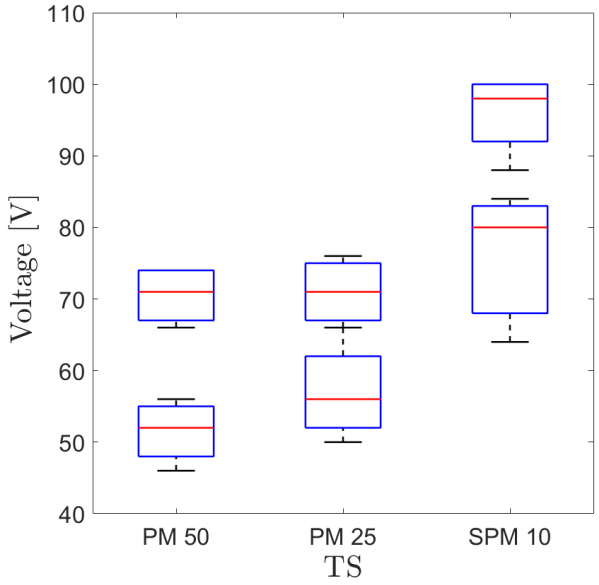
- and pixels as well:
  - Pseudo-Matrices of 1x1 and 2x2 mm^2
  - 50 μm (5 variants)
  - 25 μm (3 variants)
  - 10 μm (6 variants)

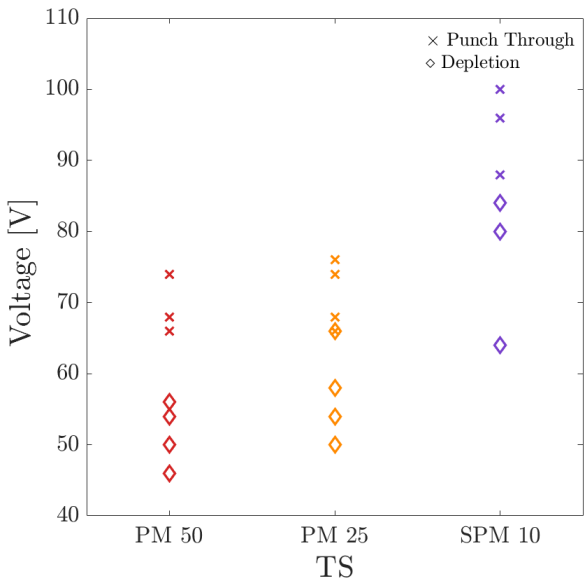
L. Pancheri [TIFPA]

Depletion Studies

Group	thickness	Vdepl	Vpt
GROUP 1: wafer #06 and #07 (BSI 8µm n- epi 1E14 / N-	200µm	87 – 102	105 – 111
GROUP 2: wafer #02 and #03 (FSI 8µm n- epi 1E14 / N-	100µm no litho	20 – 30	36 – 39
GROUP 3: wafer #15 and #16* (BSI 7µm n- epi 1E14 /N-	200µm	50 – 66	66 – 76
GROUP 4: wafer #10 and #12 (FSI 7µm n- epi 1E14 /N-	100µm no litho	9 – 18	20 – 25
GROUP 5: wafer #20 and #24 (FSI 8µm n-epi 1 40 µm / P+	300µm	21 – 23	24 – 26
GROUP 6: wafer #22 and #23 (FSI 8µm n-epi 1 40 µm / P+	100µm	20 – 30	24 – 33

note: V_{depl} and V_{PT} ranges are reported in absolute value





T. Corradino [TIFPA]

Status of silicon testing - 1st SPW

* Measurements on bonded test structures (first non-irradiated and then irradiated with x-rays and neutrons), front-side and back side

now

- **IV curves with temperature, extraction of depletion, punch-through voltages, dark current and capacitance, first laser tests**

11/21

- Charge collection with focused pulsed laser (back-side). On pixels: only signal evolution with time and position of the laser spot. On strips: charge sharing is also possible.
- Lab. sources. (top-side and back-side)

* Characterisation of the ARCADIA-MD1

now

- **functional and electrical characterisation (basic functionalities with on-chip test pulse and hit injection, s-curves, threshold calibration, rate assessment)**

12/21

- laser scans with red and IR light (CCE vs bias voltage, uniformity, clustering and resolution)
- tests with x-ray and radioactive sources (55Fe, 241Am, 90Sr)
- cosmic ray stand (sync and event building, efficiency, resolution) and beam tests with MD1 telescopes

mid-22

M. Caccia [INFN-MI]

Multi-plane MD1 Telescope Configuration

D. Falchieri [INFN-BO]

scintillator trigger

3 KC705 boards can be put in parallel to readout up to 9 Arcadia-MD1 chips for test-beam applications

master

global trigger

fanout board

ETH1-2-3

global trigger

ETH1

KC705

global trigger

ETH2

KC705

global trigger

ETH3

KC705

scintillator trigger

breakout board

ARCADIA-MD1 FEB

ARCADIA-MD2

A second main demonstrator (codename ARCADIA-MD2) has been submitted in Summer 2021, featuring design and architecture improvements targeting power reduction, scalability.

- 16x2 pixel Cores, 8 Cores in the Matrix
- Logic and buffering optimization -> Acknowledge signal propagates 7 times faster!
  - Simulations validated matrices up to 8192 pixels high
- Power optimization in the periphery
- 1 GHz DDR serializer -> 2Gbps bandwidth!
- Now in foundry, expected dies in January 2022.

CMOS Embedded Si-strip and readout

- Design and Production of continuous and “pixelised” strips, range 10 - 100µm pitch
- Proof-of-concept: **CMOS monolithic strip block and readout electronics**

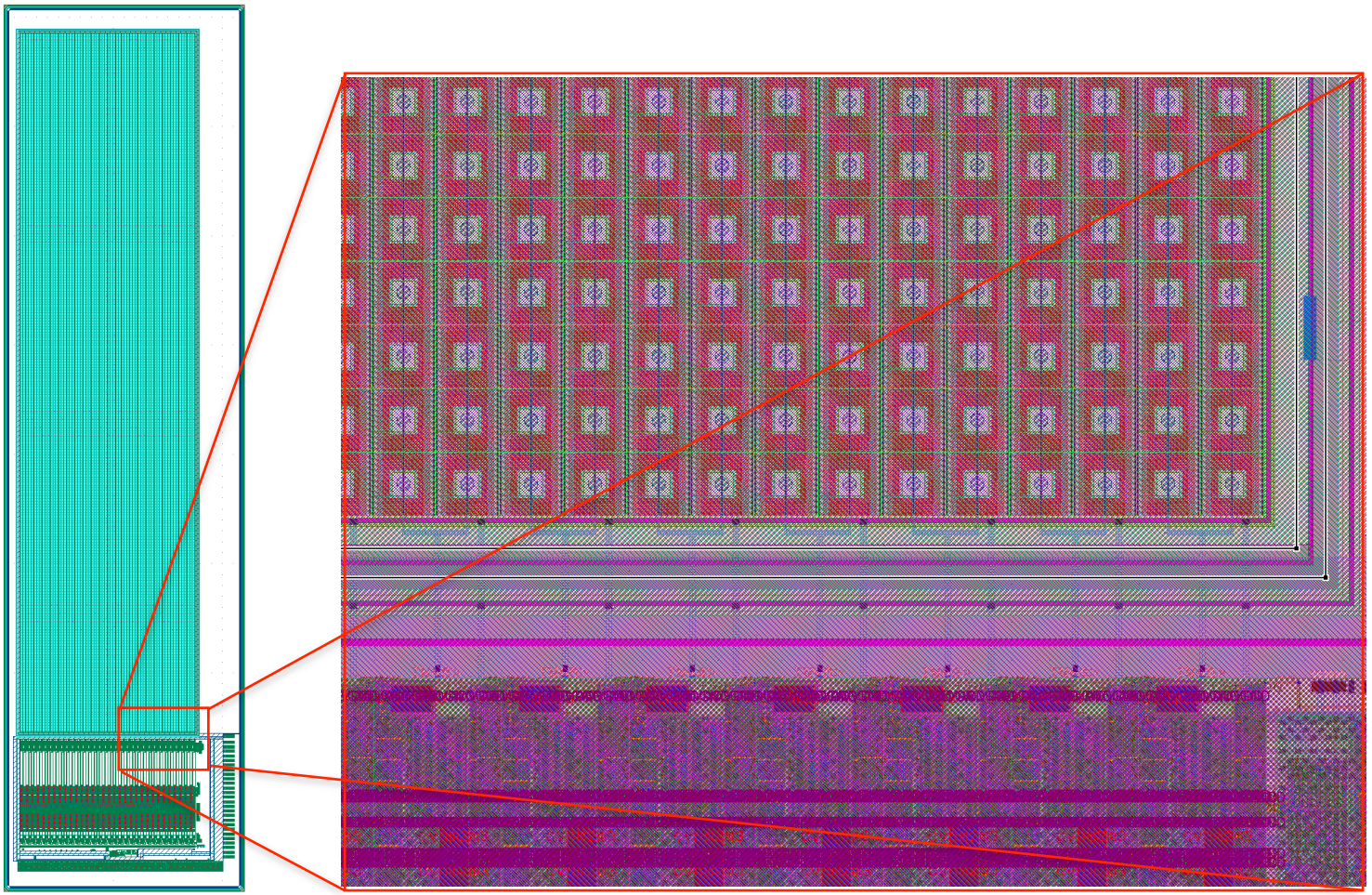


Figure: CAD Layout of 2x32x50µm pixelised strips

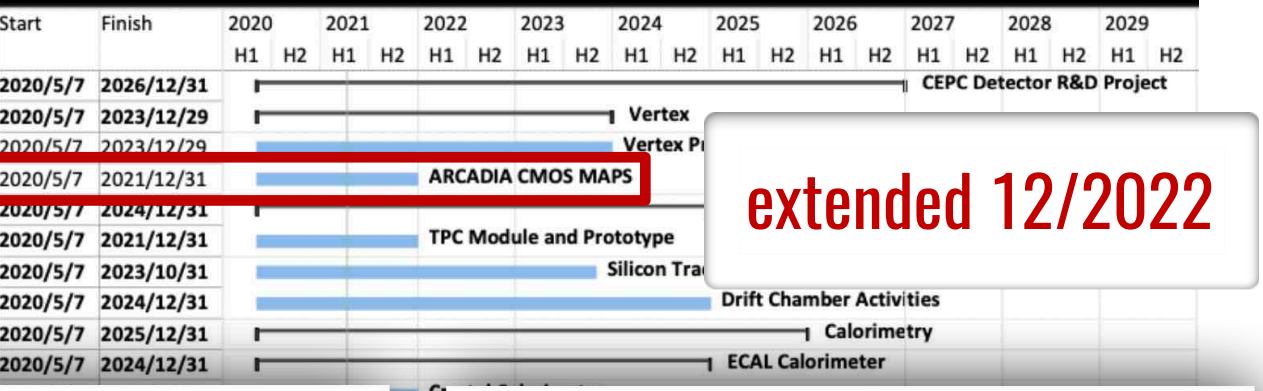
Figure: (top) detail of 2x32x50µm pixelised strips and (bottom) 32-channel custom readout

ARCADIA CMOS DMAPS at CEPC

https://indico.ihep.ac.cn/event/15229/session/6/contribution/3/material/slides/3.pdf

Projects overview: R&D schedule

PBS	Task Name	Start	Finish
	CEPC Detector R&D Project	2020/5/7	2026/12/31
1	Vertex	2020/5/7	2023/12/29
1.1	Vertex Prototype	2020/5/7	2023/12/29
1.2	ARCADIA CMOS MAPS	2020/5/7	2021/12/31
2	Tracker	2020/5/7	2024/12/31
2.1	TPC Module and Prototype	2020/5/7	2021/12/31
2.2	Silicon Tracker Prototype	2020/5/7	2023/10/31
2.3	Drift Chamber Activities	2020/5/7	2024/12/31
3	Calorimetry	2020/5/7	2025/12/31
3.1	ECAL Calorimeter	2020/5/7	2024/12/31



extended 12/2022

CEPC detector R&D Project for preliminary evaluation by the CEPC International Detector R&D Committee

https://indico.ihep.ac.cn/event/15229/session/6/contribution/3/material/slides/4.pdf

1.2 ARCADIA CMOS MAPS

Document Responsible:	Manuel Rolo
Last saved by on	11/01/2021 5:00:00 PM
Revision number:	2

"**The main goal of the project**, started in 2019 with a timescale of 3 years, is the design, production and commissioning of an array of 512x512 pixels with a pitch of 25 x 25 µm2 (total matrix area 1.28x1.28 cm2), embedded electronics performing sparsified readout and power consumption at the level of 20 mW/cm^2. This test vehicle is expected the be a **viable prototype for** applications at the **next generation lepton colliders**."

ARCADIA at AIDAinnova
WP5 - Depleted Monolithic Active Pixel Sensors

Development of next generation monolithic CMOS devices.

- Develop a demonstrator system that can be used in future experiments and upgrades
- Improvements in many directions: timing, thickness, speed, power, area, bendability,..
- Arcadia++ more focused on future colliders: ALICE LS3, Higgs factories (FCC, CEPC)
- Project started April 2021, 4 Years.

Expression of Interest for participating in the H2020 Innovation Pilot

on detector technologies at accelerators

Title: **ARCADIA++** : Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Participants (max. 6): *list the participating institutes, laboratories and industrial partners*

Name of the legal entity	Type (university, institute, laboratory, company)	Country
INFN – BO, MI, PD, PV, PG, TIFPA, TO	Institute	Italy
Univ. Oxford	University	England
PSI	Institute	Switzerland
ETH	Institute	Switzerland
Univ. Zurich	University	Switzerland
IHEP	Institute	China

Contacts: *One name + e-mail per participant*

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Depleted MAPS for Future Colliders

	RHIC STAR	LHC - ALICE ITS	CLIC	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp
NIEL [n_{eq}/cm^2]	10^{12}	10^{13}	$<10^{12}$	10^{15}	10^{16}	10^{15}-10^{17}
TID	0.2Mrad	<3Mrad	<1Mrad	80 Mrad	2x500Mrad	>1Grad
Hit rate [MHz/cm^2]	0.4	10	<0.3	100-200	2000	200-20000

Heinz Pernegger, Vertex 2018

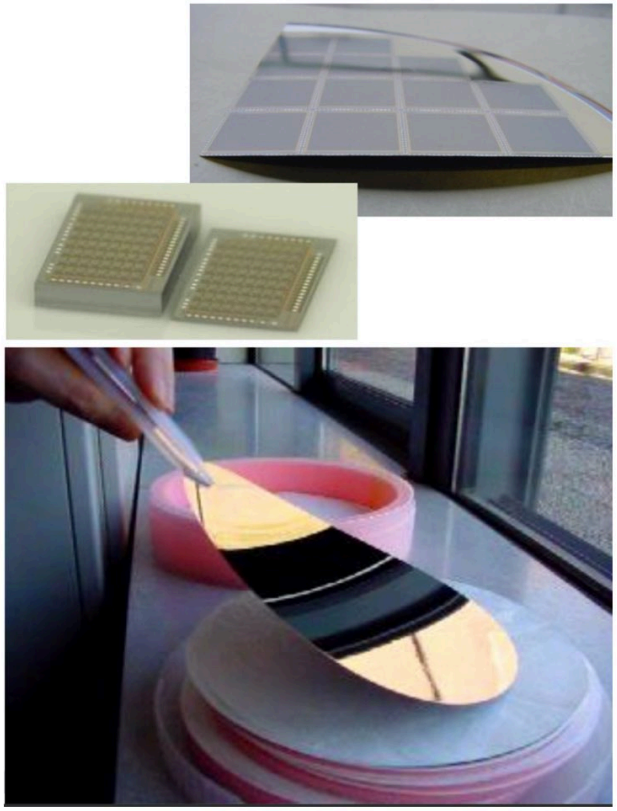
- Hit rate and radiation hardness for Frontier Detectors could require improvements of ~2 orders of magnitude in respect to the state-of-the-art technology

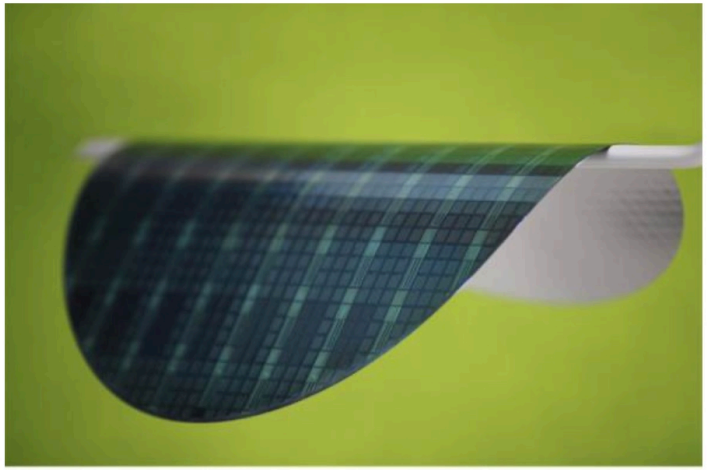
* Charge collection by drift: faster signals, better radiation hardness
* New architectures for higher event rate capability
* Advanced integration and interconnect technology for large sensor area and lightweight modules

Future R&D: Thinner Silicon

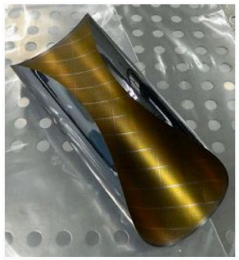
- Technology:
  - Course + fine grinding
  - Critical: thinning damage, impact on devices
- Wafer handling:
  - Very thin wafers (< 100 um): use of carrier wafers and temporary wafer (de-)bonding technology
- IMEC results:
  - Thinning down to 15 um
  - Total thickness variation ~ 2 um on 200 mm wafer

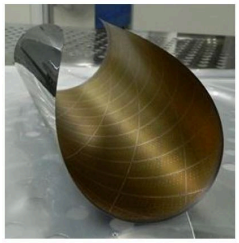
P. De Moor (IMEC)

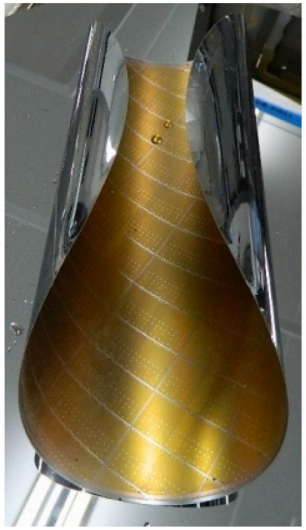




50 µm thin 300 mm Silicon Interposer Wafer with Cu-RDL metallisation. Source: Fraunhofer IZM







* Wafer-scale ultra-thin (< 20 µm) stitched MAPS could bend into a cylindrical mechanically stable self-supporting shape:

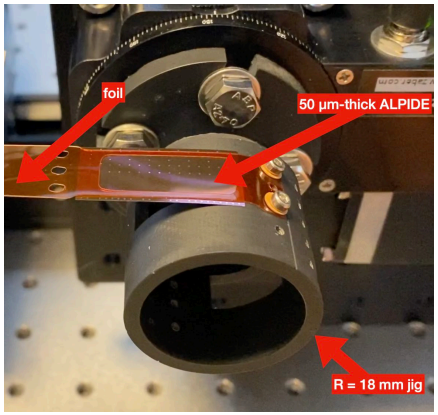
  ☑ purely Si based collider detector for tracking and PID with a VERTEX with an unprecedented low material budget of < 0.05 % X_0 per layer

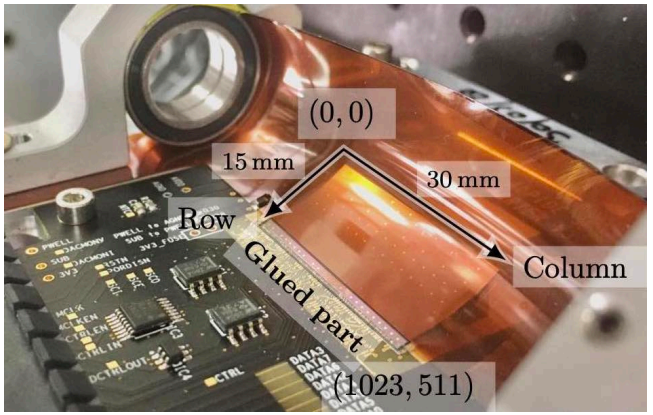
Wafer Thinning, applied to MAPS

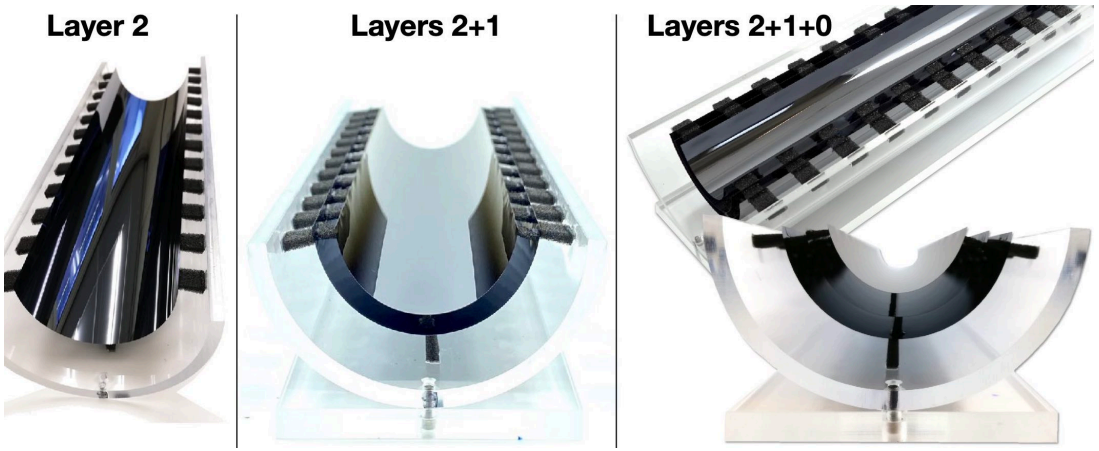
or… µITS3, i.e. 6 ALPIDEs at ITS3 radii

ALICE ITS3 working group demonstrated the bending, operation and performance of thinned MAPS, using 1.5 cm × 3 cm ALPIDE chips, and system studies towards the integration of wafer-scale sensors

- bent to radii of about 2cm without any signs of mechanical or electrical damage
- characterisation using a 5.4 GeV electron beam, detection efficiencies above 99.9 % at typical operating conditions
- 3-layer integration successful using 50 µm dummy Silicon



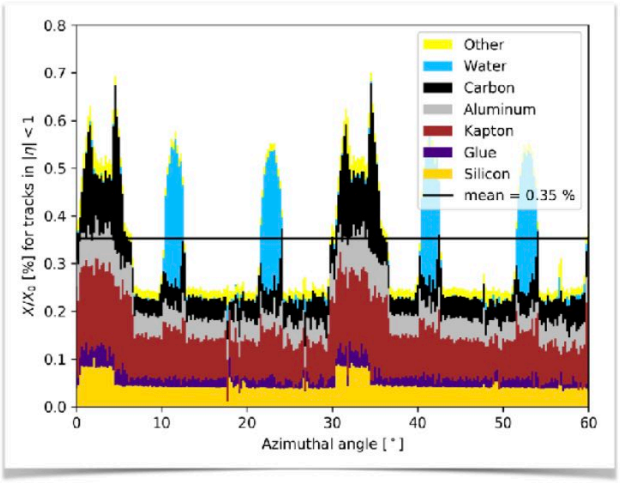


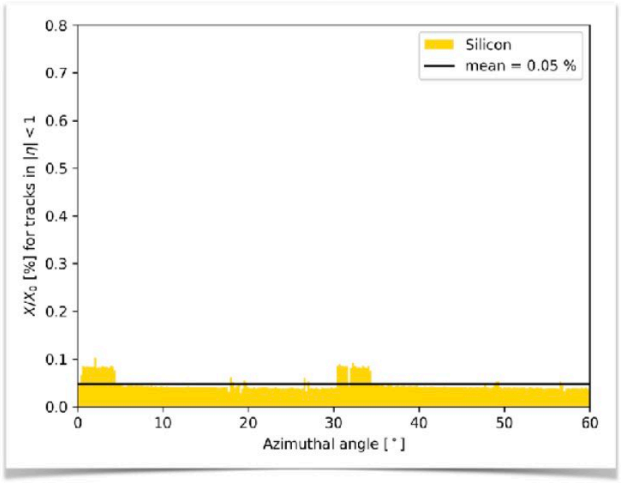


arxiv:2105.13000 "First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors"

Magnus Mager CEPC2021

Trending up: going "green"



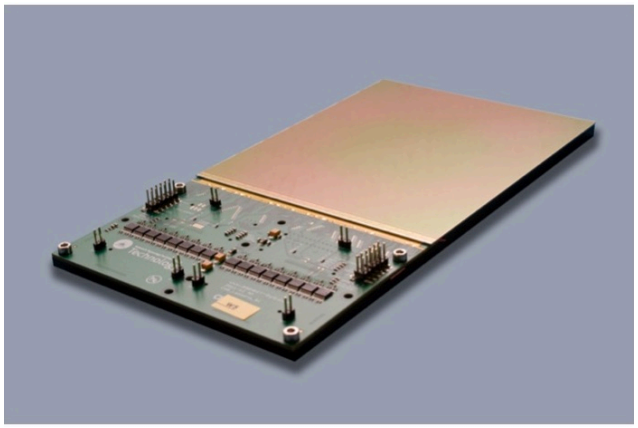


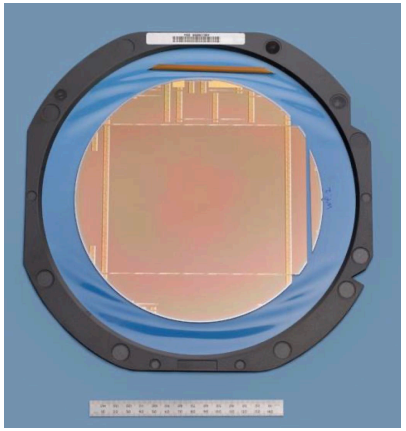
courtesy slide from Magnus Mager

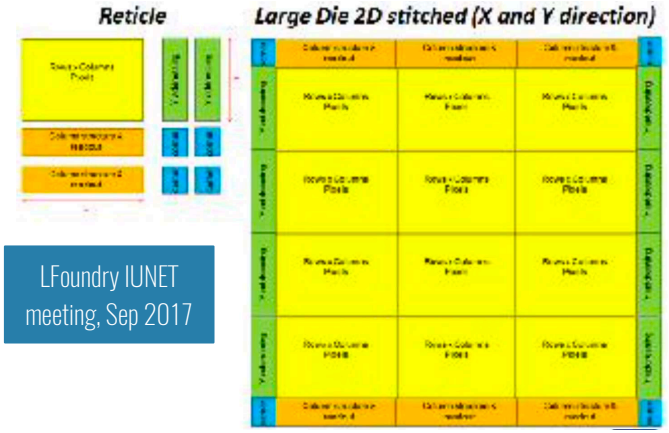
- Observations:
  - Si makes only **1/7th** of total material
  - **irregularities** due to support/cooling
- Removal of water cooling
  - **possible** if power consumption stays below 20 mW/cm²
- Removal of the circuit board (power+data)
  - **possible** if integrated on chip
- Removal of mechanical support
  - **benefit** from increased stiffness by rolling Si wafers

* **Power needs to be lowered to O(20mW/cm²)**

Trending up: Bigger, Stitched Silicon





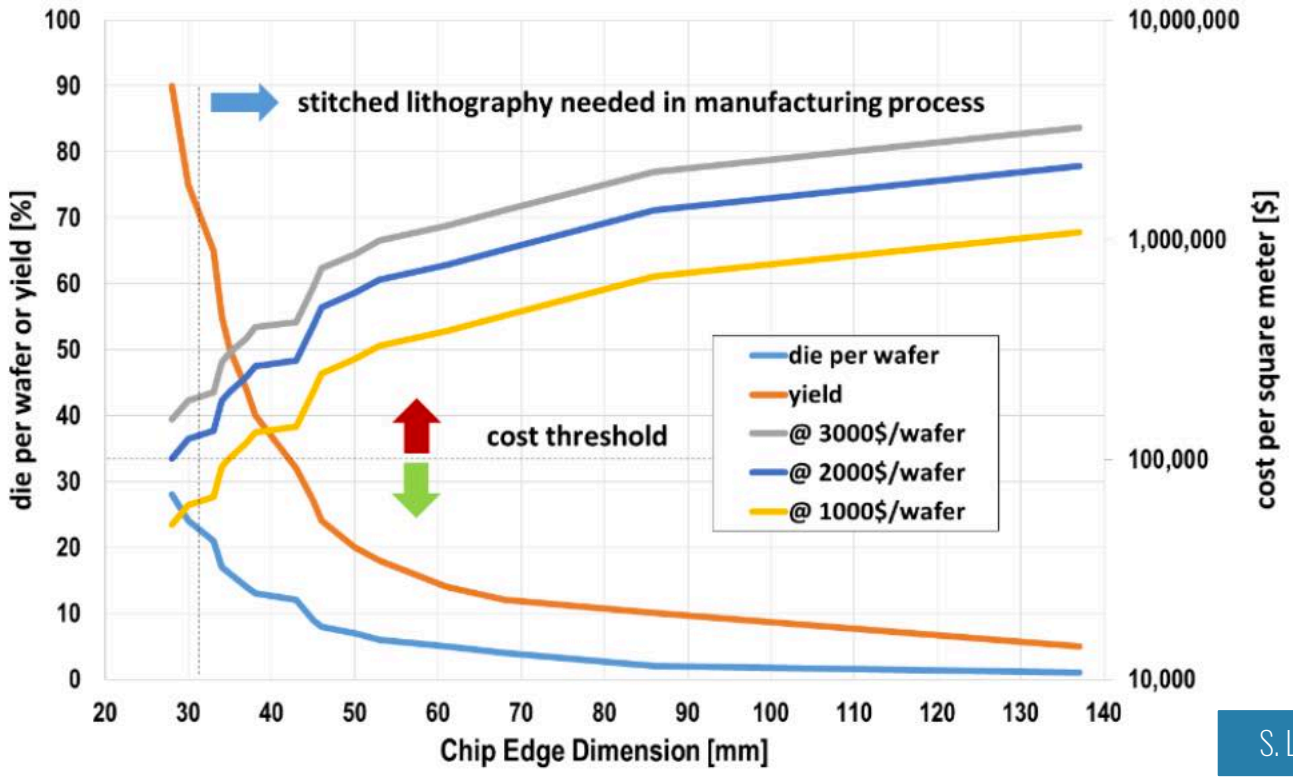


LFoundry IUNET meeting, Sep 2017

- (left) **Example of a wafer-scale imaging sensor chip for X-Ray applications developed at RAL (UK)**
- **139 x 120 mm CIS, Towerjazz 180nm on 200 mm (8") wafers, 1 sensor per wafer**

- *2D Stitching paves the way for all-silicon CMOS monolithic APS as active interposers: substrate handles signal, power and data interconnects, enabling the development of ultra-low material budget trackers;*
- *particularly interesting assuming 12" wafers, very low power (no water cooling) and no mechanical support for an only-silicon inner tracker in future HEP colliders. Different considerations may apply for an outer Si-tracker…*

Cost and Yield considerations (my favourite slide on)



S. Lauxtermann, PIXEL2018

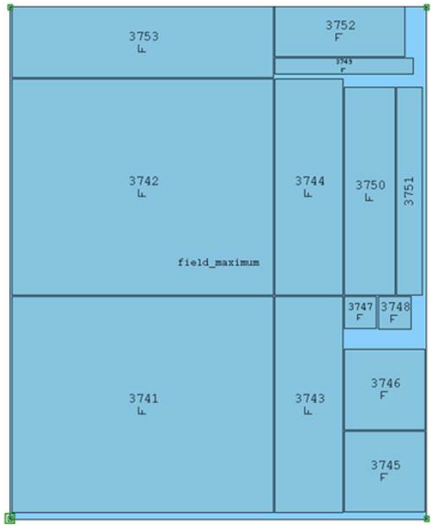
Cost of $100,000/m² tracking area is achievable with the following assumptions

- **> 75% Yield**
- **No stitching**
- **Wafer cost <$2,000 (only achievable using high volume CMOS manufacturing)**

Summary

- ARCADIA secured a total budget of 1.4 M€ and is extended to end 2022 with several groups working on:
  - Sensor R&D and Technology
  - CMOS IP Design and Chip Integration
  - Data Acquisition for electrical characterisation and beam tests with multi-chip telescopes
  - Radiation Hardness qualification
  - System-level characterisation for Medical (pCT), Future Leptonic Colliders and Space Instruments

- **ARCADIA Status and Schedule for 2022**
  - ARCADIA-MD1 submitted in October 2020, first dies in June 2021
  - 1st SPW run included 800 mm2 of innovative DMAPS, sensor and CMOS technology (tests on sensors are ok, tests on all digital and analog features confirmed the expected functionality)
  - 2nd run mid-2021: in foundry, 3rd run scheduled for mid-2022;



… and Outlook

- CMOS Depleted monolithic pixel (and strip) sensors are now a strong candidate both for future low material budget silicon trackers and for timing layers, with investment and R&D mostly focusing on:
  - very low-power architectures O (20 mW/cm^2)
  - process engineering for better time resolution O (100 ps) or better
  - larger and thinner chips towards all/only-silicon inner trackers
- We need to foster access to advanced technologies and foundries, and make a good use of the most advanced integration and industry standard wafer stacking/bonding techniques

Thank you for your time!