International silicon detector activities

FCC R&D Collaboration Meeting, Italy, 15 December 2021

Harald Fox

List of institutes

Physics | Lancaster University

- Australia
  - University of Adelaide
- China
  - Institute of High Energy Physics, CAS
  - Shang Dong University
  - Tsinghua University
  - University of Science and Technology of China
  - Northwestern Polytechnical University
  - T.D.Lee Institute-Shanghai Jiao Tong University
  - Harbin Institute of Technology
  - University of South China
- Germany
  - Karlsruhe Institut für Technologie
- Italy
  - INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell'Insubria
  - INFN Sezione die Pisae, Università di Pisa
  - INFN Sezione di Torino, Università degli Studi di Torino
- UK
  - University of Bristol
  - STFC-Daresbury Laboratory
  - University of Edinburgh
  - Lancaster University
  - University of Liverpool
  - Queen Mary University of London
  - University of Oxford
  - STFC-Rutherford Appleton Laboratory
  - University of Sheffield
  - University of Warwick

Sensor proposal: ATLASPix

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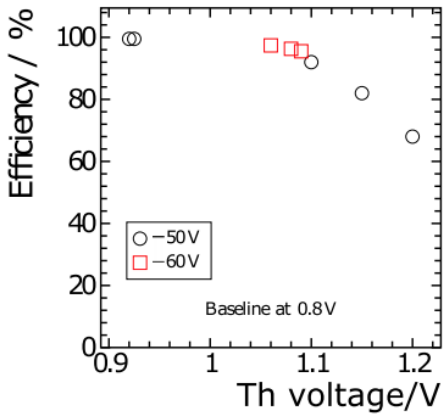
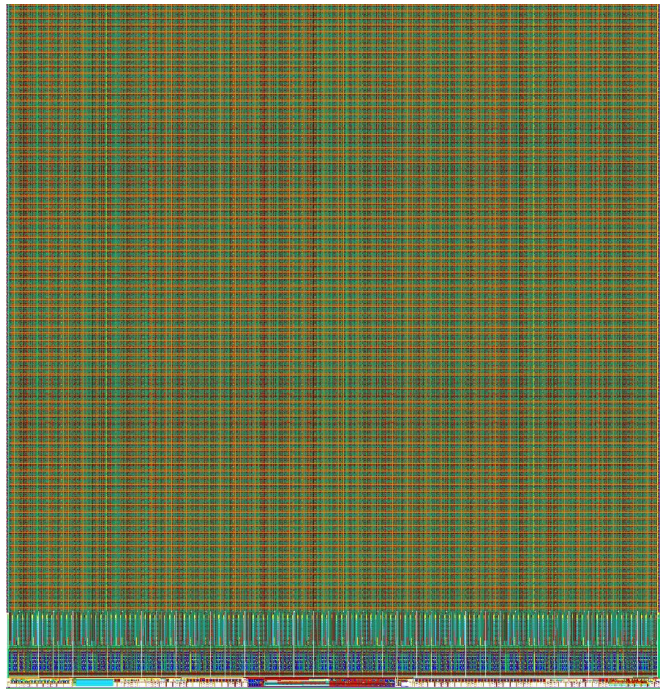
ATLASPix is a CMOS sensor developed to fulfil the requirements for the ATLAS upgrade

- Not strictly an ATLAS development
- **Monolithic CMOS** allows to produce **large** areas **fast** and **cheap**
- No hybridisation – wirebonds or C4NP bumps possible
- **25ns timing** compliant
- Hit efficiency 99.5% (ATLASPix1)
- Pixel size **150 µm by 50 µm** (or smaller)
- Triggered or triggerless readout possible
- 1.28 GBit/s downlink

I. Peric et. al., NIM A924 (2019) 99-103



ATLASPix3



ATLASPix3

- Reticule size: **2.02 cm by 2.1 cm**
- Full-size sensor, ATLASPix3 (TSI, 200Ωcm, 180nm) **available**
- 132 columns with 150µm pixel
- One column contains 372 pixels, a configuration register block, 372 hit buffers, 80 trigger buffers and two **end of column (EoC) blocks**. EoC1 is attached to hit buffers and EoC2 to trigger buffers.

Readout Systems: KIT single chip board

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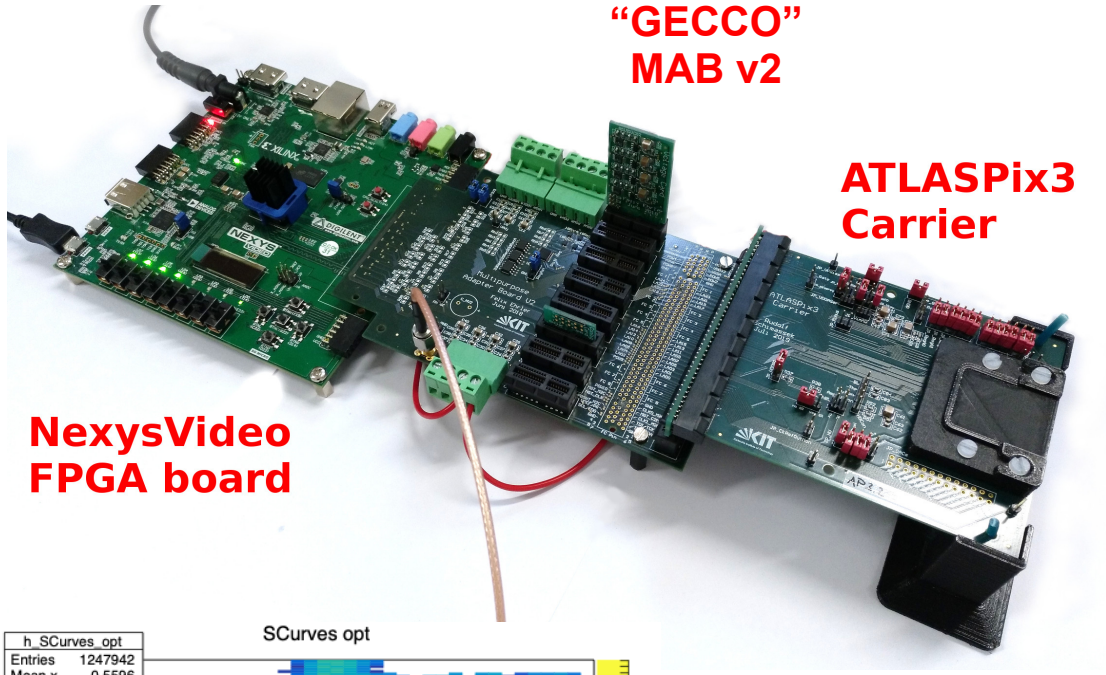
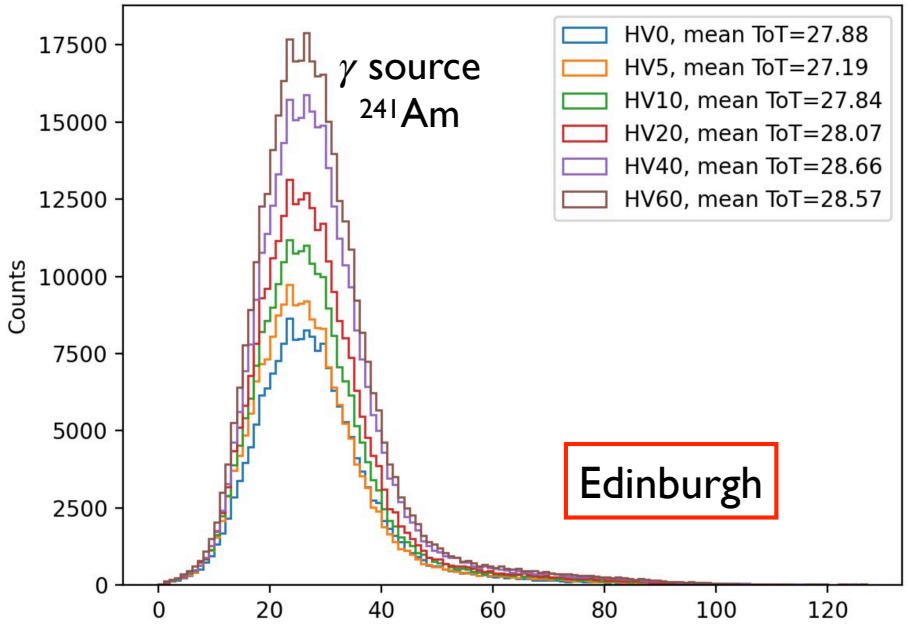
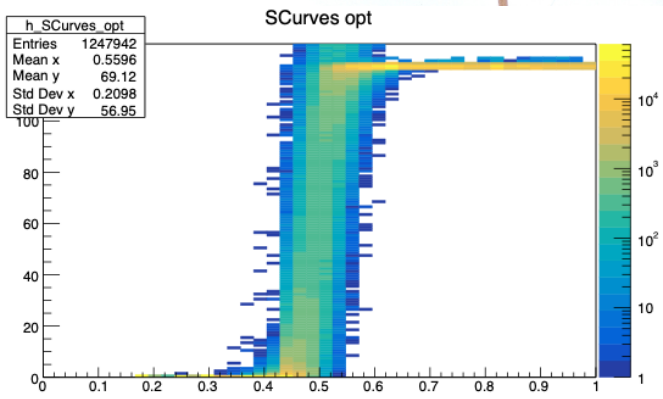
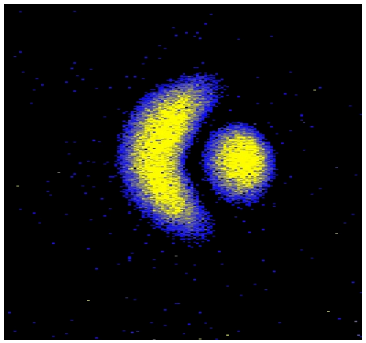
Starting point is the **ATLASPix3 single-chip card** produced by KIT and used for the tests



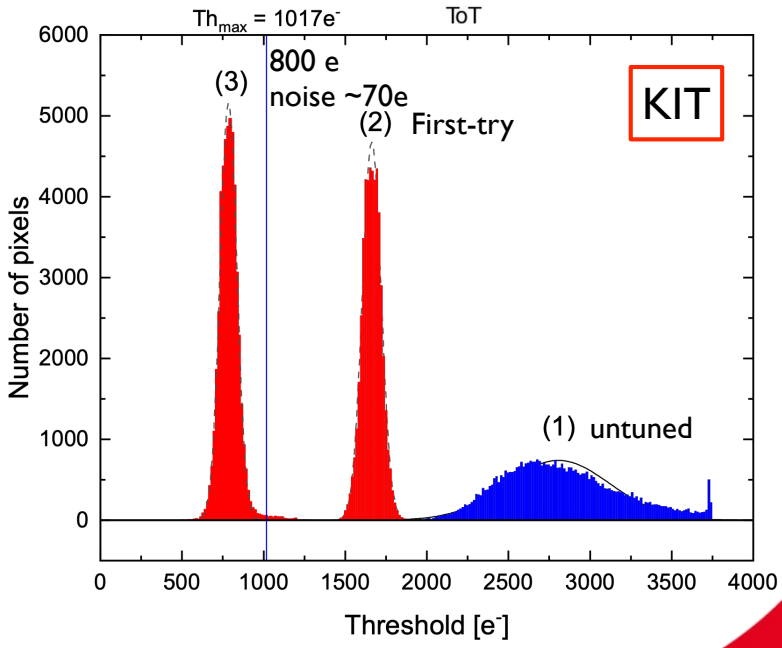




Calibration with S-Curves (injections)



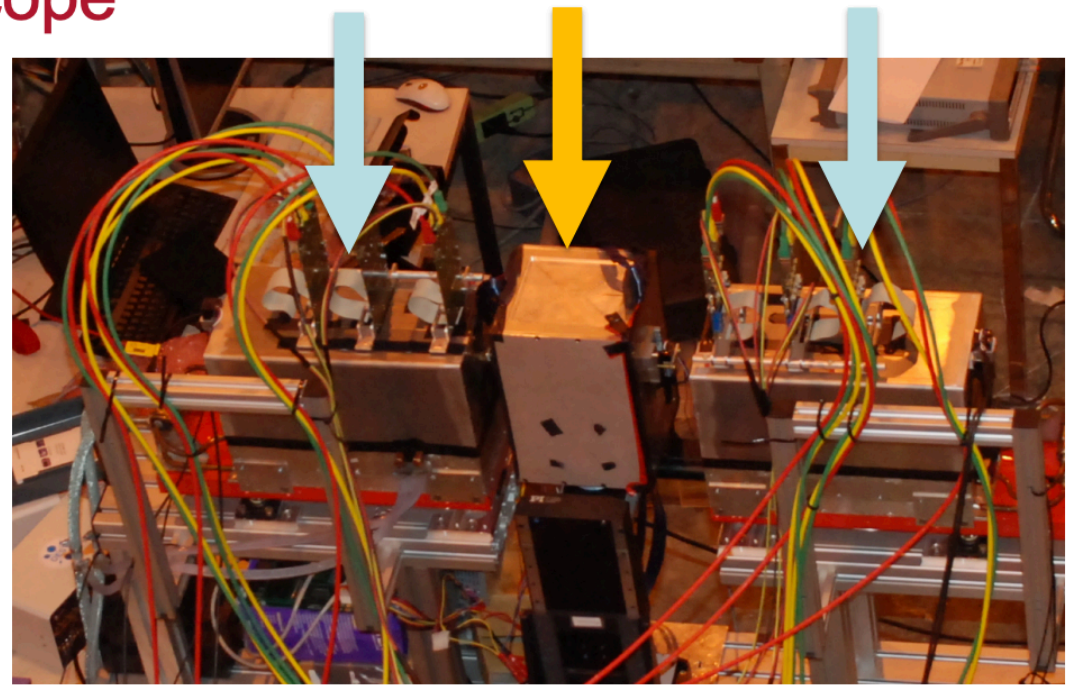
Fe-55 with collimation

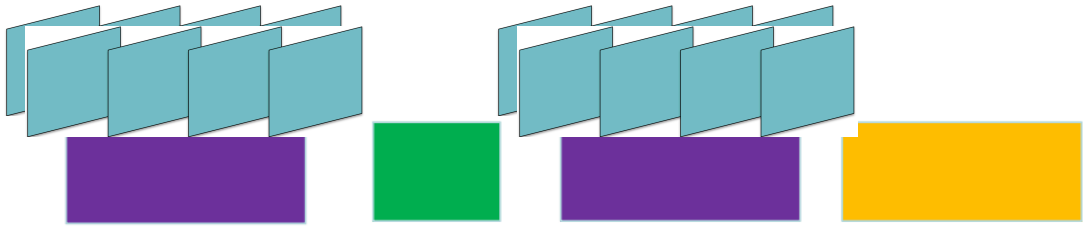


Clustering analysis and further tests ongoing.

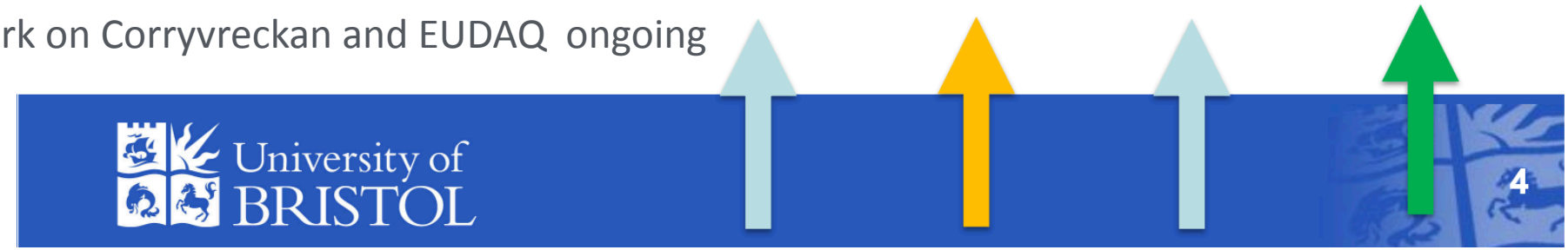
Proposed telescope

- Our DAQ system supports 4 ATLASPix3.
- We will make
  - 2 “tracking stations”
  - DUT station
  - Space for additional DUTs
- No need for trigger system: each sensor provides hits and time stamps.
  - Can synchronize the reset signal.





Work on Corryvreckan and EUDAQ ongoing



Sensor Development

Karlsruhe Institute of Technology

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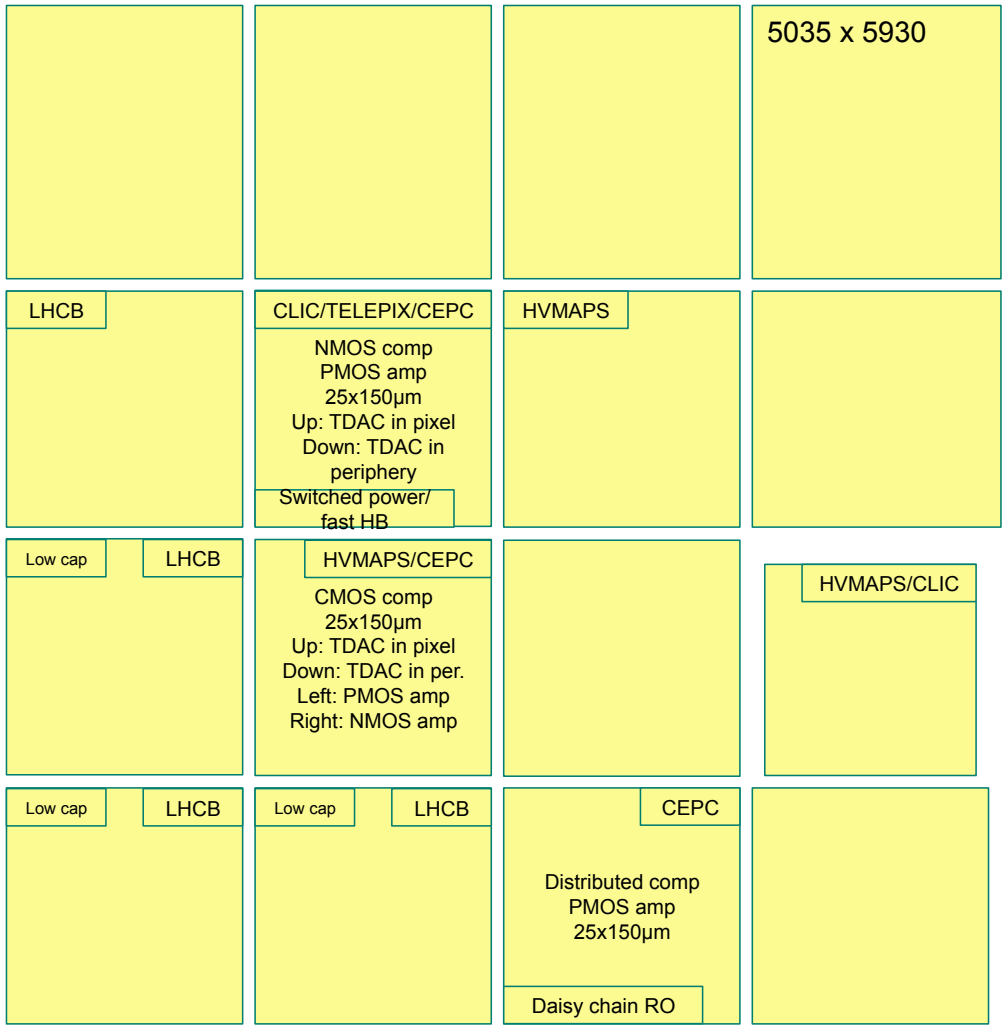
Engineering run developing ATLASPix3 family. Reticule map:



Collaboration with **LHCb Mighty Tracker** and other projects.

CEPC institutes make a **significant contribution** to the cost of the submission.

Test evolvement of ATLASPix3:

- Smaller pixel size (**25µm**) in ϕ direction
- **Lower capacitance**
- **Amplifier (PMOS → N/C-MOS) and comparator (NMOS → P/C-MOS) design**
- Electronics in **pixel or periphery**
- **Daisy chain** of readout

Sensor development

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Options:

Different pixel sizes

Different amplifier types (NMOS and PMOS)

Different comparator types (NMOS, CMOS and distributed)

Different TDAC types (placed in pixels or in periphery)

Fixed improvements versus ATLASPIX3

Hit buffer cell with time to digital converter (supports time resolution ~ 100ps), TDAC, differential receiver for distributed comparator

Possibility of daisy-chain readout – one chip acts as data collector for another

Possibility to bias pixel n-well with voltage higher than 1.8V, and to bias pixel p-well with voltage lower than 0. It reduces capacitance. Reduced capacitance means better time resolution for the same power consumption.

PMOS amplifier has lower noise than the NMOS amplifier when the bias current is high (~10µA). It has better (smaller) time walk for threshold of nine sigma noise. PMOS amplifier is more suitable for larger pixels i.e. pixels with larger capacitance (larger than 150fF)

NMOS amplifier has better time walk for nine sigma noise for small bias currents (~1µA). It is a good choice for small pixels with little capacitance. Some risk because NMOS has more flicker noise and because we have little experience with this amplifier type

NMOS comparator is the standard comparator type we used so far. It has some disadvantages: rather high current consumption (~3µA), larger delay than CMOS comparator, need for additional bias voltage of 2.1V, output signal of reduced amplitude, it occupies large area and causes large detector capacitance

CMOS comparator does not have the disadvantages of NMOS comparator, it is faster for the same current consumption, potentially more radiation tolerant, smaller. Disadvantage is that CMOS comparator needs additional deep p-well implant (iso-PMOS option). This implant will be produced by TSI for the first time – there is some risk that it does not work.

Distributed comparator has only three transistors in the pixel and adds very little capacitive load. The receiver and TDAC are placed in the hit buffer at the periphery. It is fast, low power and does not require additional iso-PMOS. The disadvantage is that it requires two lines per pixel to connect it with the hit buffer. This is not a problem for pixels larger than 50µm x 150µm.

TDAC can be placed in pixel but it adds detector capacitance. TDAC can also be placed at the periphery, in this case it makes periphery slightly larger

First measurements:

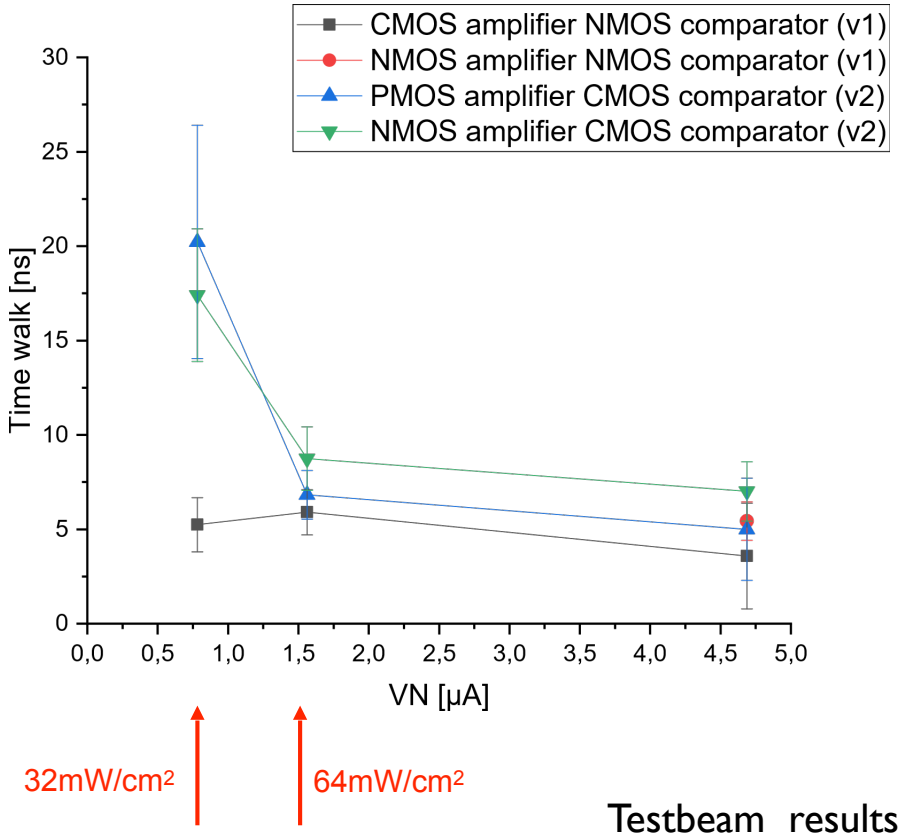
Pixel matrices with three amplifier types have been operated with smallest possible threshold

Signal to noise ratio (from ToT) and time walk for signals larger than 3200e have been measured

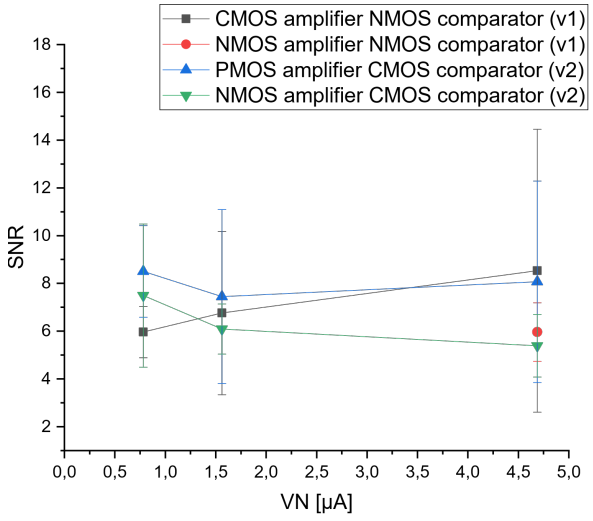
CMOS amplifier has smallest time walk

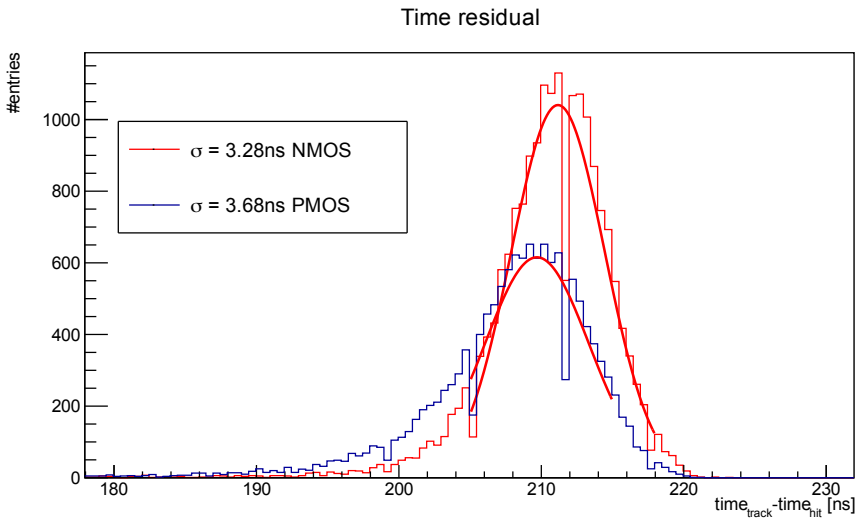
Low power consumption is possible (up to factor of 4 reduction compared with ATLASPix3)

25µm pitch gives an uncorrected resolution of 8.2µm. Analysis in progress.



ATLASPIX3: 140mW/cm²





Testbeam results curtsey of Dohun Kim (LHCb), Lennart Huth (DESY)

55nm sensor development

Shanghai Huali Microelectronics Corporation (**HLMC**) is a Chinese foundry. As of 2018, HLMC had 55 nm, 40 nm, and 28 nm process technologies and are capable of producing up to 35,000 wafers per month.

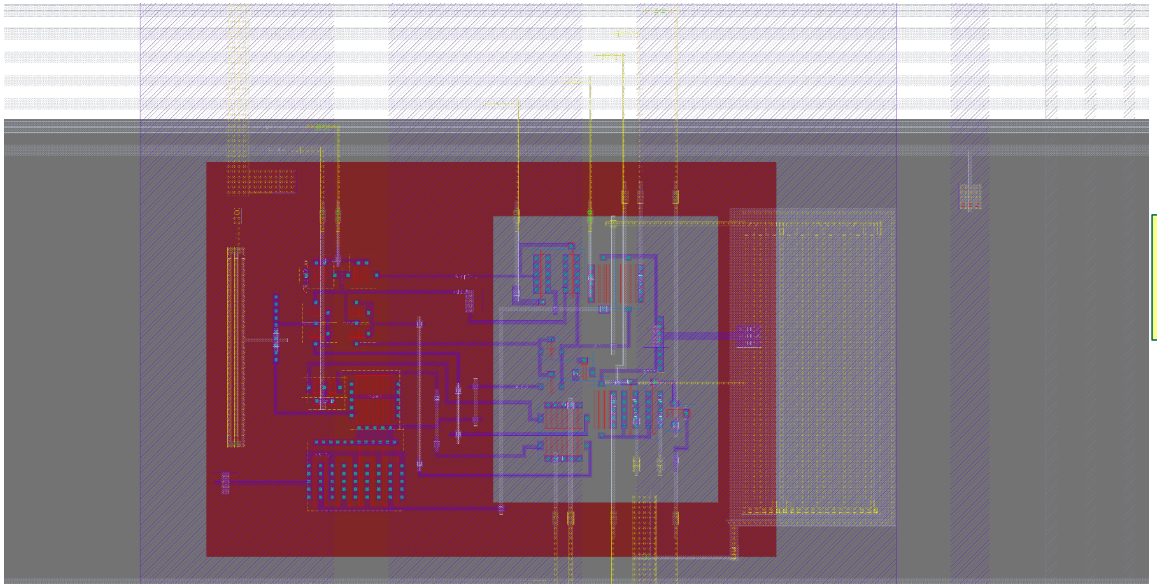
We have started with design of the dedicated CEPC design in the HLMC 55nm HVCMOS technology

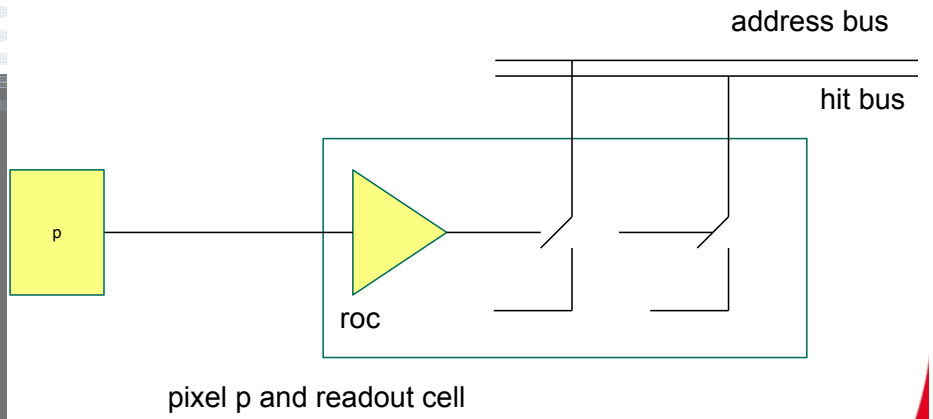
The test sensor 3 × 2 mm2 should be submitted within an MPW run March 2022

HLMC technology offers similar layers as TSI: deep n-well, maximum voltage for HV transistors is 32V, Metal layers 1 – 6 can be used for fine pitch routing, three more thick metal layers, suitable for power, LV 1.2V

The realistic pitch is down to 0.2um – relaxed and according to recommendation is 0.3 (in 180nm was 0.6)

There are only hspice models available, we used Mentor Calibre for DRC LVS





pixel p and readout cell

Ivan Peric: *UK-CEPC tracker workshop*

Cooling measurements

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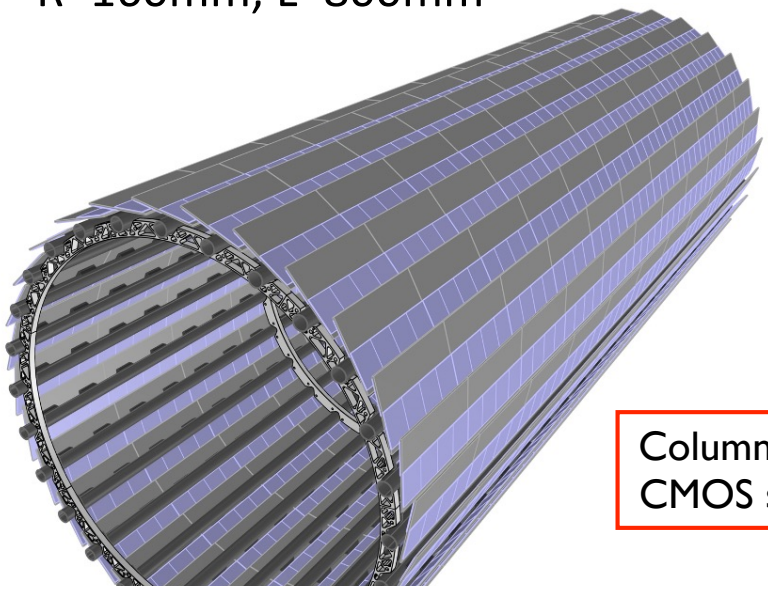
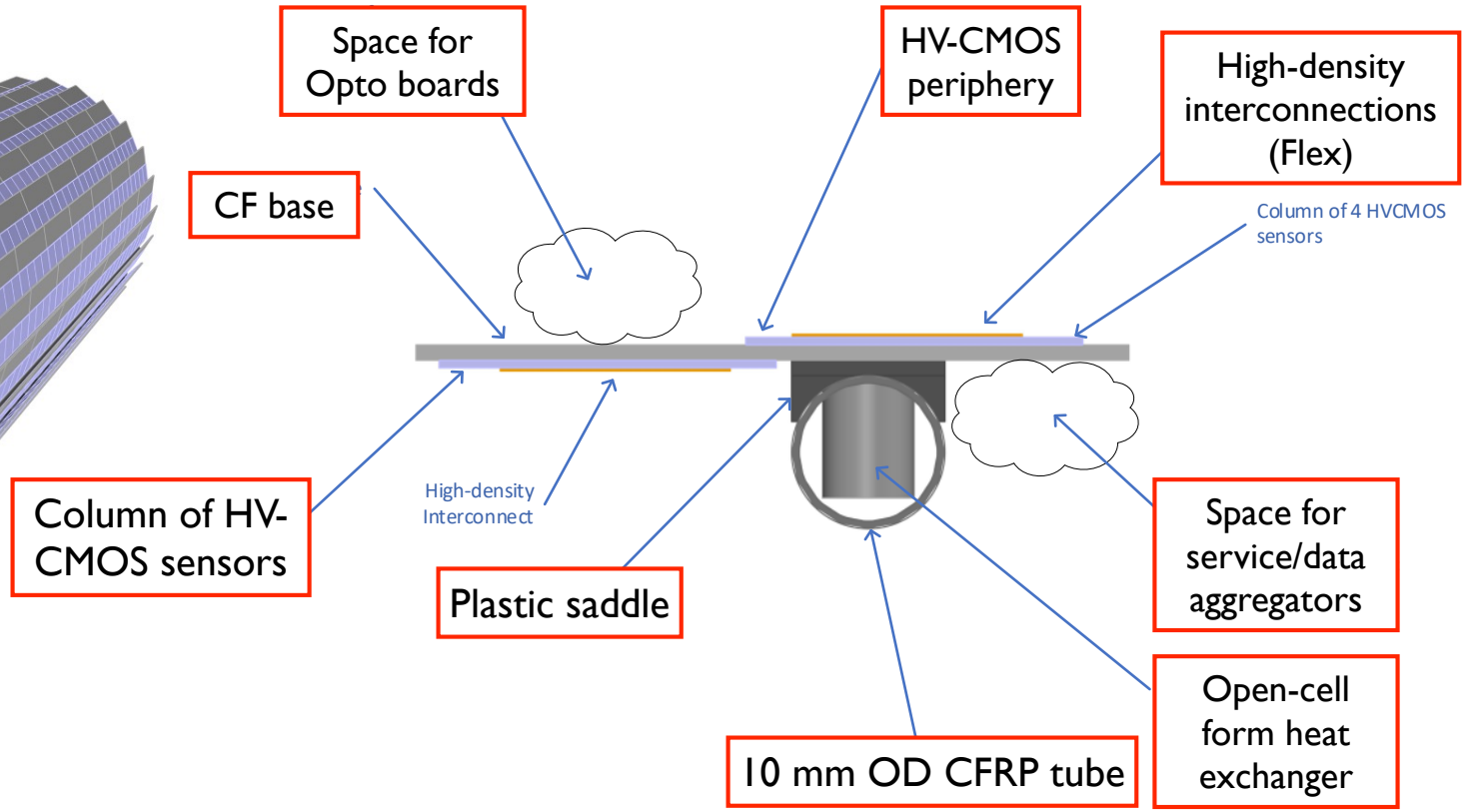
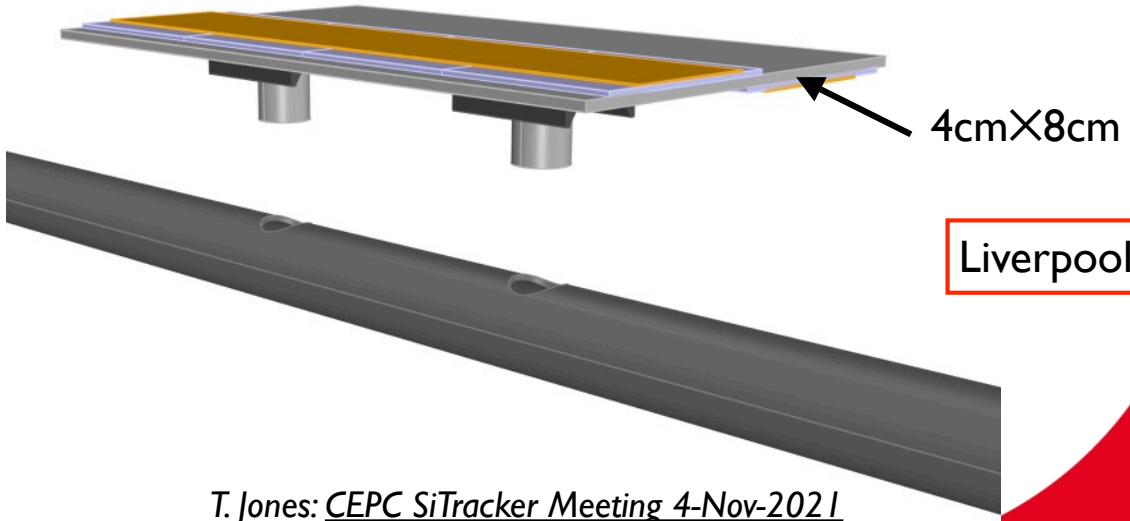
R=160mm, L=800mm





- HV-CMOS sensors glued to CF base
  - Asymmetric arrangement with peripheral areas as close as possible to the middle where power consumption is max
- Base attaches to support tube via two saddles
- Saddles have apertures through which the foam heat exchangers pass and glue to the base



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Pre-prototype thermal evaluations

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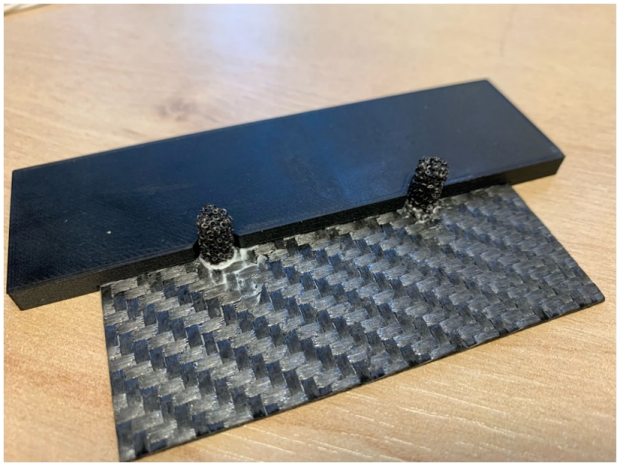
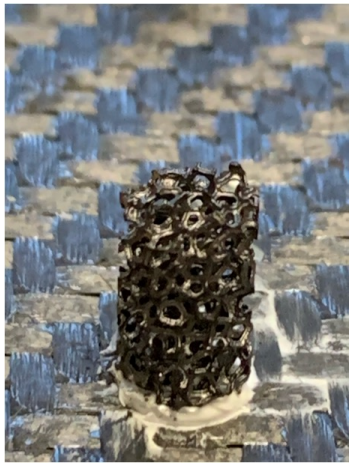
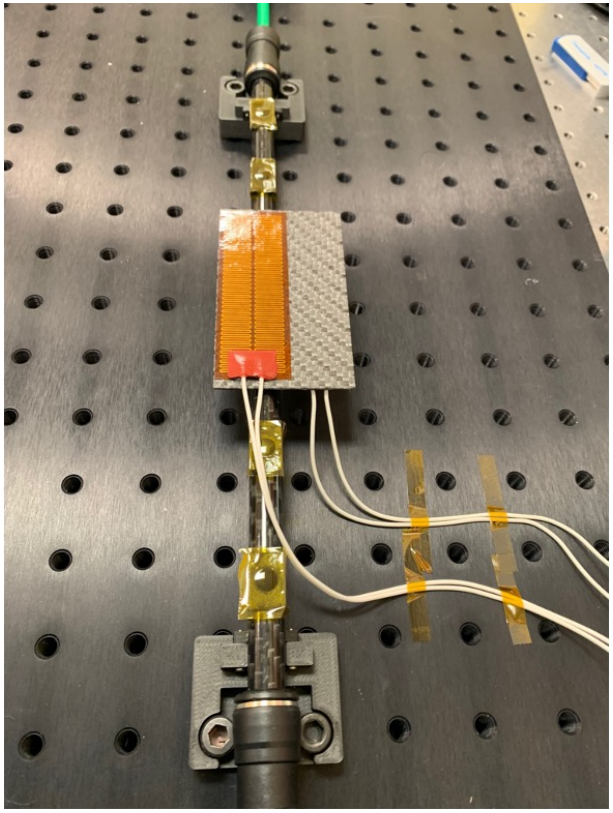
Pre-prototype: Base attached to tube & heaters on







- Investigate performance of high-thermal conductivity (eg Allcomp) foams as a heat exchanger
  - Combination of large area and increased stream velocity through foam can lead to high efficiency
- Characterise performance (i.e. temperature rise vs power) for different flow velocities
- Develop FEA models simulating the fluid flow through foams

*First look: at 3.1W power (expected from 8cm*4cm area), temperature rise ~10 degrees w.r.t. CDA*

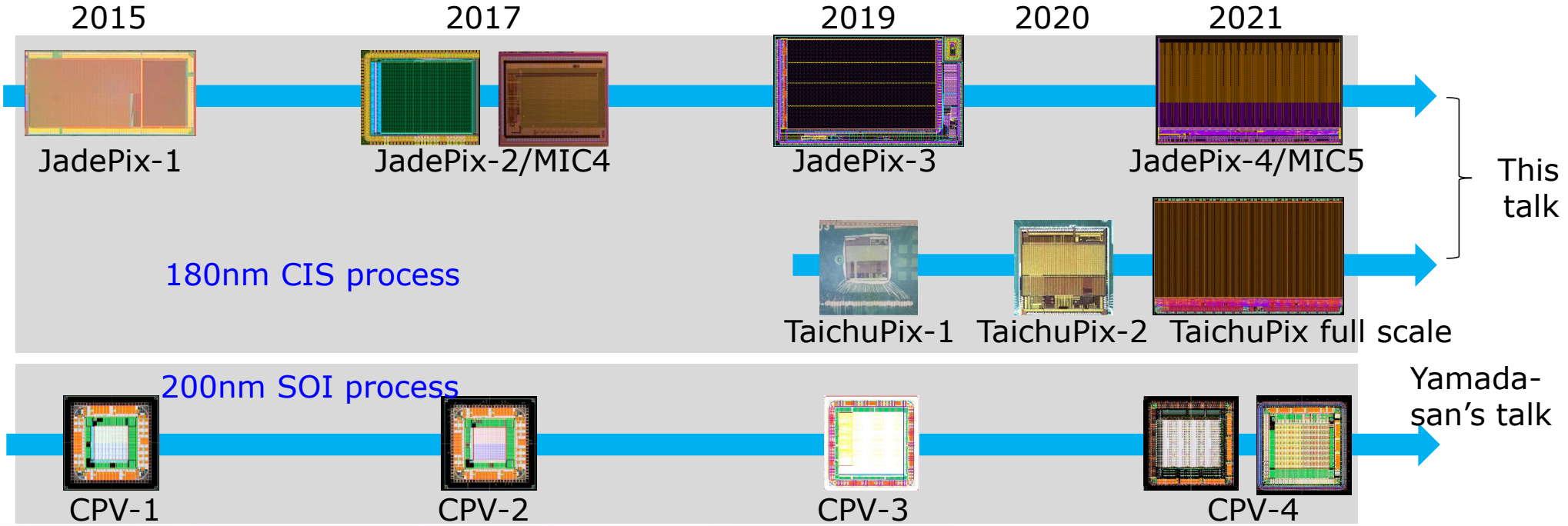
Liverpool

T. Jones: CEPC SiTracker Meeting 4-Nov-2021

Sensors for the vertex detector

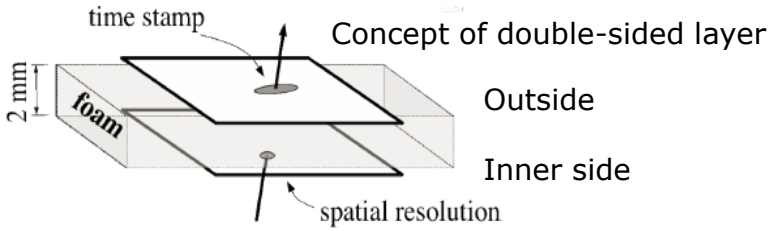
Projects in China

- Development of pixel sensor for CEPC are supported by
  - Ministry of Science and Technology (MOST)
  - National Natural Science Foundation of China (NSFC)
  - IHEP fund for innovation

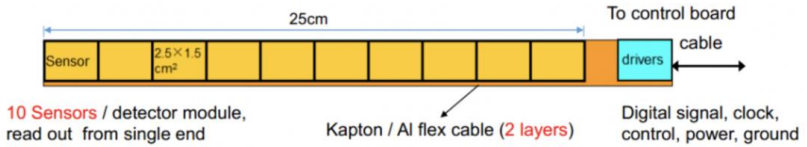


Strategies to address the challenges

- JadePix sticks to a double-sided concept
  - Pitch, power, readout speed
  - A pair of complementary design envisioned



- TaichuPix stresses on the system level
  - Full scale prototype for ladder assembly
  - Fine time stamp & Radiation hardness to cope with Z-pole mode



Schematic of full scale sensors on the ladder

Impact parameter resolution

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

Vertex detector specs

$\sigma_{s.p.}$ ~ 2.8um ----------> **Small pixel** ~ 16um

Material budget ~ 0.15% X_0/layer ----------> **Thinning to** ~ 50um

----------> **low power** ~ 50mW/cm^2

r of Inner most layer ~ 16mm ----------> **fast readout** ~ 1us

----------> **radiation tolerance** ~

$\leq 3.4\ Mrad/year$

$\leq 6.2\times10^{12} n_{eq}/(cm^2\ year)$

JadePix3/4 and TaichuPix comparison

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	Jadepix3	Jadepix4 (submitted)	Taichupix
Foundry	TowerJazz 180nm CIS	TowerJazz 180nm CIS	TowerJazz 180nm CIS
Readout	Rolling Shutter	Asynch. Enc. and Reset Dec.: AERD	Column Drain
Integration time	<100 µs	~1 µs	
Pixel size	16 × 23.11 µm2	20 × 30 µm2	25 × 25 µm2
Resolution	~3 µm (laser)	5 µm	25/√12=7.2µm
Power	~91 mW/cm2 (extrapolated)	<100 mW/cm2	

JadePix3

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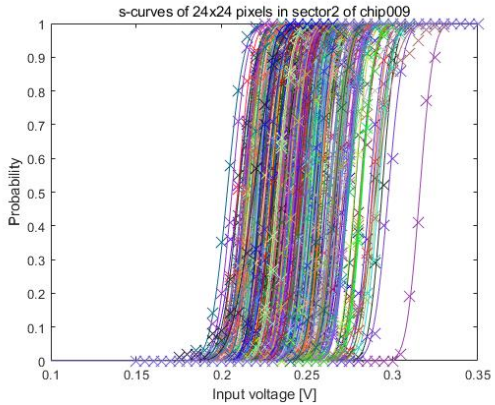
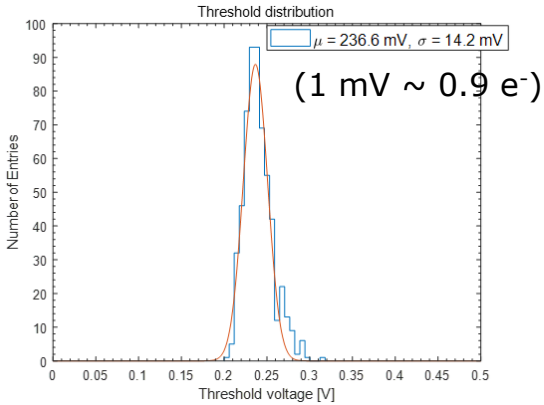
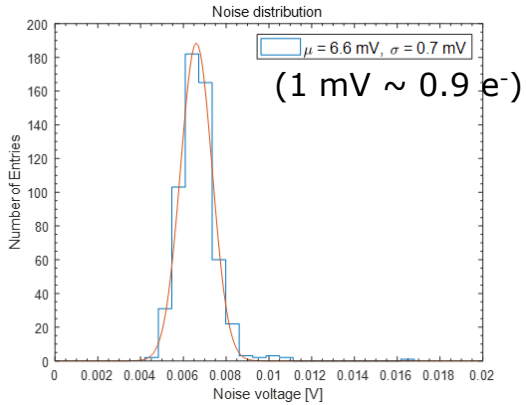
- Pulse amplitude scan and **S-curve*** fit @ nominal threshold

*S-curve: cumulative Gaussian distribution

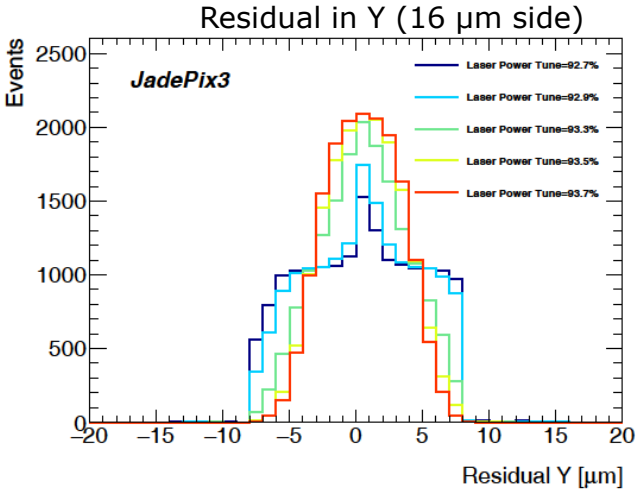


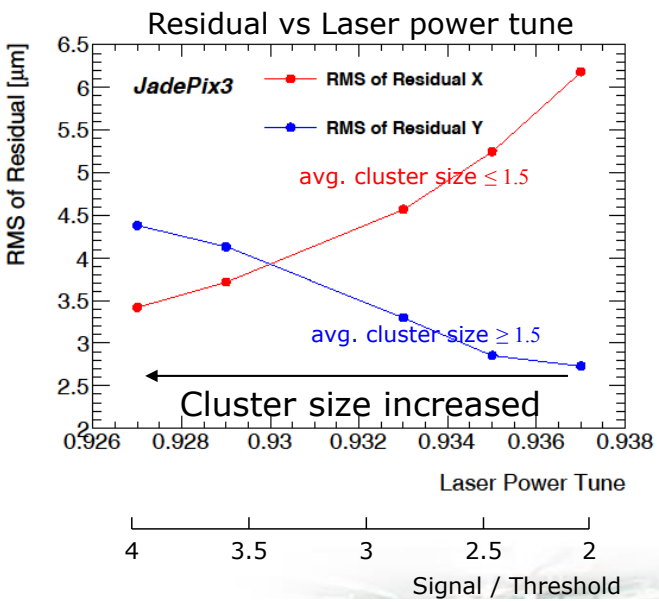




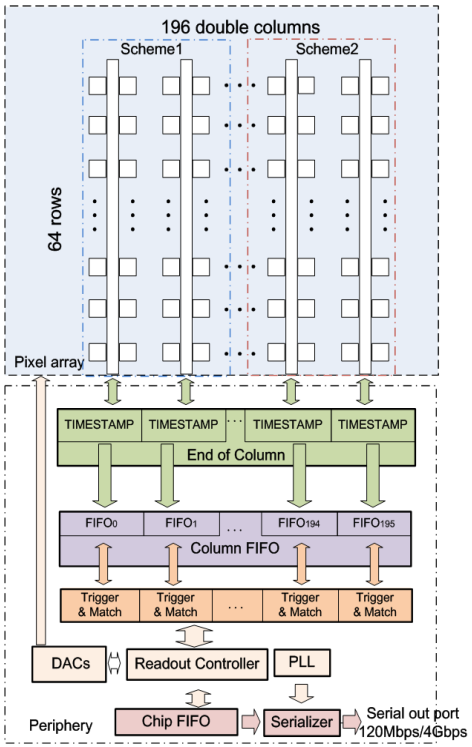
- **Minimum value** as cluster size approaching 1.5
  - 3.34 μm @ signal = 880e⁻ in X
  - 2.31 μm @ signal = 440e⁻ in Y

Laser measurement



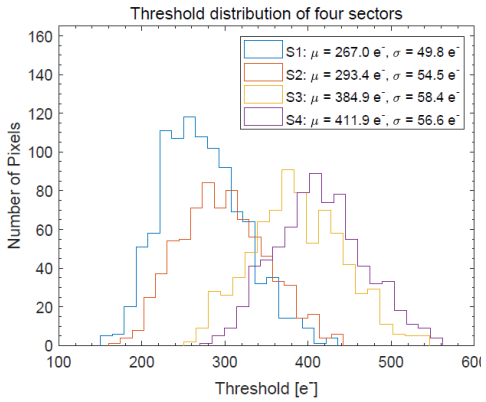


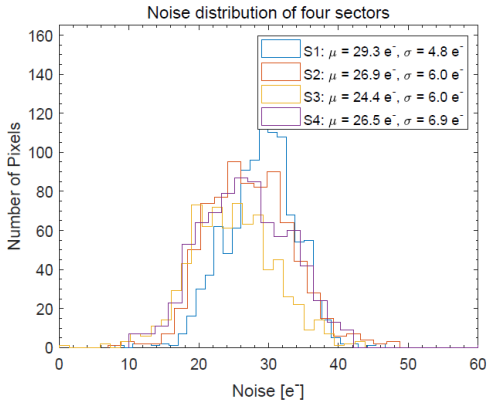
TaichuPix architecture



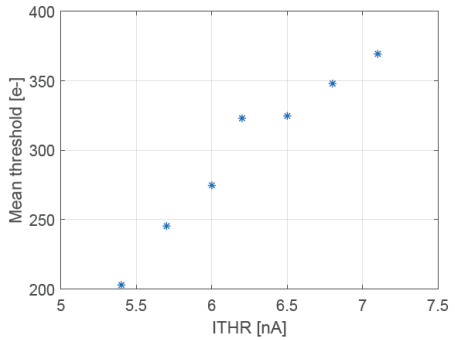
- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - Priority based data driven readout, zero-suppression intrinsically
  - Modification: **time stamp is added at EOC** whenever a new fast-or busy signal is received
  - **Dead time**: 2 clk for each pixel (**50 ns** @40 MHz clk)
- **Two parallel pixel digital schemes**
  - ALPIDE-like: Readout speed was enhanced for 40 MHz BX
  - FE-I3-like: Fully customized layout of digital cells and address decoder for smaller area
- **2-level FIFO architecture**
  - L1 FIFO: In column level, to de-randomize the injecting charge
  - L2 FIFO: Chip level, to match the in/out data rate between the core and interface
- **Trigger readout**
  - Make the data rate in a reasonable range
  - Data coincidence by time stamp, only matched event will be readout

TaichuPix

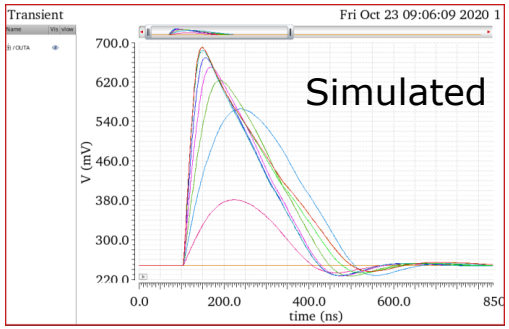




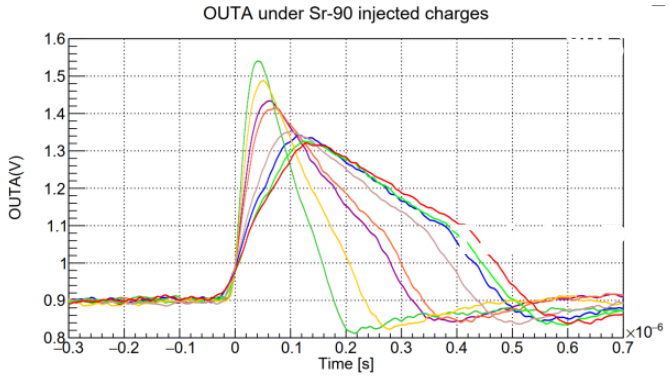
Mean threshold vs. Threshold current ITHR



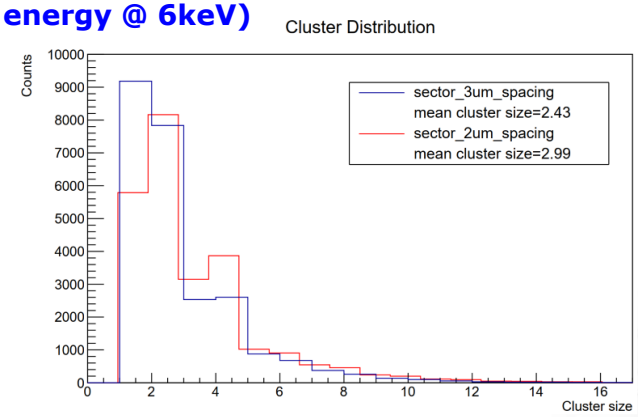
Chip4	Threshold Mean (e⁻)	Threshold rms (e⁻)	Temporal noise (e⁻)	Total equivalent noise (e⁻)
S1	267.0	49.8	29.3	57.8



TaichuPix2 response to X-ray tube (cutting energy @ 6keV)

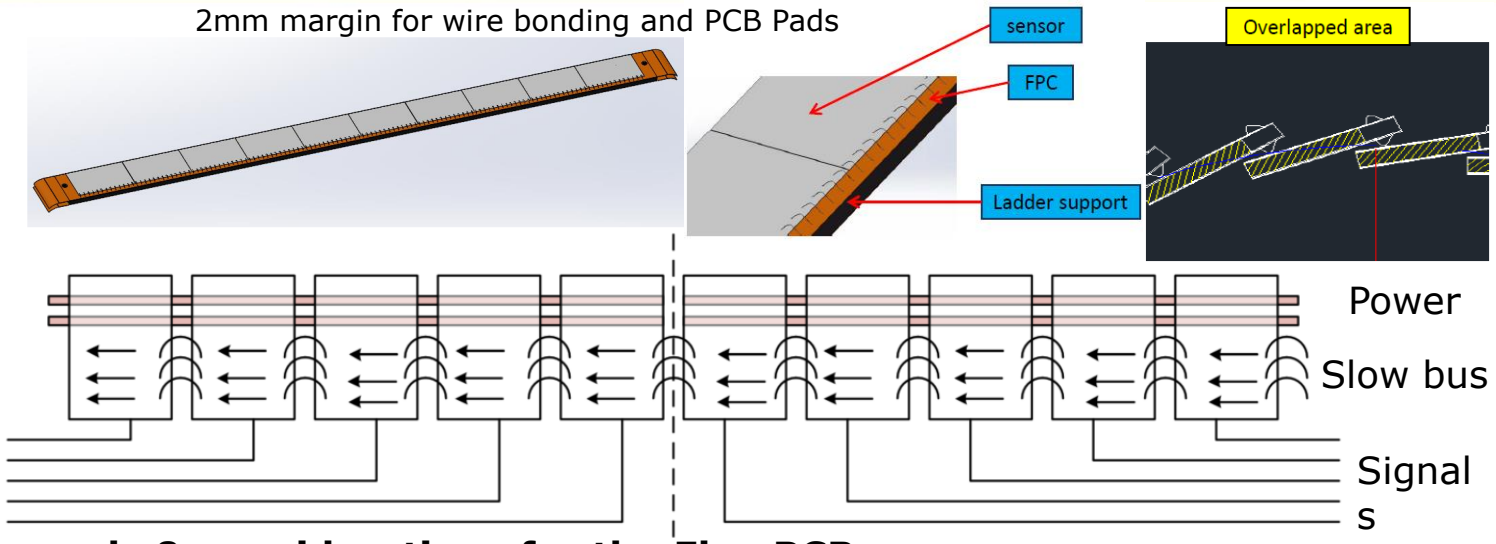


TaichuPix1 response to **^{90}Sr** exposure



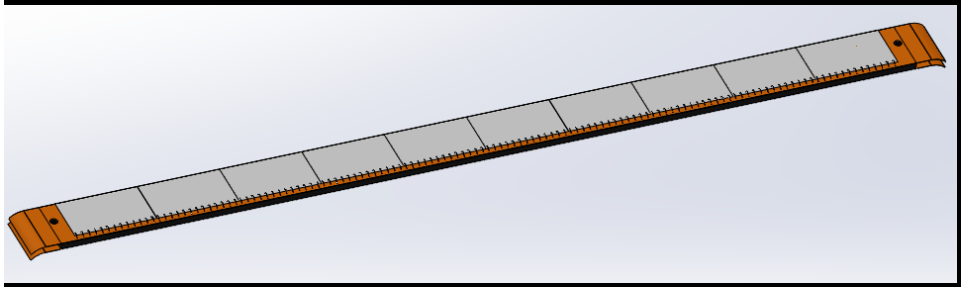
TaichuPix1 cluster size to **^{90}Sr** exposure

Flex cable design consideration (TaichuPix)

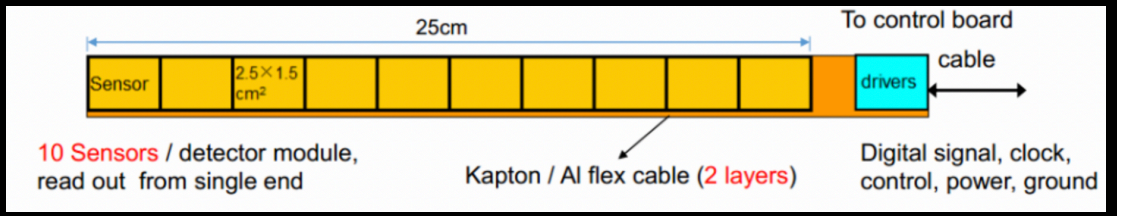


- **Design goals & considerations for the Flex PCB**
  - Minimum material budget
    - Minimum dead zone extension, limited height of PCB
      - Minimum set of signals on Flex
      - Inter-chip connection for slow controls through wire bonding → save some space & metal on PCB
    - Robust power supply
  - Manufacturability

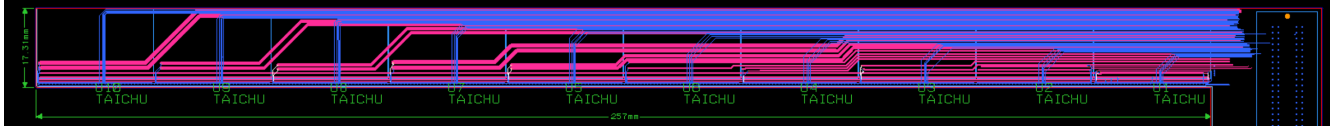
3D model of the ladder



Schematic of ladder electronics



Design of Flexible PCB prototype

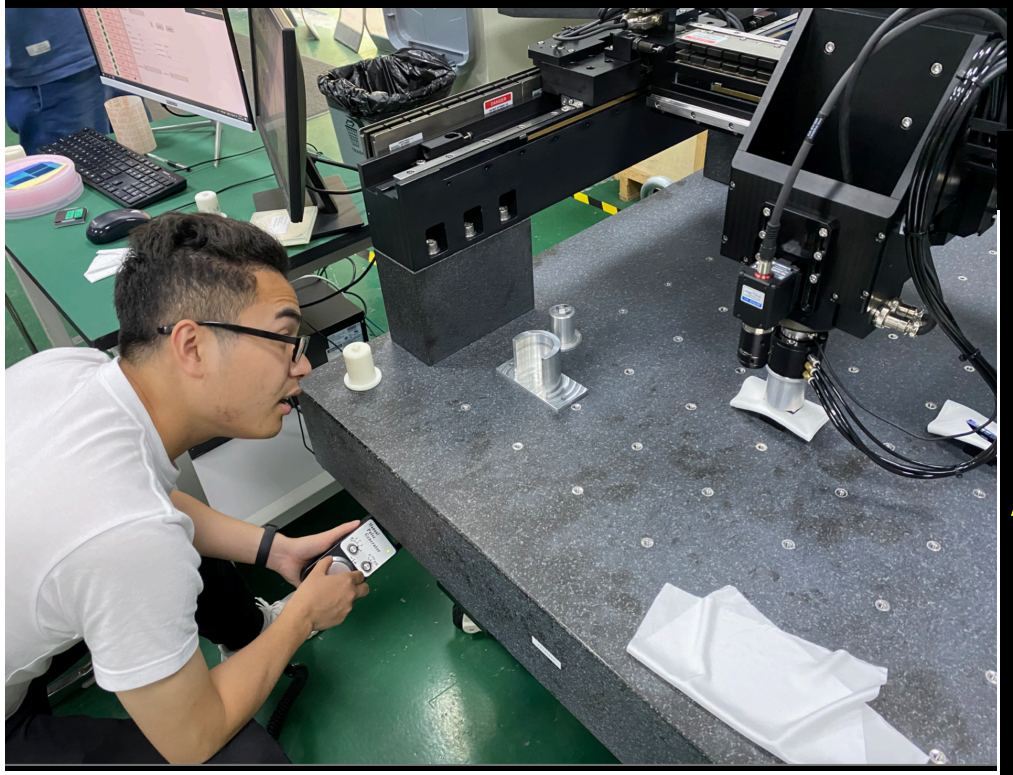


- Double side flex + rigid PCB for 10 chips(15.31 X 25.6mm)
  - 17.31mm X 257mm for flex part.
- Copper thickness: 0.5oz (18um)
- Signal width: 3mil/3mil, power supply width:20~60mil

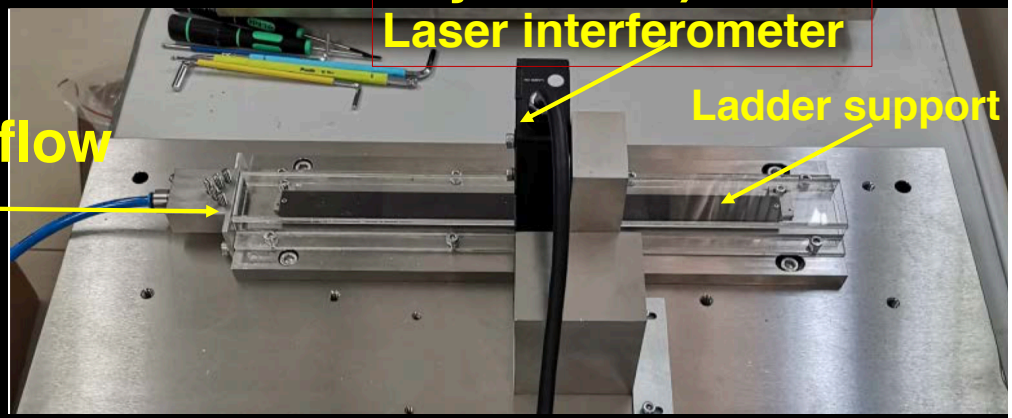
Profile of flexible PCB

	Achieved Thickness (μm)	Optimization goals (μm)
Polyimide	25	12
Adhesive	28	15
Plating Cu	17.8	17.8
kapton	50	50
Plating Cu	17.8	17.8
Adhesive	28	15
Polyimide	25	12

Gantry system



Test setup prototype for ladder cooling
Use compressed air for cooling
(See more from Jinyu's talk)



Conclusion

A good sensor for the tracker is in hand

Development possible with quick turnaround time:

- gain factor 2 in ϕ-resolution
- gain factor 4 in power consumptions

Long term option in preparation (55nm technology at Chinese fab)

Development of sensors for vertex detector ongoing

Converging of three different design options?