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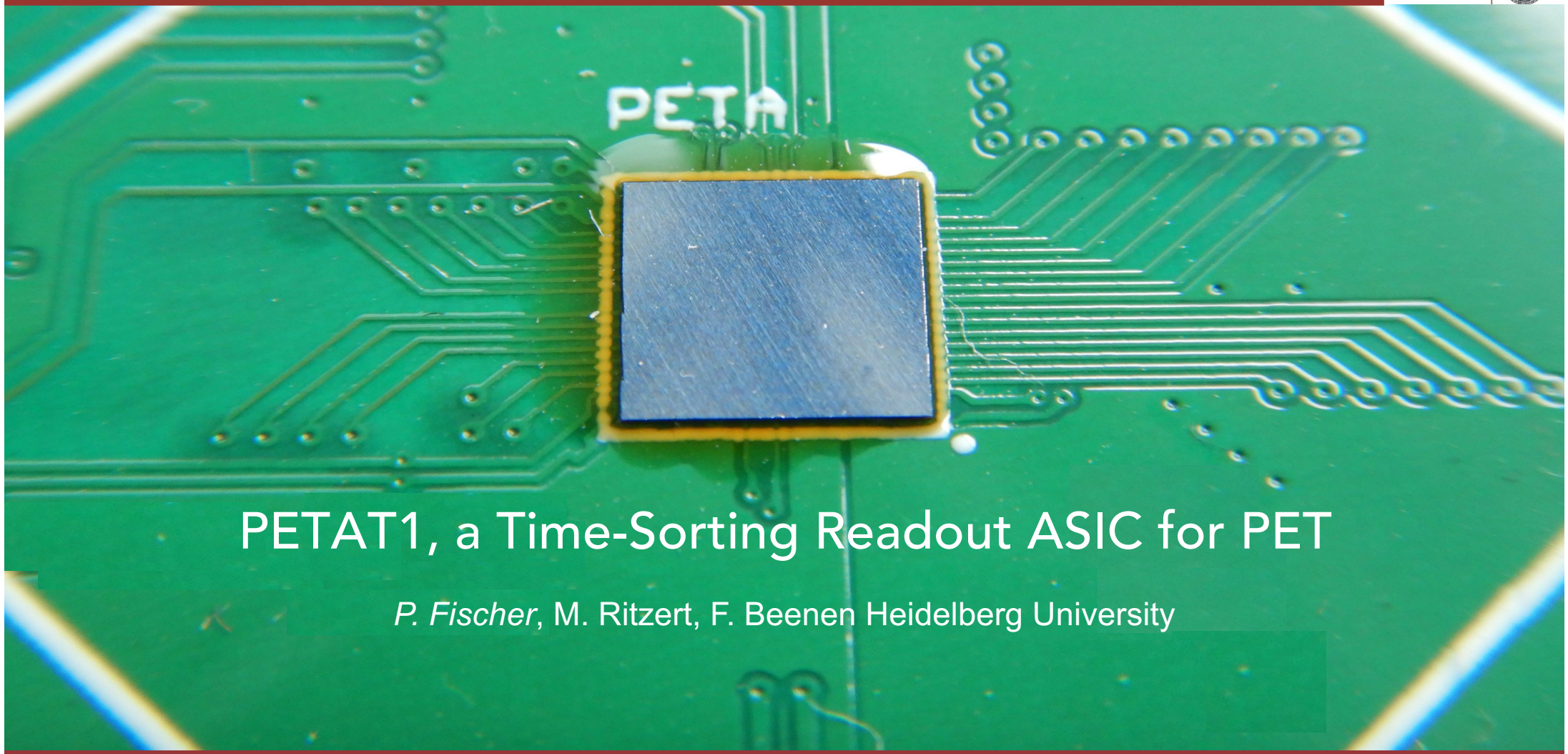

PETAT1, a Time-Sorting Readout ASIC for PET

P. Fischer, M. Ritzert, F. Beenen Heidelberg University

‘State if the Art’ PET Readout

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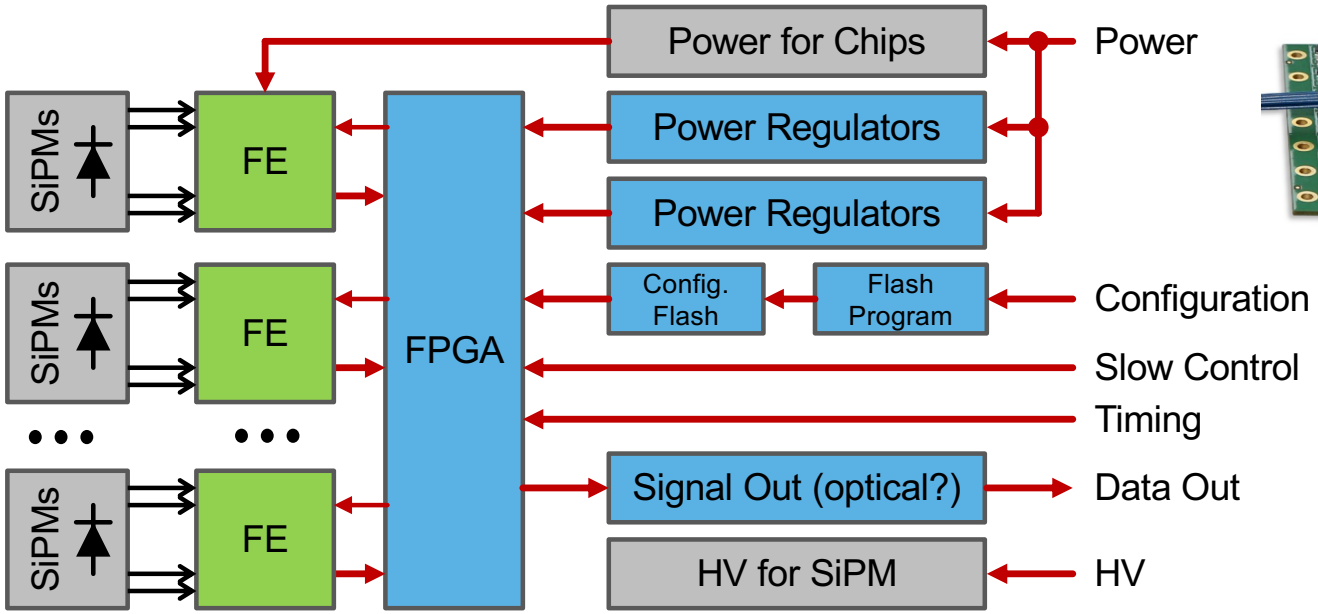
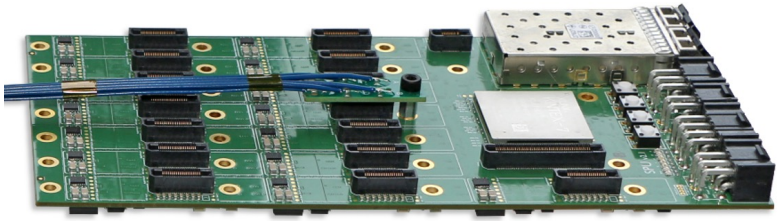
– Most modern PET readout systems use specialized ASIC to read SiPMs
– These transfer their data to FPGAs for data aggregation





Hyperion III platform as presented e.g. by D. Schug yesterday here

– FPGA & its infrastructure add *complexity, space, power, need cooling*, …
This is particularly problematic for Total Body PET Scanners with many channels and restricted space
– *Can this be improved ?* ***– Yes. (this talk…)***

Basic Concept

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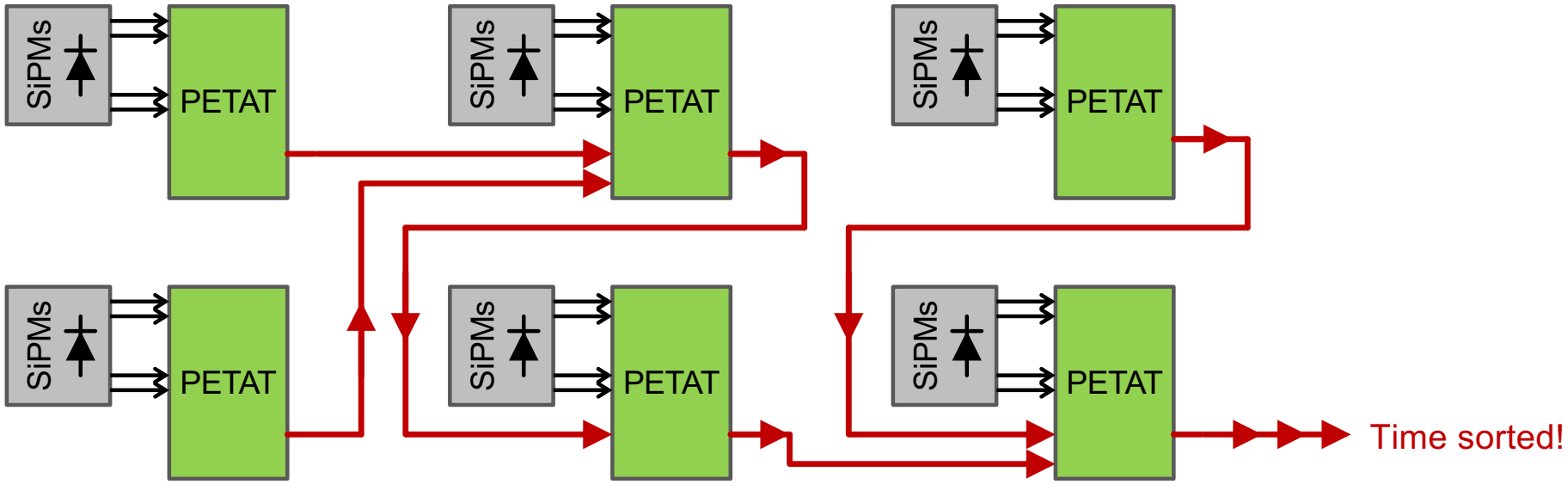
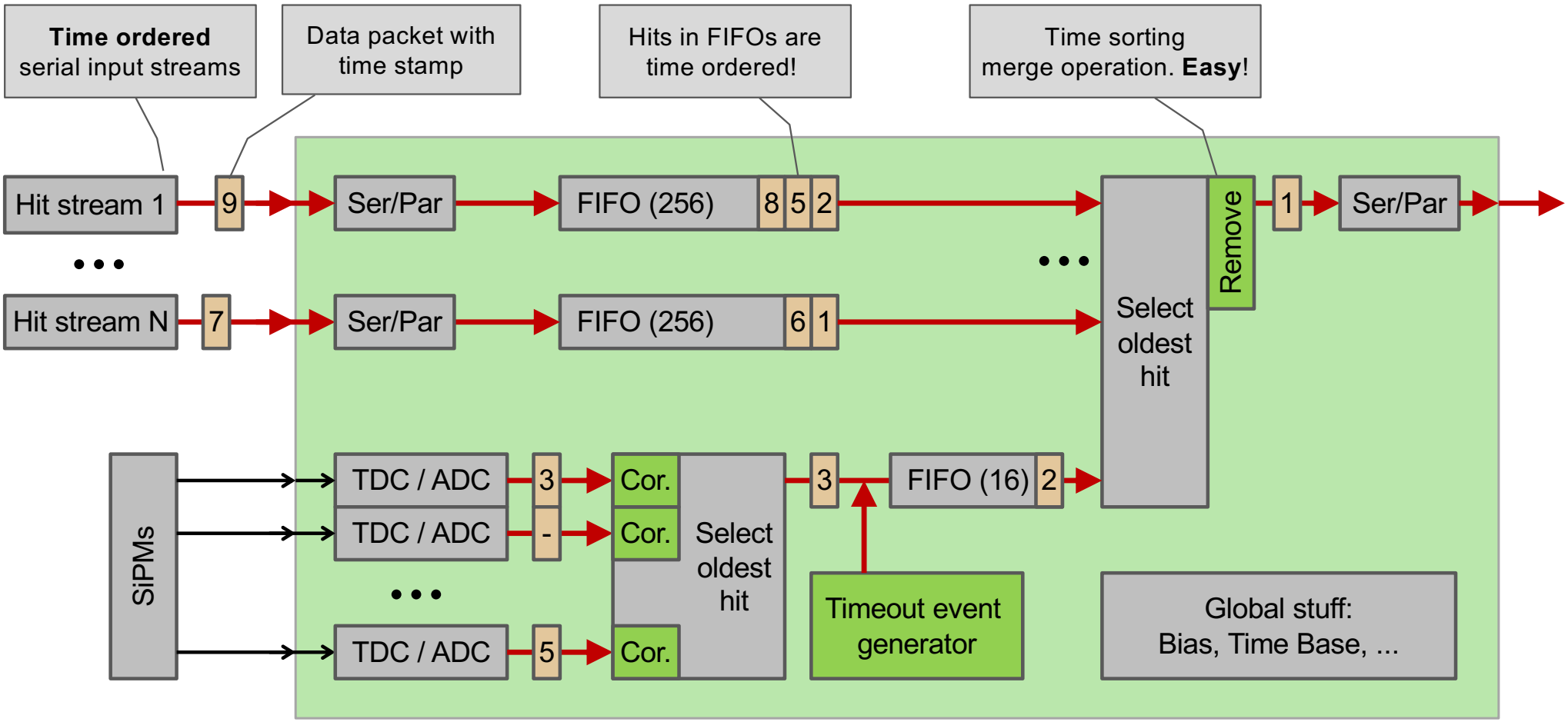
– Each chip generates own data from SiPM inputs (amplify, time stamp, integrate, get amplitude)
– In *addition*, chips can *receive* (serial) data from *other chips.*
– Each chip *merges the data* and sends it out (serially) - *No more FPGA* required!



– This approach allows it to generate a time-ordered hit data stream!

Inside PETAT1 (simplified)



The Fabricated PETAT1 Chip

Starting Point: PETA8

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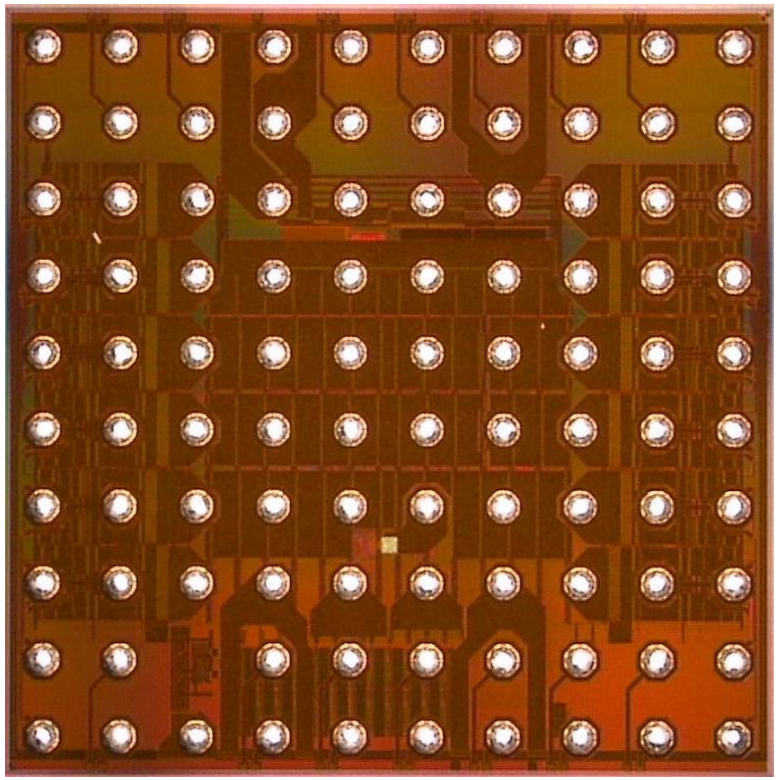
My group has developed the PETA8 SiPM readout chip:

– 32 Channels
– ~13 mW / channel (analogue + digital, incl. global blocks)
– TDC with 50 ps / bin
– Charge integrator with 9 Bit ADC
– JTAG, neighbour Logic, solder balls, …

This chip / its predecessor is being used by several PET/MRI scanner projects:

– SAFIR (ETH Zürich, see J. Debus's talk yesterday here)
– RF penetrable PET (C. Levin et al., Stanford University)
– (others upcoming)

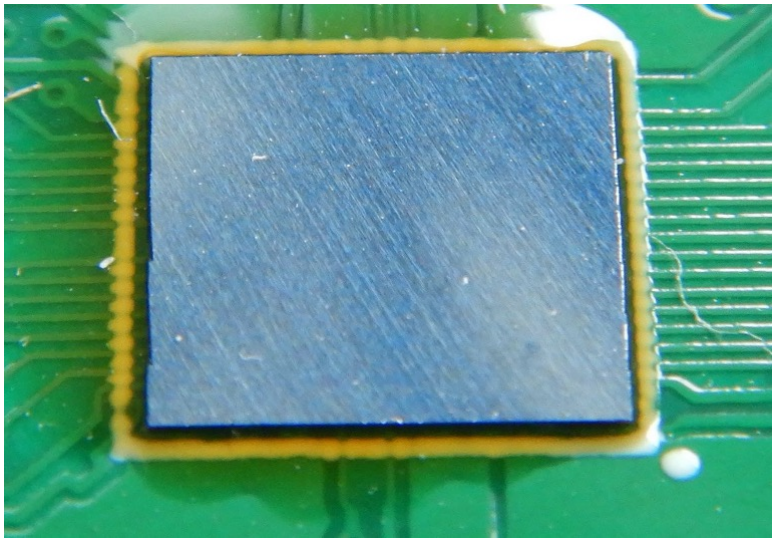
System CRT is ~*194 ps* / *242 ps*



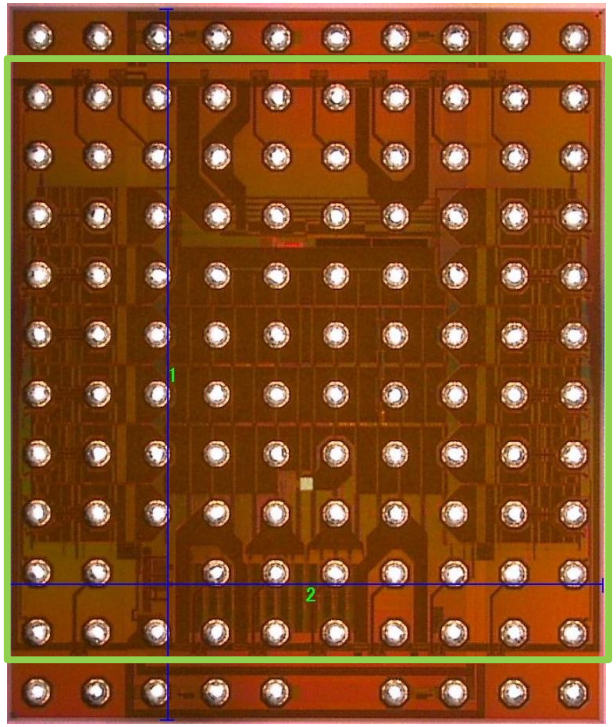
PETA8 chip photograph

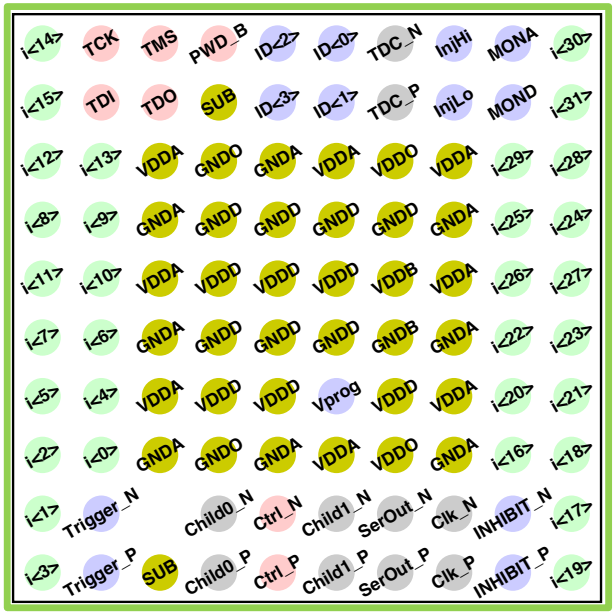
PETAT1

– PETAT1 has been designed and fabricated in 180nm CMOS technology
– It comes as a naked die of 5 x 6 mm^2 size (upper / lower rows are test structures)
– Solder Balls in 500 µm pitch allow for simple flip chip soldering



PETAT1 flipped to a test PCB





(Signals and Pins)

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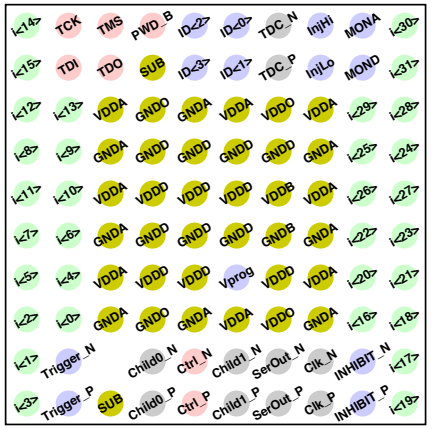
– PETAT1 has very few *mandatory* pins:

Category	Pins	Mandatory Signals
Power	4	Analogue, Digital
SiPM Inputs	32	Single ended inputs
Slow / Fast Control	1 (diff.) 4	Fast Reset, configuration, … Unique (static) Chip ID
TDC	1 (diff.)	Clock ~600 MHz
Readout	1 (diff.) 2 (diff.) 1 (diff.)	Clock Serial Child inputs Serial Output
Test	1	Analogue Injection

Category	Pins	Optional Signals
Slow Control	4 1	JTAG: TCK, TMS, TDI, TDO PowerDown
Test	1 (diff.) 1 1 1	Digital Injection 2nd analogue Injection (Lo / Hi) Analogue monitor for debugging Digital monitor for debugging
Misc	1 (diff.) 1	Inhibit = Gating Programming of Chip-ID

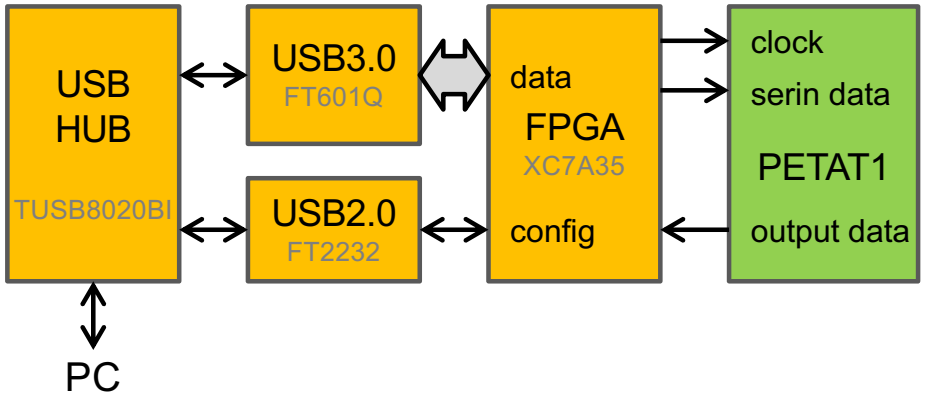
Optional pins

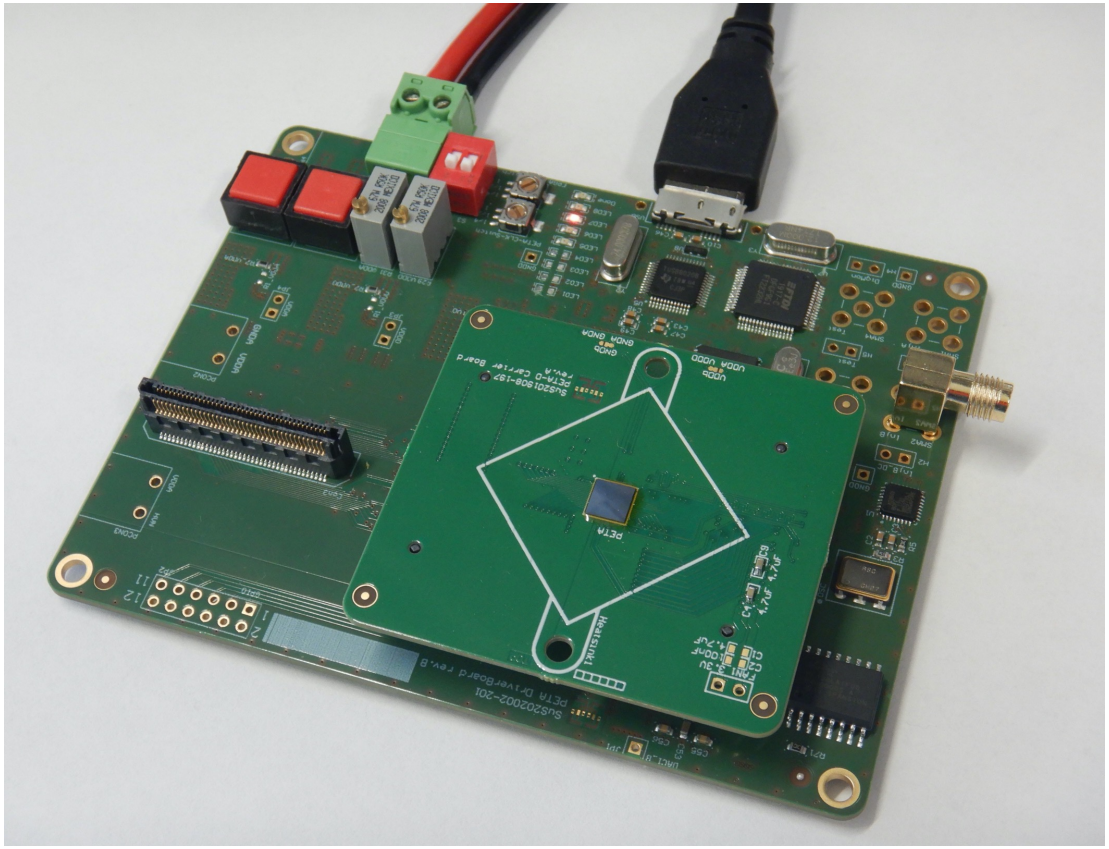


– This simplifies PCB and system design significantly (no analogue pins!)

Test Setup

– Custom USB 3.0 Board with FPGA:





– FPGA
  – generates serial input data (emulating other chips)
  – sends it to PETAT1
  – receives output data & stores it
  – Data is read via USB and analysed
– Only single chips tested so far
– All digital tests as expected 😀

Simulation

(Very Simplistic!) Simulation to Demonstrate Feasibility in PET

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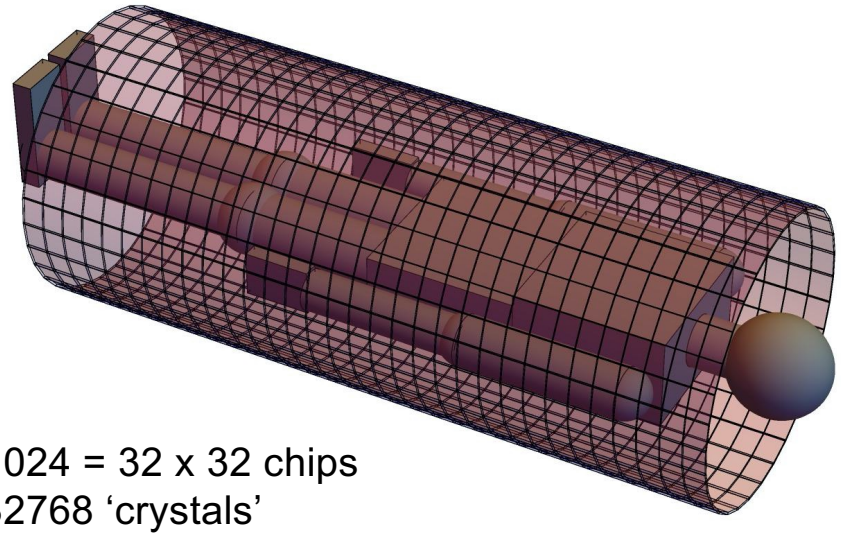
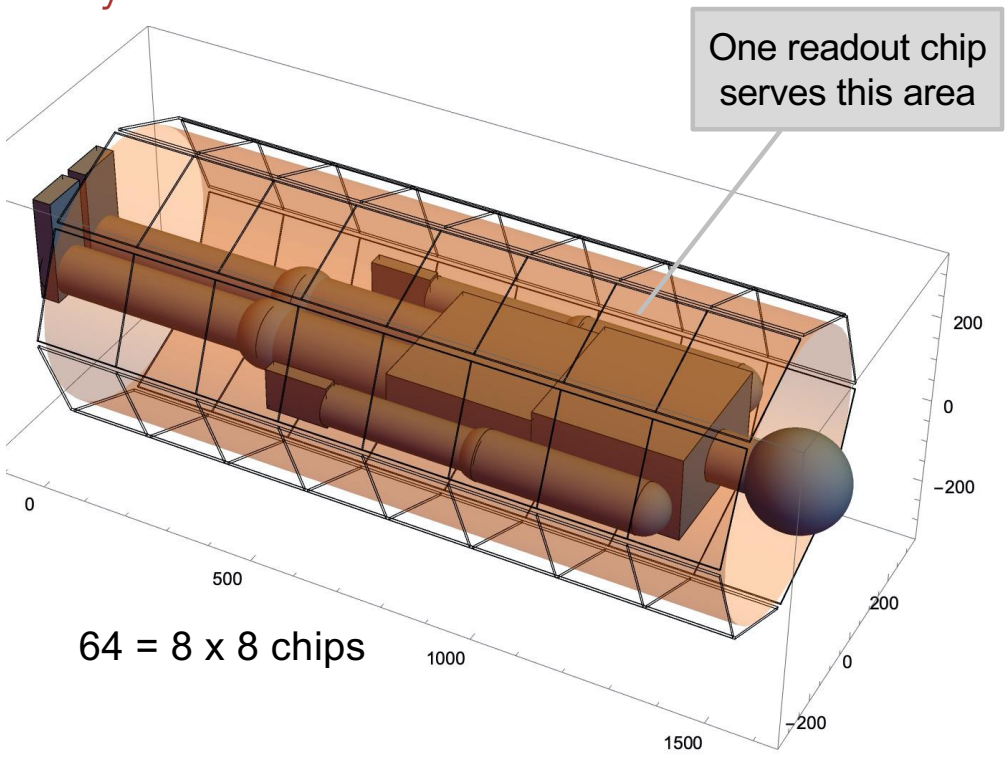
– Scanner R_I = 30 cm, L_Z = 150cm. Varying # of 'crystals' and readout chips
– *Very* simple 'PET': No absorption, scatter,... Time resolution is 'perfect' to ease reconstruction with ToF
– **Fully** simulated digitally (i.e. cycle accurate) all (up to 1024!) chips
– Study output data. Reconstruct Image for consistency check

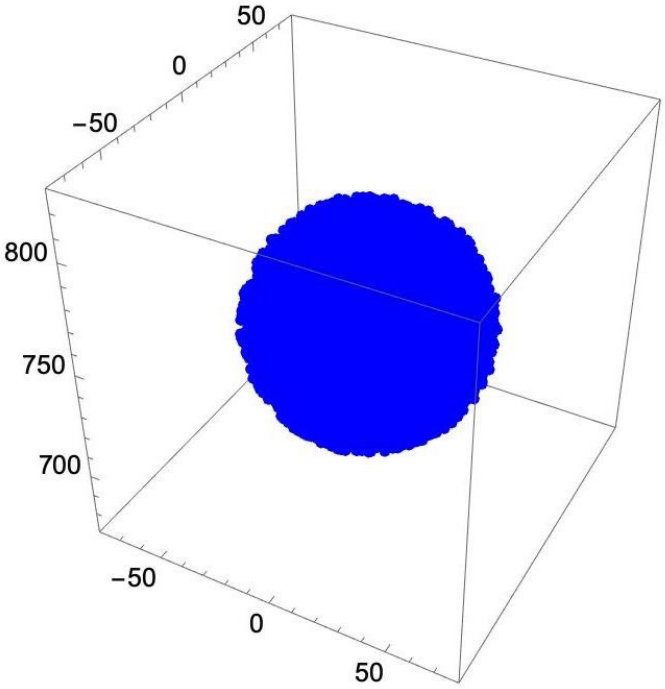


- 1024 = 32 x 32 chips
- 32768 'crystals'
- (dϕ,dZ) ~ (7,11) mm

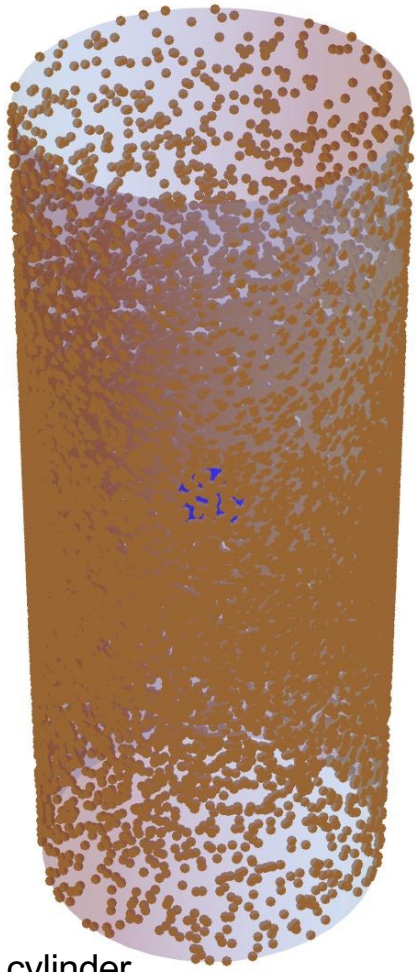


64 = 8 x 8 chips

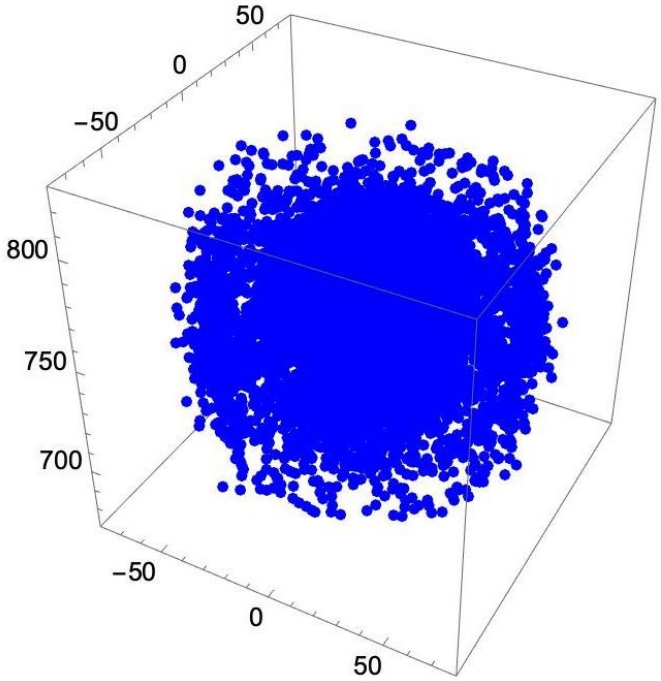
Source, Decays, Hits, Reconstruction



Generated decays:
Homogeneous sphere of R=15 cm



Hits on PET cylinder



Reconstruction
- Hit position degraded by crystal size
- ToF with ‘perfect’ time resolution

Chip Connection Topologies

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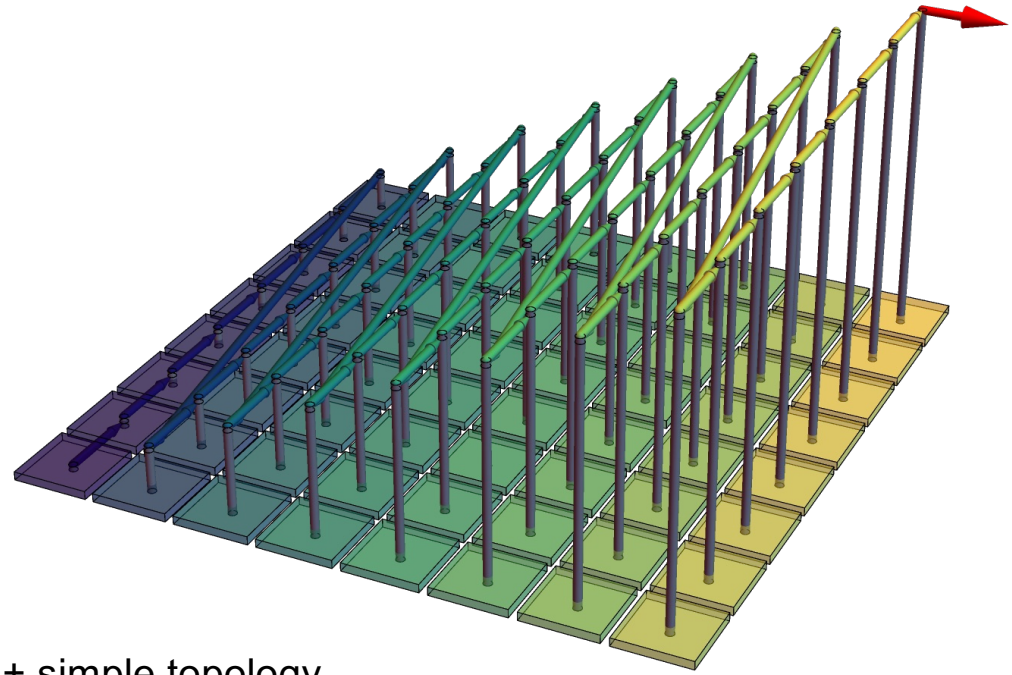
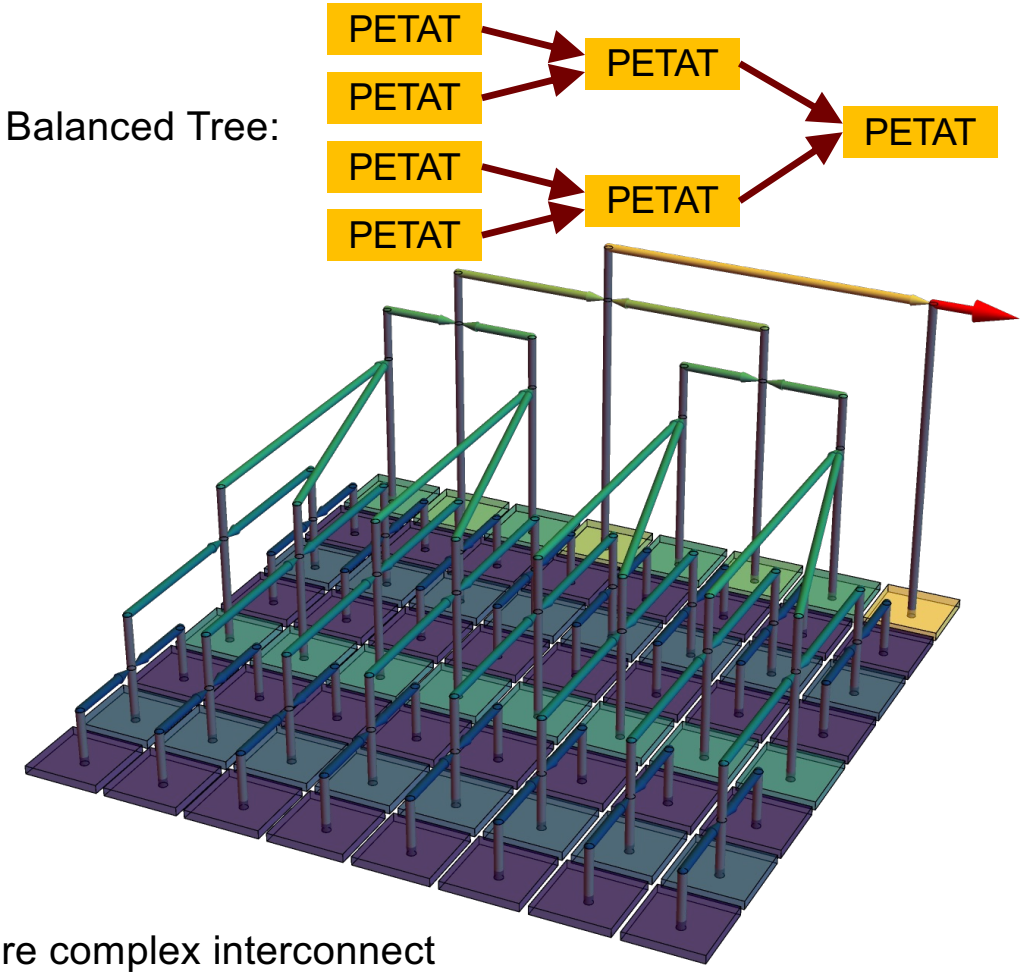
Linear chain: PETAT → PETAT → PETAT →



+ simple topology
- Hits in last chips must wait long -> buffer load

Balanced Tree:



- More complex interconnect

Expected and Simulated Maximum Data Rate

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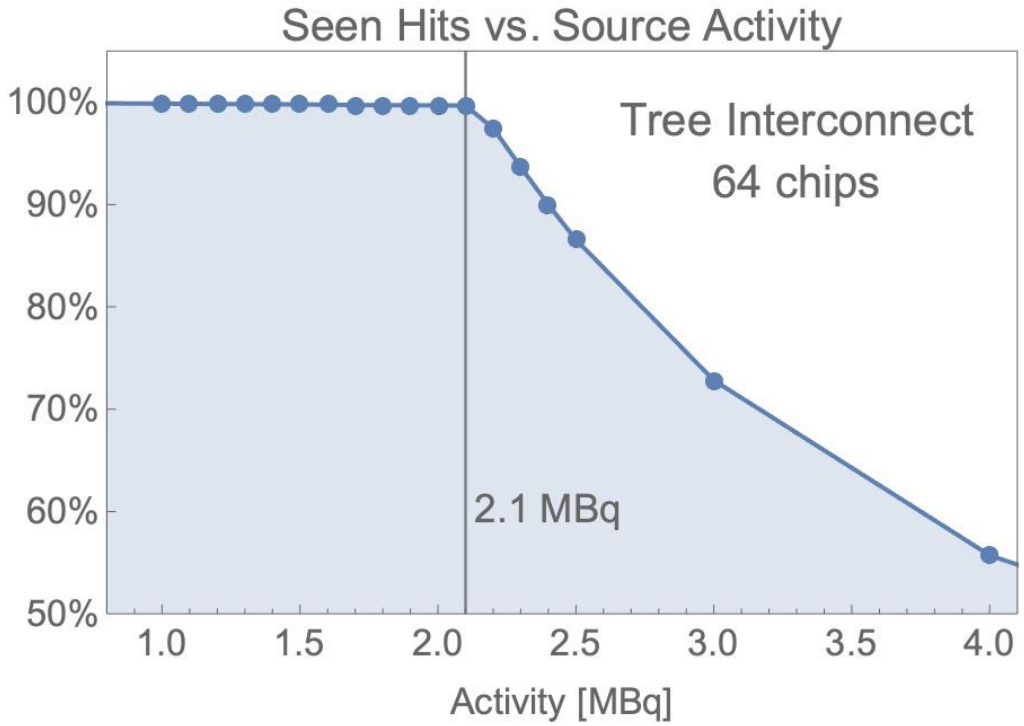
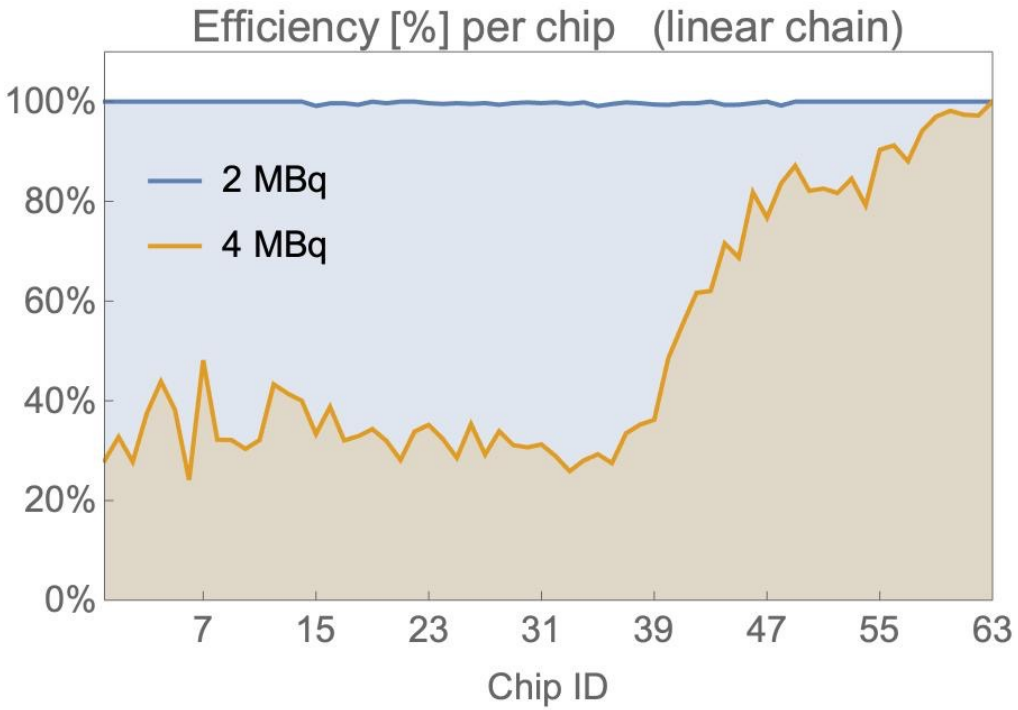
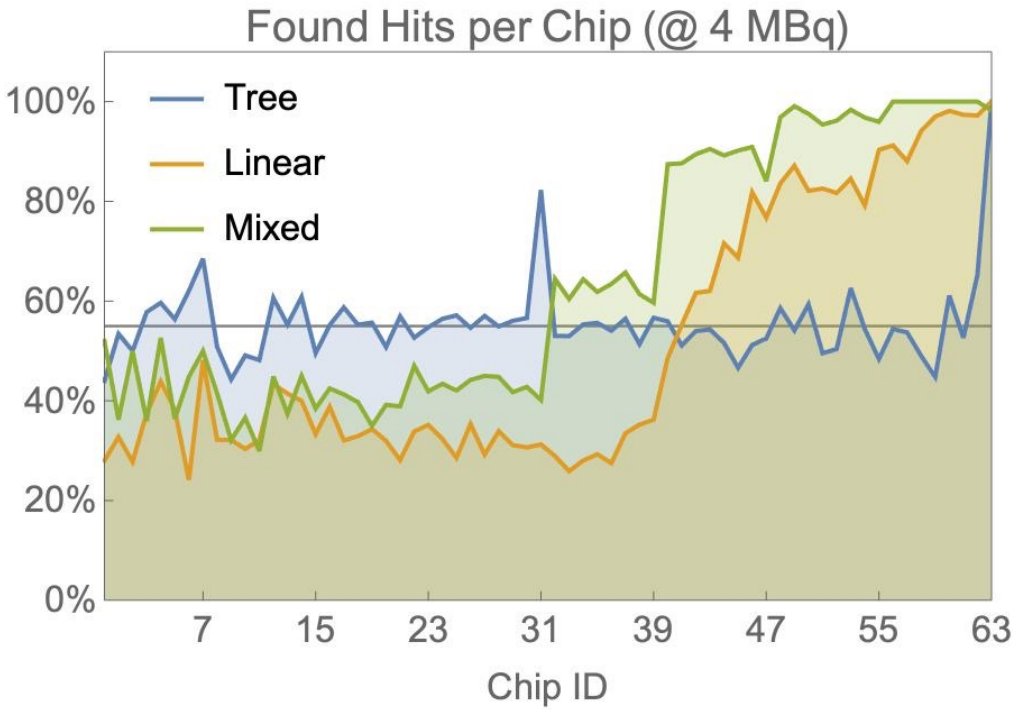
– At our present clock of 312.5 MHz and 80 bit events (incl. 8B10B), the link limit is 3.9 Mevents/s
– This corresponds to a source activity of ~2.1 MBq (losses at cylinder ends, no absorption. No sharing!)



– Architecture is ***FULLY efficient*** up to the max. rate! No 'safety margin' needed! 😀

Study of Data Losses





- Image shows data loss *in each chip* for 'just acceptable' and '2 x too high' hit rates for linear chain

- Differences between topologies are clearly visible in *overload* condition:
- Losses in 'Tree' are still very balanced

Final FPGA Processing

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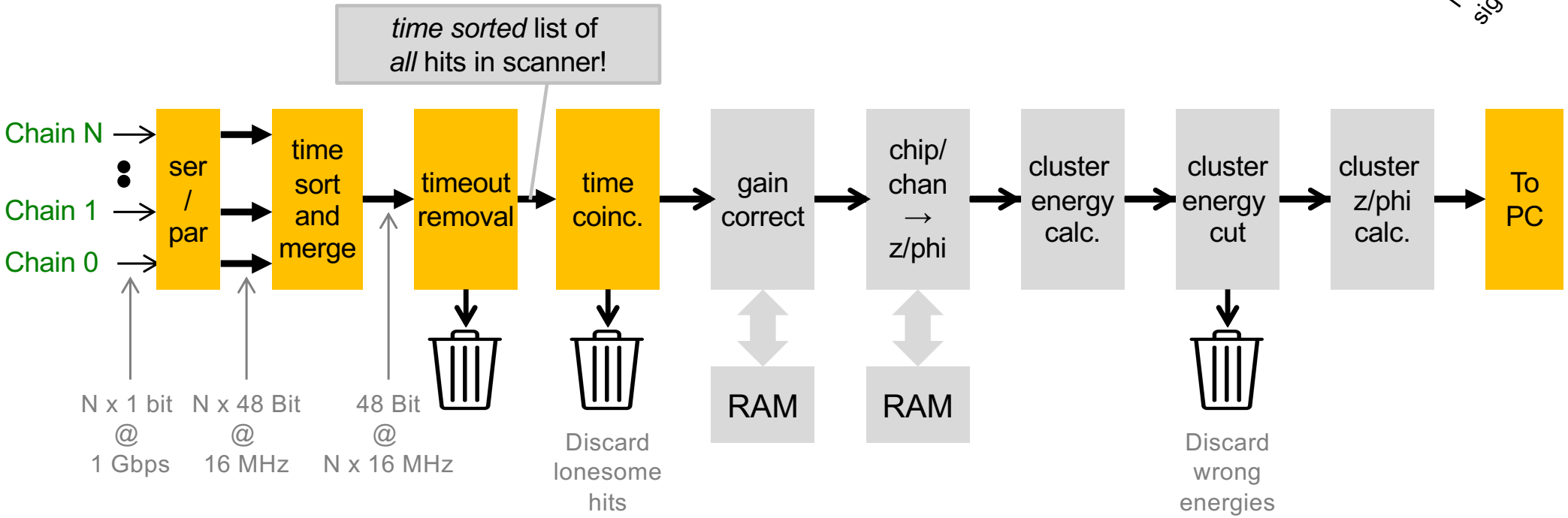
– Achievable rate per chain is ~16 MHits/s (@ ~1 GHz transport, 8B10B, 48 Bit / Hit) → ≳ 8 MBq
– For higher activities, must use several chains. For N=32 chains, can read ***≳260 MBq***
– The N serial chains can be combined in **ONE** final FPGA per SCANNER:

No absorption, signal sharing...



– FPGA preprocessing reduces data volume to PC to a minimum!

Summary, Next Steps

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- We propose a ***hierarchical data collection*** for PET Data
  →No FPGA close to R/O ASICs, minimal # components, reduced power, compact design

- This allows ***on-the-fly time-sorting*** of PET events. 'Final' data merging requires only one global FPGA
  → Real time hit processing and data reduction, immediate rejection of singles, energy cuts, ….

- We have designed, fabricated and successfully tested a first ***prototype chip PETAT1***

- We have set up a ***cycle-accurate sim.*** of >1000 chips to study data losses vs. topology, FIFO sizes, …
- We have combined this with a first very simple PET Monte Carlo to demonstrate feasibility

- Next Steps
  - Hardware test of multiple chips , more realistic PET sim., design improvements, new chip with latest SiPM FE
  - Build a 'demo' scanner ?

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Thank you for your attention