SVD Status

(+ richieste SVD-Pisa,
monitor&radiation systems + richieste SVD-Trieste nel talk di L. Vitale)

S.Bettarini per il gruppo SVD

Meeting con i referees: 8/9/2021

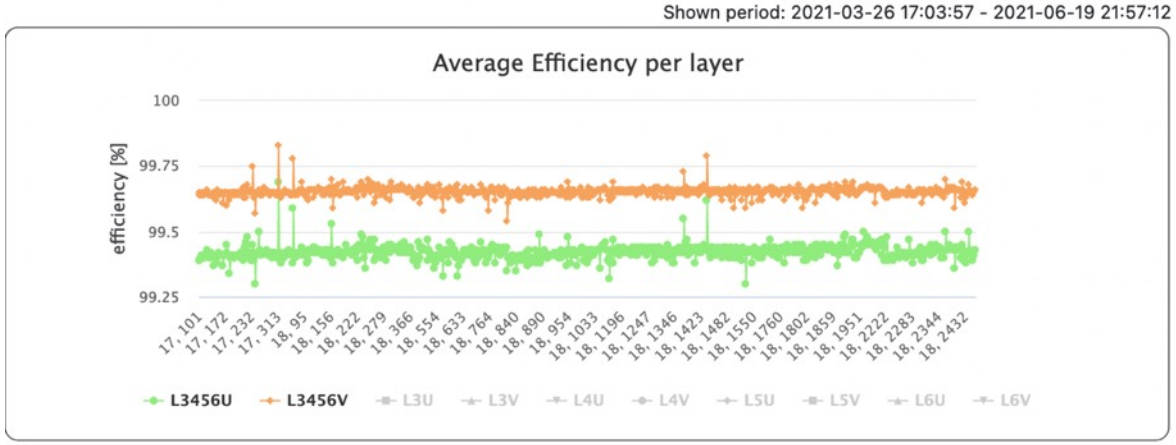
Outline

- SVD Status:
  - Operation & shifts
  - Performance: SNR, position and hit-time resolution (see backup slides)
  - Detector studies: BKG projection, radiation damage,
    offline SW improvements (see backup slides)
- Shutdown 2022
- Activities related to the VTX upgrade: CDR in 2022
  - 5 barrel layers: all-pixel VTX design
  - Mechanics: low-mass ladder R&D – support structure and cold-plate
  - Cu-flex circuits prototypes (X_0 improvement for Al-flex)

- Riepilogo richieste SVD-Pisa

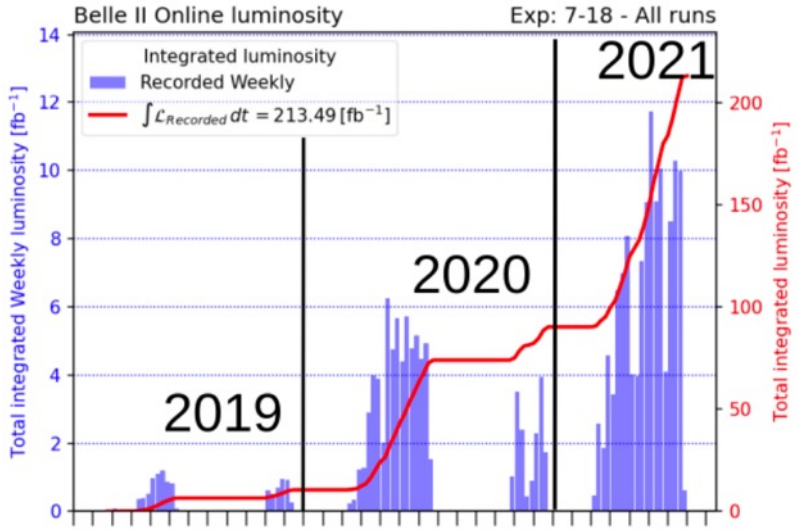
SVD Operation

- Operation in 2021 very smooth & data quality good
  - High & stable efficiency > 99% , no downtime, no BAD runs
  - Avg BG occupancy ~0.5 % (well below the limits of 3-5%) with some occasional high spikes not affecting performance.
  - Several beam abort with huge dose: PS errors and APV25 chip misconfigured but NO permanent damage in SVD (DCU channel damaged during QCS quench).



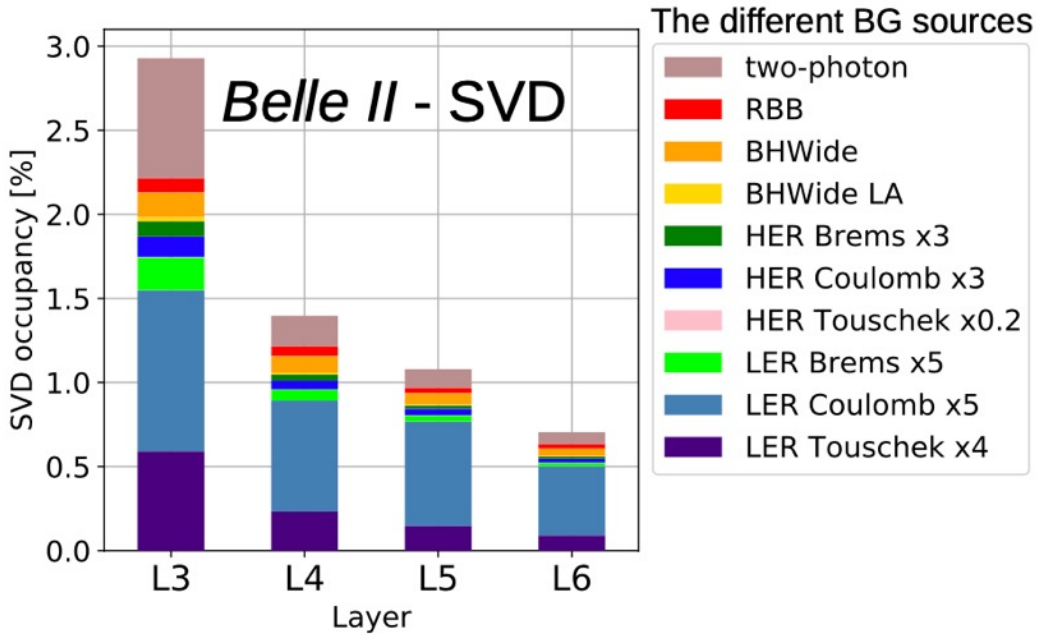
- Online SW very stable, regular maintenance & improvements + preparation for future
  - VLHI SW rewritten, for better future maintainability: long term tests in Belle II (e-hut) in Aug-Sept
  - VXD: RAD SW new features implemented for simpler & safer operation
  - Starting to think on further automatization of local run, in future to be taken by CR shifter during occasional no beam

- Operation Coordinators & shifts
  - SVD Operation Coordinator + SVD expert shifts (remote/local) with 24/7 coverage as in 2020 runs
  - R(remote)OC: after 3 months of short (3 weeks) shifts done by experts, for future runs organized again with 3 months coverage:
    - Y. Uematsu (U. Tokyo) SVD for 2021a
    - K. Lautenbach (Marseille) Remote for 2021c
    - K. Kang (in IPMU from Sep) for end of 2021c and 2022a.
  - As soon as the COVID-19 restrictions are removed go back to the shift system based on experts on site.



SVD background extrapolation

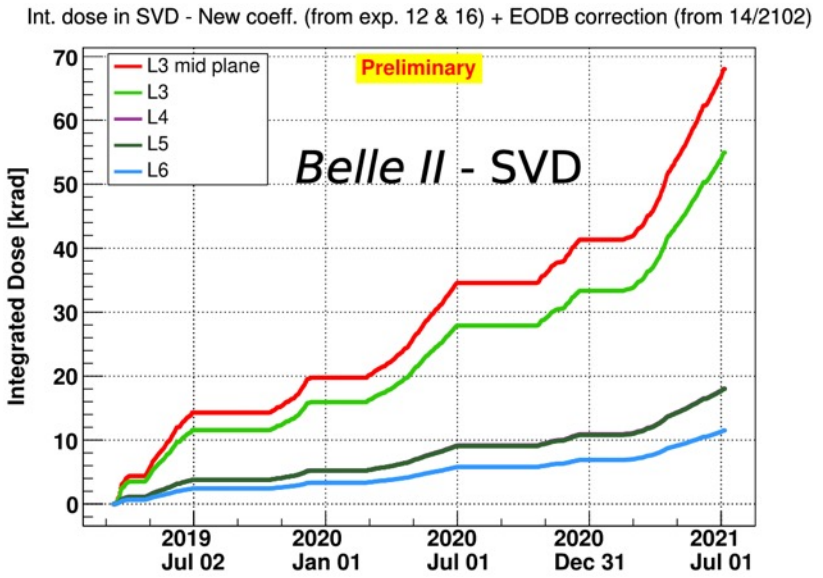
- Beam background increases SVD hit occupancy which degrades tracking performance.
- With current luminosity average hit occupancy in layer-3 is well under control (< 0.5%)
- SVD BG analysis with latest MC campaign:
  - Scaling factors DATA/MC from maximum found in BG studies for May/Jun/Dec 2020 (still preliminary)
- Extrapolation (L=8 10^{35} cm^{-2} s^{-1}) for Layer3 occupancy now ~3% BUT there are large uncertainties:
  - MC assumes optimal collimator settings, maybe not possible in real operation (occu higher)
  - no injection BG (occu higher)
  - lower beam pipe pressure (occu lower)
- Current SVD limit for good tracking is ~3%. It will be up to ~5% (TBC) when we will apply BG rejection with hit time.



SVD Dose analysis & radiation damage effects

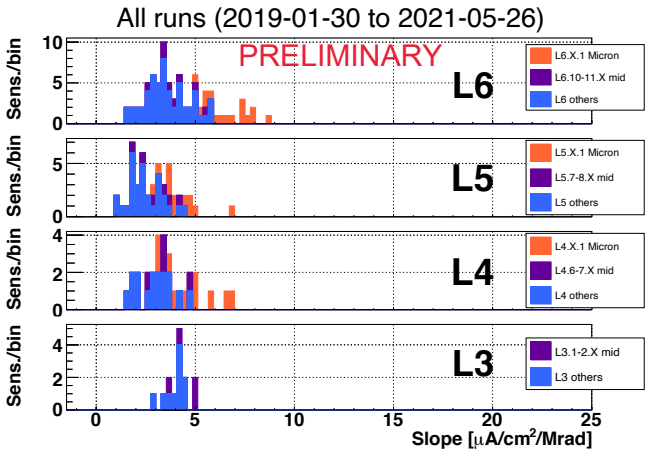
SVD dose

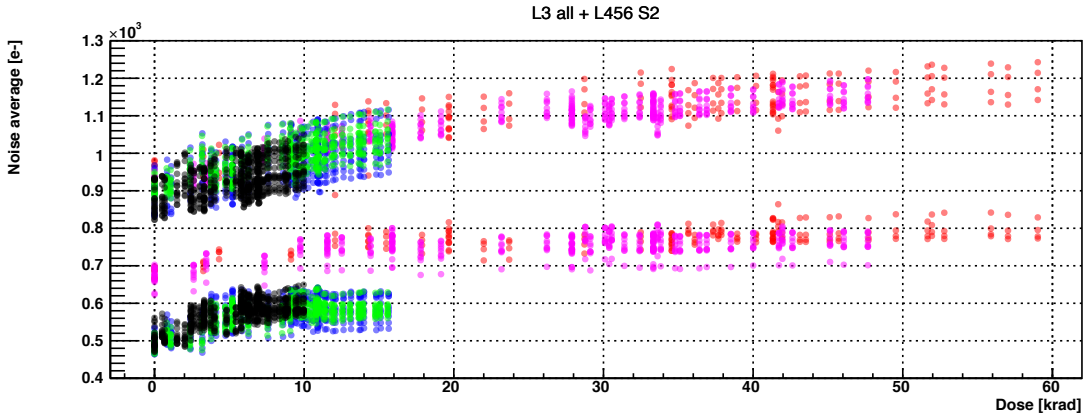
- Updated SVD dose analysis
  - 60 krad in layer-3 mid plane (the most exposed to radiation)
  - 1-MeV equivalent neutron fluence: ~1.6 ˆ 10^{11} n_{eq}/cm^2 in first 2.5 years (assuming dose/n_{eq} fluence ratio = 2.3 ˆ 10^9 $n_{eq}/cm^2/krad$ from MC)
  - Dose estimate based on correlation between SVD occupancy and diamonds dose
  - Now use new poisson trigger data w/o inj veto
  - Still some large uncertainties (50%?)



- Analysis of the rad damage effects in all sensors up to 2021ab rur
  - not affecting performance
  - Sensor current increase linearly with dose (as expected), consistent in all sensors & in reasonable agreement with expectation
    - 2-5 uA/cm2/Mrad with large variation due to temperature effects and dose spread among sensors in layer (avg layer dose considered except for L3)
  - Noise increase 10-25% observed, not linear as expected, due to increase in sensor interstrip capacitance for higher fixed oxide change from irradiation → saturated on n side and start to saturate on p side too.

Sensor current slope with dose (up to June 2021)



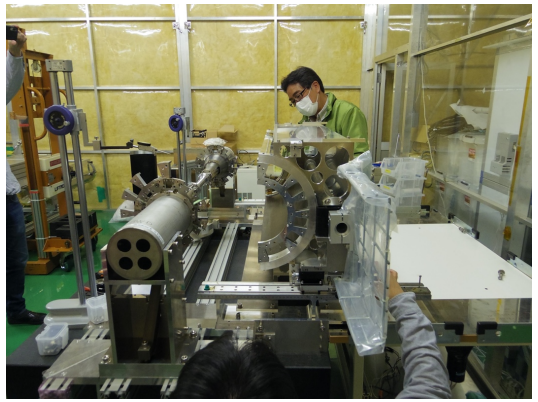


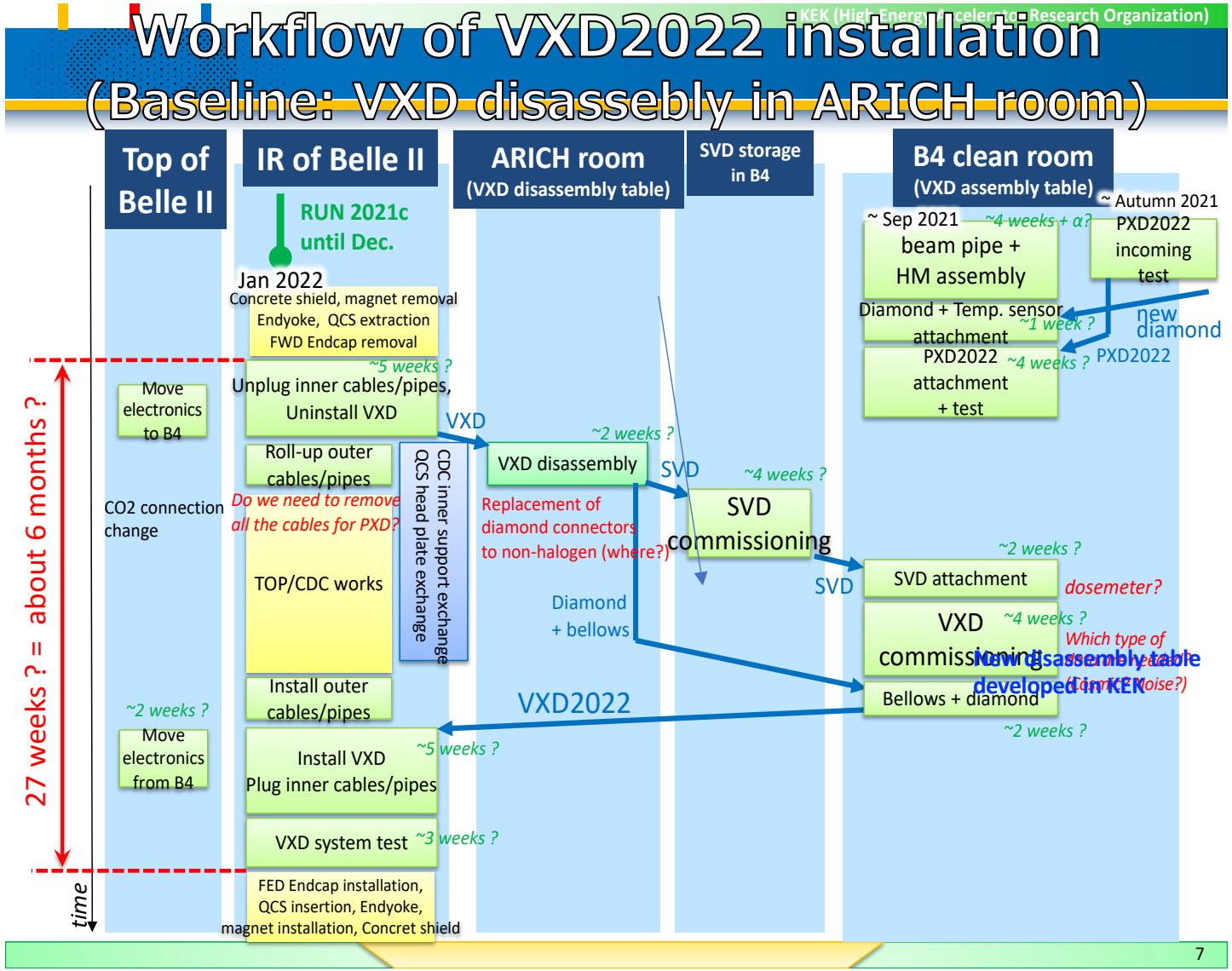
Noise vs Dose (up to June 2021)

VXD 2022 preparation activities

- VXD2022 installation group formed
  - huge effort for the entire SVD group: not only "historical" experts but involvement of also new/fresh manpower, crucial for next steps.
- T_0 shifted from Jan. to July 2022.
- Detailed schedule with time estimates and manpower for all the steps prepared:
  - Based on first VXD installation + changes for additional complexity (VXD disassembly...)
- 1st Review of the entire VXD2022 effort done on md Feb.

SVD has to be detached safely on this table





Shutdown 2022: Activities & Request (from Pisa)

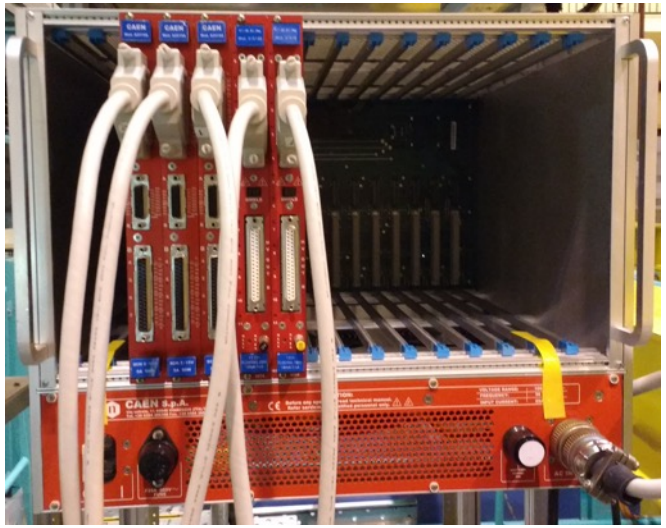
- SVD un-cabling & re-cabling (as done for the installation):
  - 2 (times) x [2 A.T. technicians x 2 weeks]
  - 2 (times) Mech. Eng. X 10 gg for learning the procedures and present for the crucial operations (to be able to make the same for the upgraded VTX detector)
  - 1 (Expert-physicist) to coordinate

Tot. 6 m.u. @ KEK

To be added to (hyp.:“normal” SVD operation in 2022):
SVD local shift [Jan., June] under normal running (i.e. no covid-19 restrictions):
[4.5 months (running) + 2 x 0.5 month (preparation/end)] x Pisa SVD fraction ~ 1 m.u.

Richiesta SVD: apparati 8.5 kE
(relativo al sistema Power Supply)

- 1 Crate + gruppo PDP spare (controller, LV and HV boards)
- Abbiamo un solo "spare”, in realtà è necessario per il test-stand in B1.
- Avere test-stand in B1 operativo è molto importante: ad esempio è utilizzato per il test delle PS boards, tornate a KEK dopo la riparazione, prima della sostituzione in esperimento di eventuali board che manifestano problemi.
- Durante il running abbiamo avuto un failure del controller del PDP nel sistema installato in esperimento e quindi abbiamo runnato per diversi mesi senza spare e senza la possibilità di utilizzare il test-stand.
- Il controller riparato è tornato a KEK poco prima della fine del run e quindi non abbiamo avuto la possibilita’ di testare con il fascio una PS board modificata (dalla CAEN) con una importante miglioria del monitoring in corrente.
- Dopo le PS boards spare che abbiamo comprato anni fa, questa richiesta ci mette al sicuro con un numero di spare ragionevole per OGNI parte del sistema dei power supply.
- L’offerta riguarda meteriale inserito nell'accordo quadro infn.
- Prezzo finale (allineato con l’ordine iniziale del sistema PS) con consegna a KEK (merce sdoganata).



SY4527

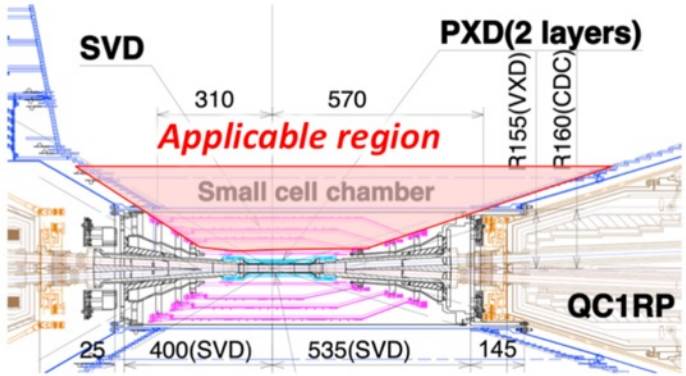
PDP

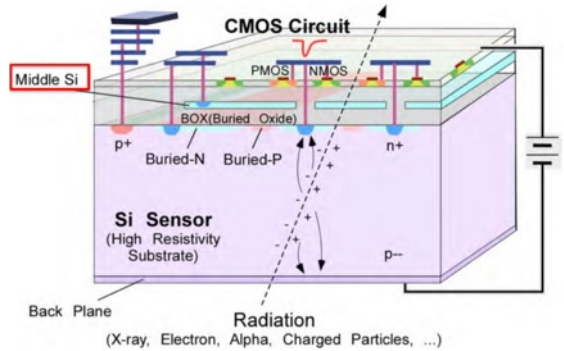
Upgrade del rivelatore di vertice di Belle II

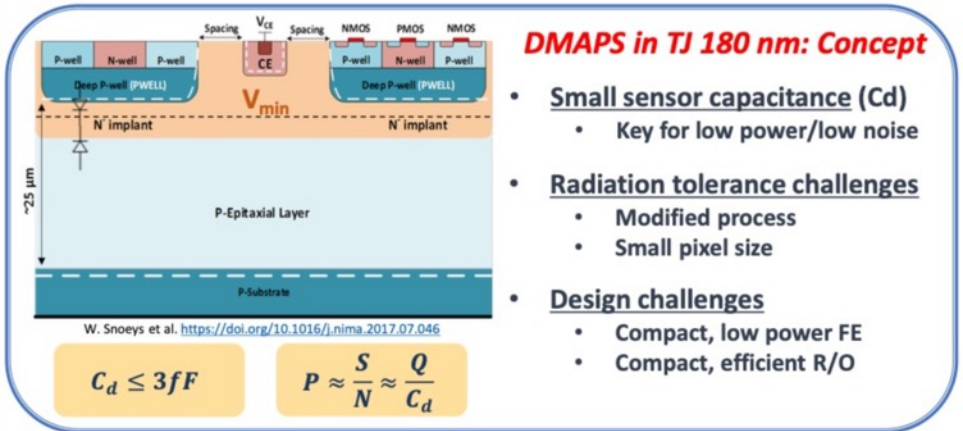
- Scenario con molte incertezze sulle possibili “opzioni” dell’upgrade di SKB. Ipotesi di lavoro: flessibilità sulla timescale (>= 2026).

  CDR nel 2022.

- Molteplici soluzioni tecnologiche per VXD, ciascuna con un chiaro piano di sviluppo/test per il sensore:
  - Thin-fine pitch DSSD detector (TFP):
    - Applicabile solo alla regione esterna (raggio>L3)
    - Hi-Ω (Micron) Sensor + front end ASICS SNAP128A
    - Test sensor+r.o. chip nel 2022: S/N marginale?
  - DuTip-SOI: 7-layer Vertex detector replacing PXD+SVD
    - Dual Timer Pixel basato su FD-SOI CMOS technology (Lapis semiconductor)
    - Superate le due principali difficoltà della tecnologia:
      - back-gate effect
      - radiation tolerance.
  - DEPFET: soluzione “adiabatica” (NO R&D)
    - “stessi” L1&2 a pixel con gli stessi problemi in caso di burst di radiazione
  - VTX DMAPS: Depleted MAPS in tecnologia 180 nm Tower-Jazz
    - Linea di sviluppo per ATLAS-itk: famiglia TJ-Monopix

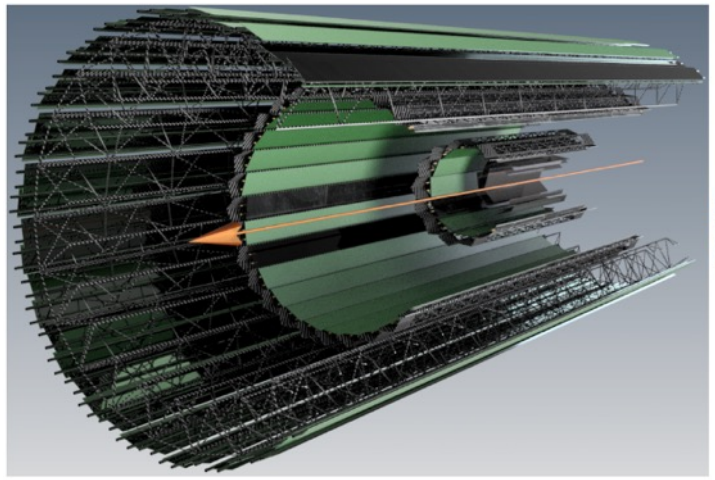


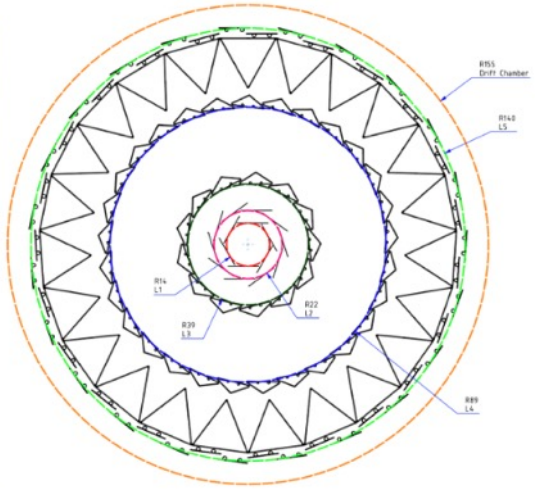




VTX baseline concept:

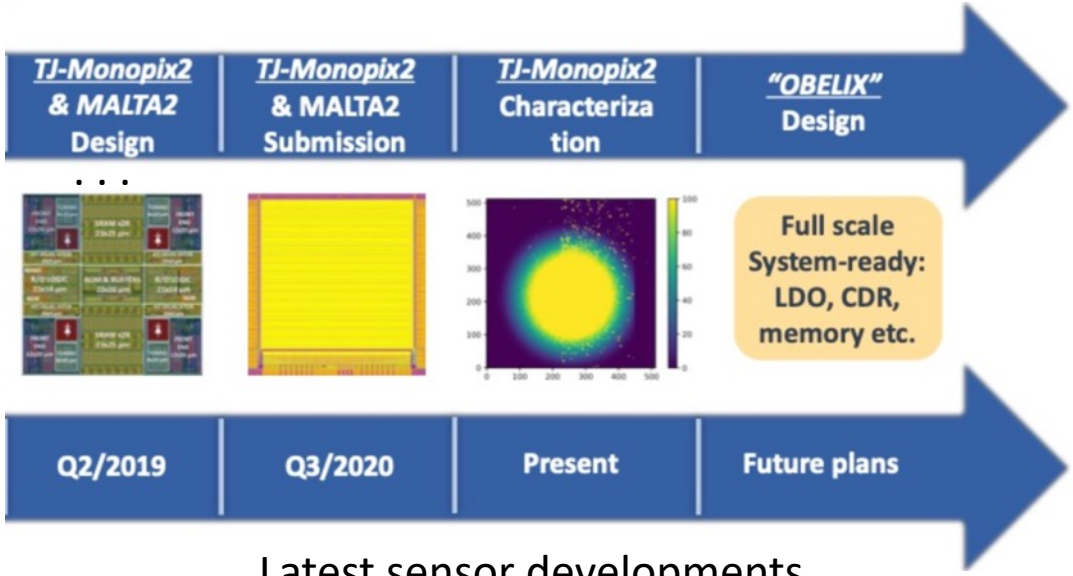
- Low material (~50 µm thin sensors) :
  0.1% X0 (L1+L2) - 0.3% (L3) - 0.8% X0 (L4+L5)
- Moderate pixel pitch~40 µm^2
- Fast integration time: 25-100ns
- Operation simplicity and reduced services
- One chip design for all layers, but different integration between inner (L1+L2) and outer (L3, L4+L5)





5-layer VTX Conceptual Design

TJ-Monopix2 chip: proof of principle of prototype sensor for Belle II VTX



Latest sensor developments

Funds for submission:
Austria - France
Germany
Italy - Spain

Activities organized in 3WPs

- VTX coordinator [C. Marinas (Valencia)]
- WG1: Software, performance, benchmarking [B. Schwenker (Goettingen)]
- WG2: Chip design, testing [J. Baudot (Strassbourg), T. Hemperek (Bonn)]
- WG3: System integration, services [S. Bettarini (Pisa)]

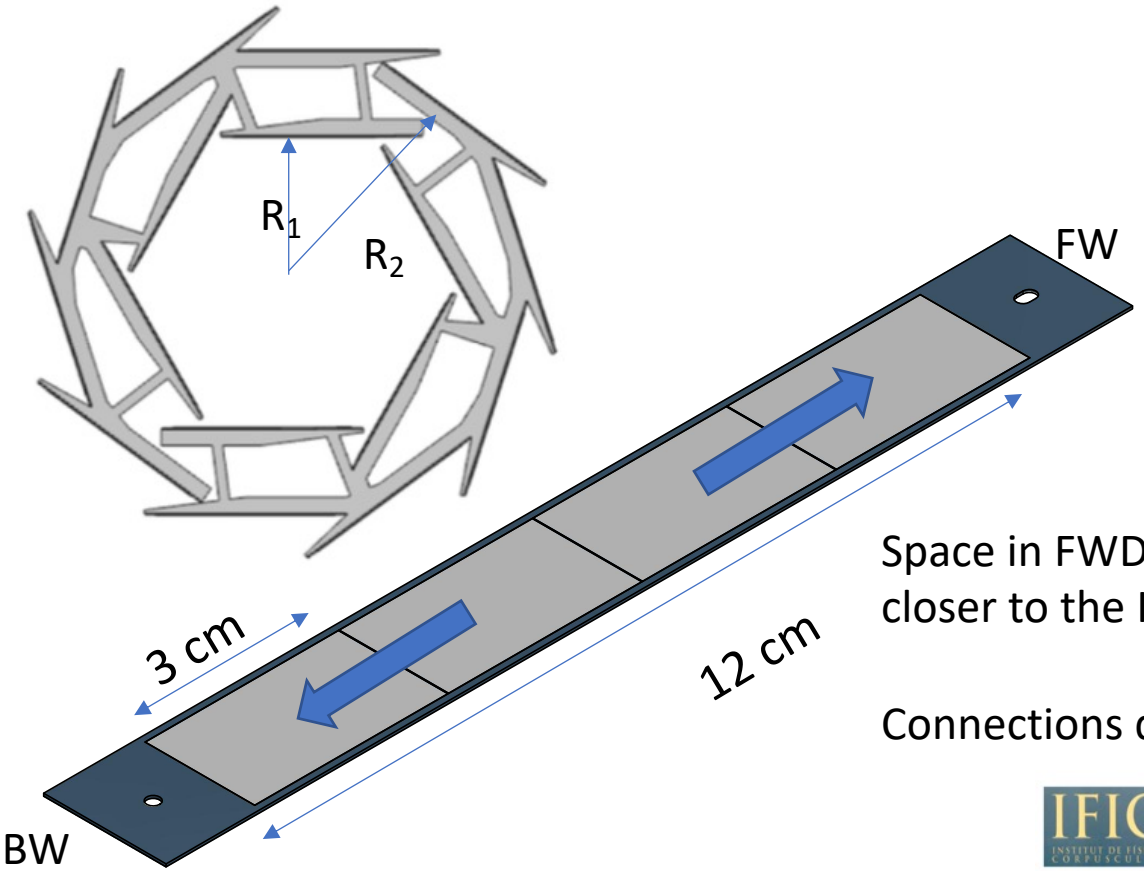
The plan is to submit the TJ-Monopix2 chip (already received) to extensive tests already this year:

- Threshold scans,threshold tuning, calibration on bench (done)
- 2 test-beams@DESY: Aug(done) & Nov. 2021 for:
  - Efficiency/Resolution measurements
- Radiation hardness (NIEL and TID irradiation campaigns)
- Test systems (DAQ) will be distributed to the VTX institutions.

R&D on iVTX ladder: all-silicon-ladder concept

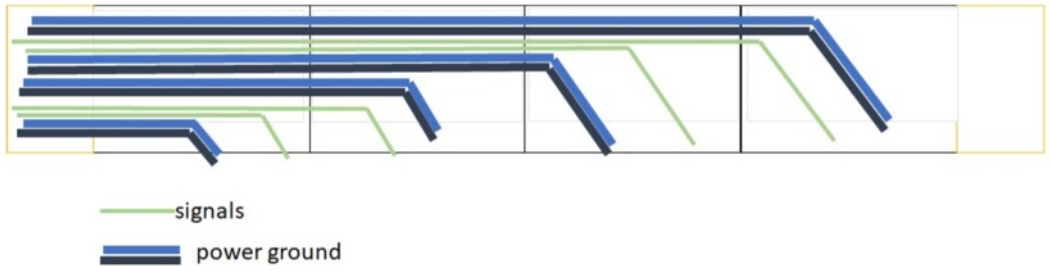
A single piece of silicon, with a slightly thicker silicon frame and a 40 μm-thin central region:

- L1 and L2 modules identical, placed at R_1=1.4 cm and R_2=2.2 cm
- 500 um active-area overlap
- Material budget: 0.1 % X_0/layer
- Cooling: forced air flow (V_{air}~m/s) for the acceptance region(to be simulated/experimentally demostrated!).



To reach the low-material-target: flex-less module.

Signal and Power Distribution

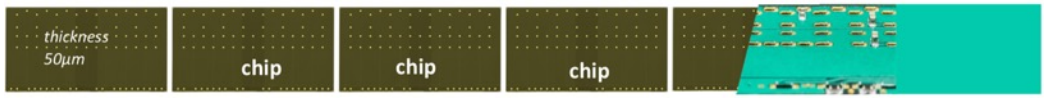


Space in FWD is tight and some machine upgrade options consider moving QCS closer to the IP: desirable to have services from BWD side only (for the inner layers)

Connections done at the bottom of the chip with vias between the chip and the RDL

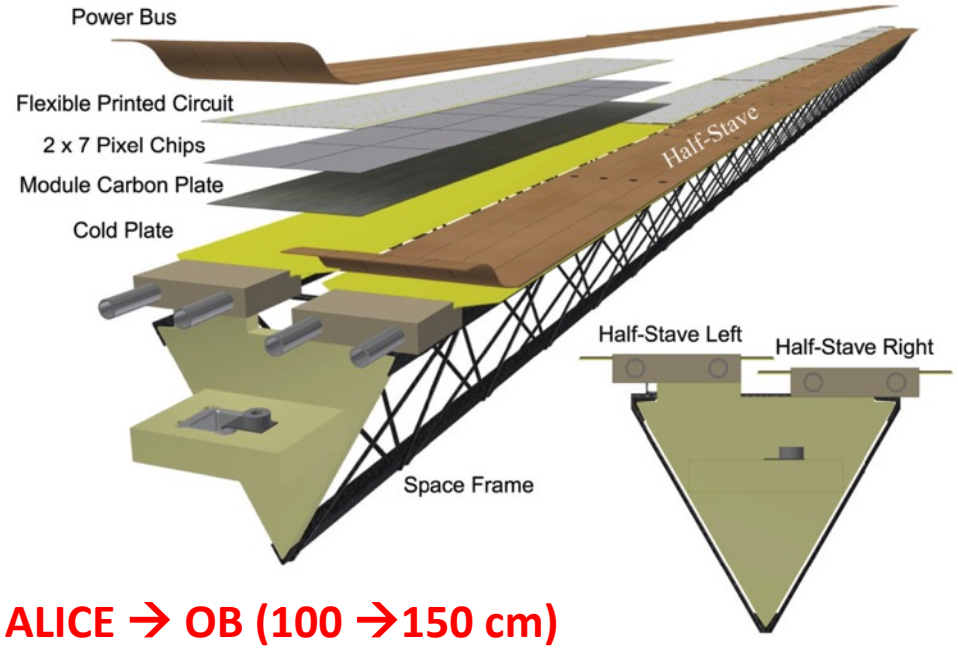
oVTX spec's

Power BUS



oVTX: L5

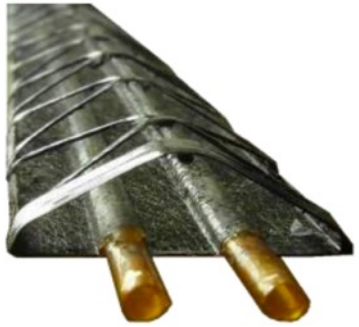
- Material budget: ~0.8 % X_0 /layer
- Staves «a la Alice» OB:→R = 14cm,Length=70cm
- Water cooled sensors
- Operation at room temperature
- Specific power consumption: ~ 200mW/cm^2
- Power BUS needed!



ALICE → OB (100 →150 cm)

oVTX: L4 and L3

- Material budget: 0.3 % X_0 /layer
- Staves «a la Alice» IB: R=3.9/9.0 Length=20/45 cm
- Barrel shaped
- Water cooled sensors
- Operation at room temperature
- Specific power consumption: ~ 200 mW/cm^2

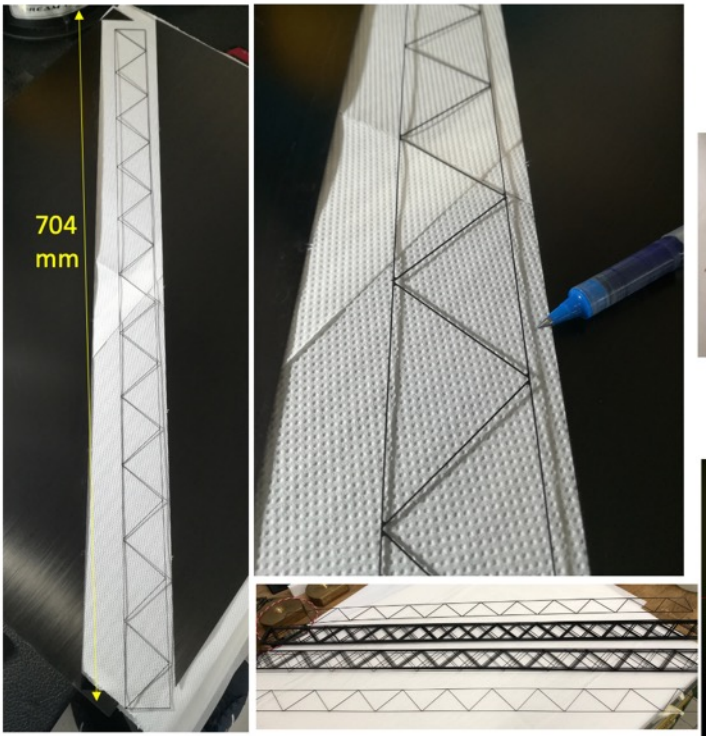


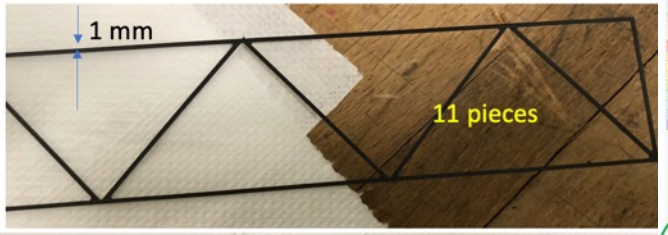
ALICE → IB (30 cm)

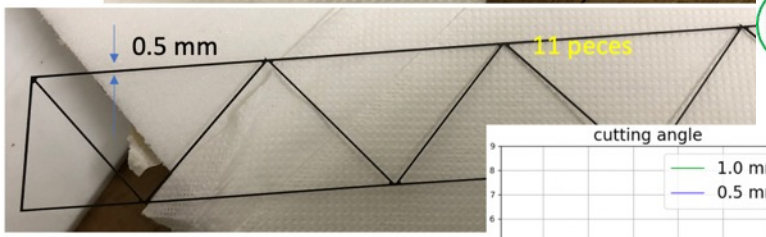
@INFN-Pisa: oVTX struttura meccanica con “Subtractive Method”

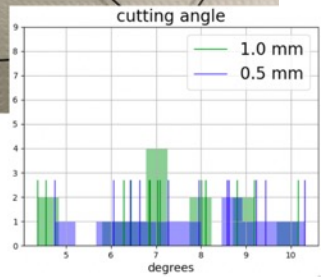
- Il più challenging (70 cm) L5 ladder: realizzare la struttura a traliccio incollando le 3 strutture planari ricavate con taglio a water-jet

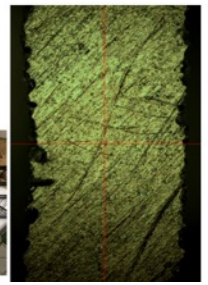
CF water-jet cut (by WatAJet Company)

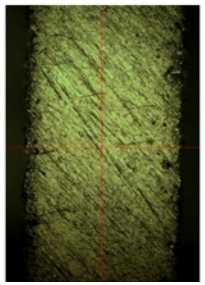


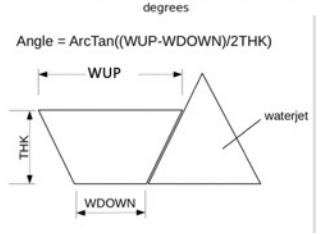






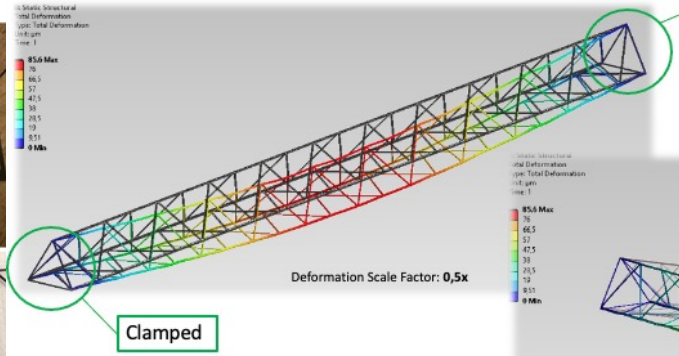




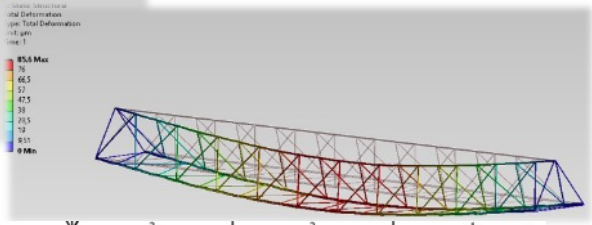


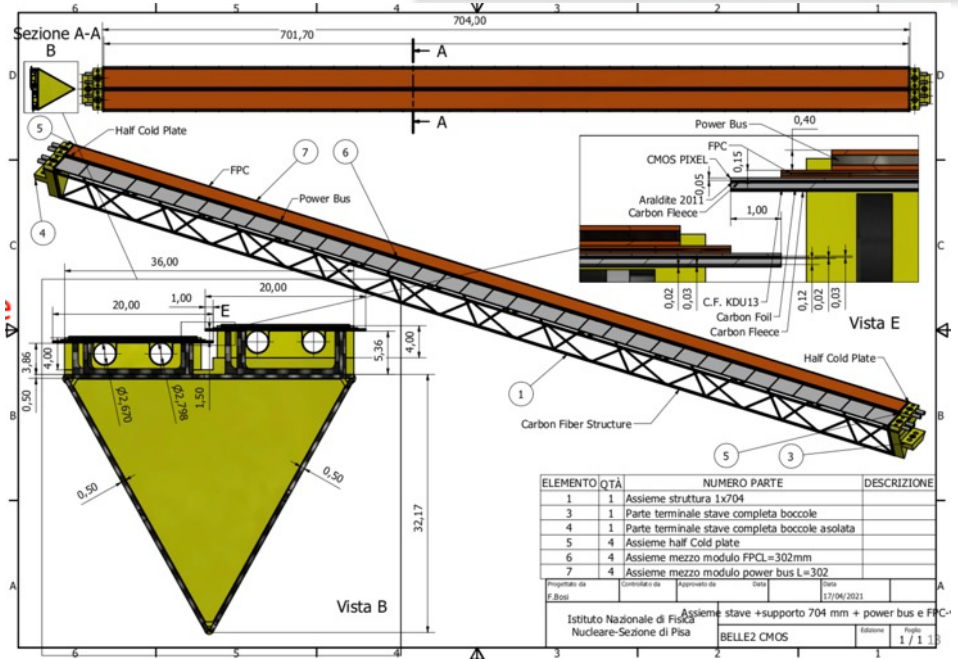
- The maximum sag of the structure is 85,6 µm

FEA



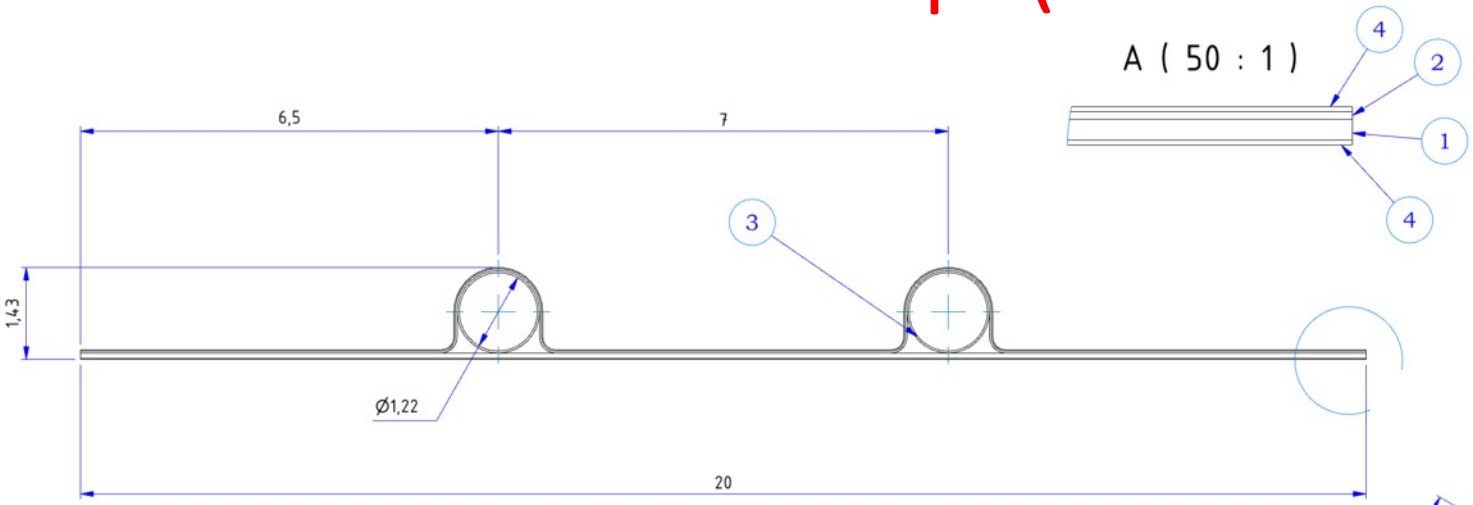
- The results are quite good, this kind of geometry could be a viable solution





Istituto Nazionale di Fisica Nucleare
Sezione di Pisa

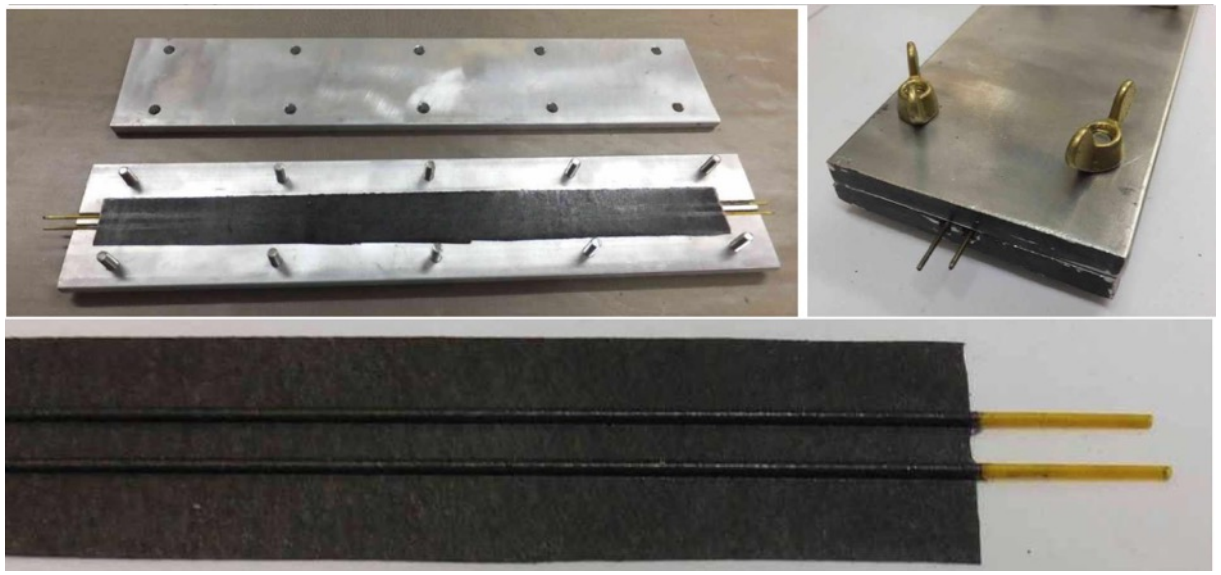
Cold Plate concept (the same for all L3,4 & 5 layers)



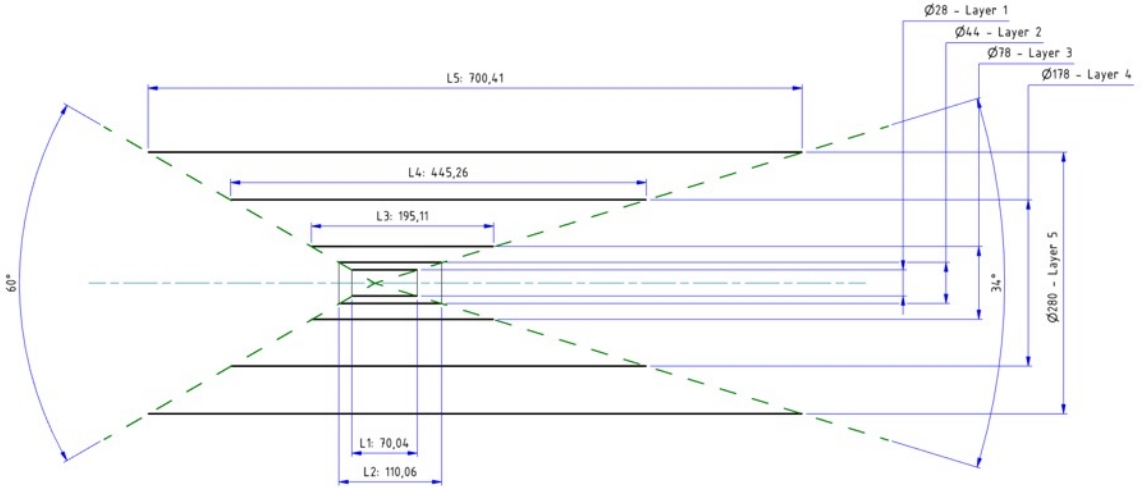
Item	Qty	Description	Thickness
4	2	Carbon fleece	~ 20 um
3	2	Polyimide tube	~ 32 um
2	1	Graphite foil	~ 30 um
1	1	High thermal conductivity CF - K13D2U	80 um

PART LIST

COLD PLATES	
Layer	Length
3	210.5 mm
4	450.9 mm



Reference Cones



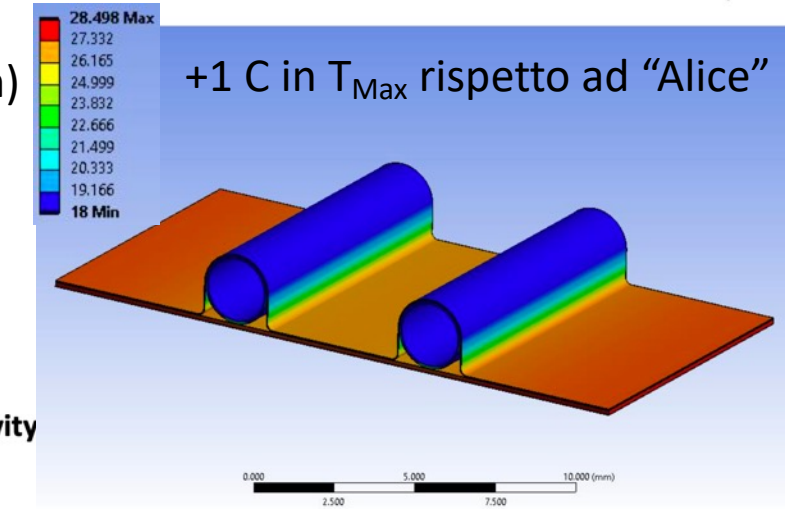
Already received the budgetary offer by

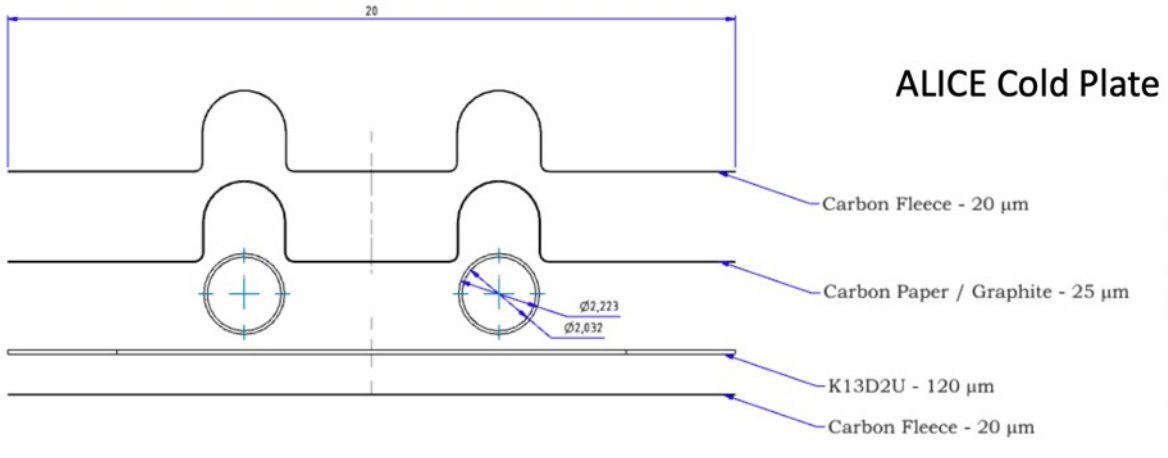
LOSON COMPOSITI

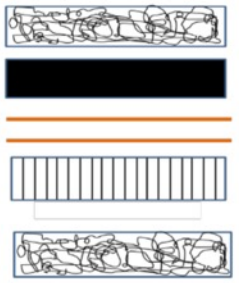
Modifica del design di “Alice” della cold-plate

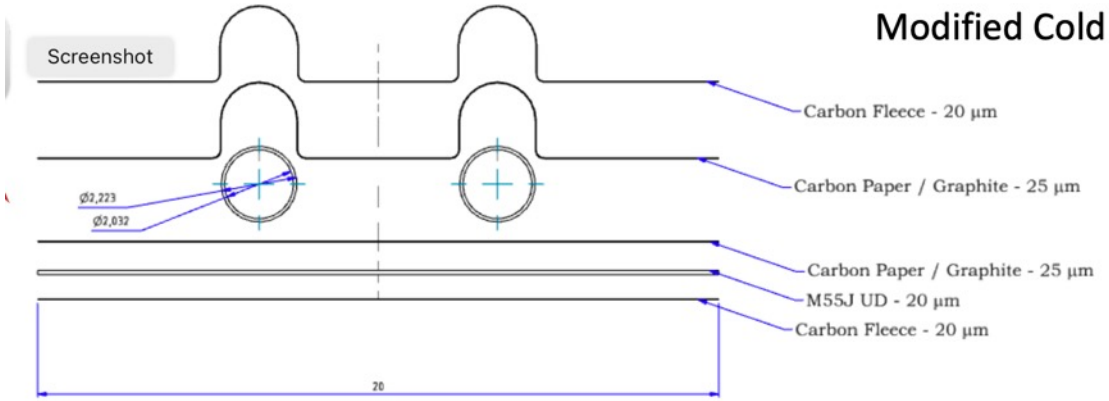
- Problemi di reperibilità di piccole quantità della fibra K13DU
- Modifica: introduzione della fibra M55J + aggiunto uno strato di Carbon-Paper (20 um)
- Material budget (cold-plate) : 0.066 % X_0→ 0.074% X_0

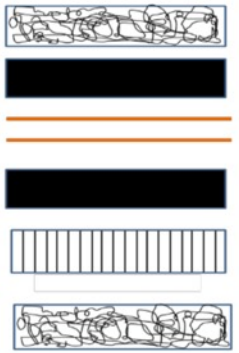
Modified Cold Plate – M55J+Carbon Paper







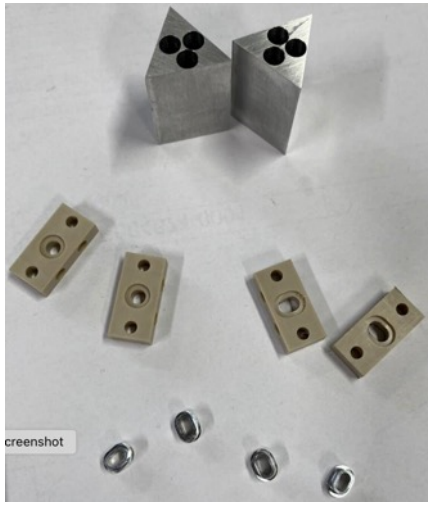




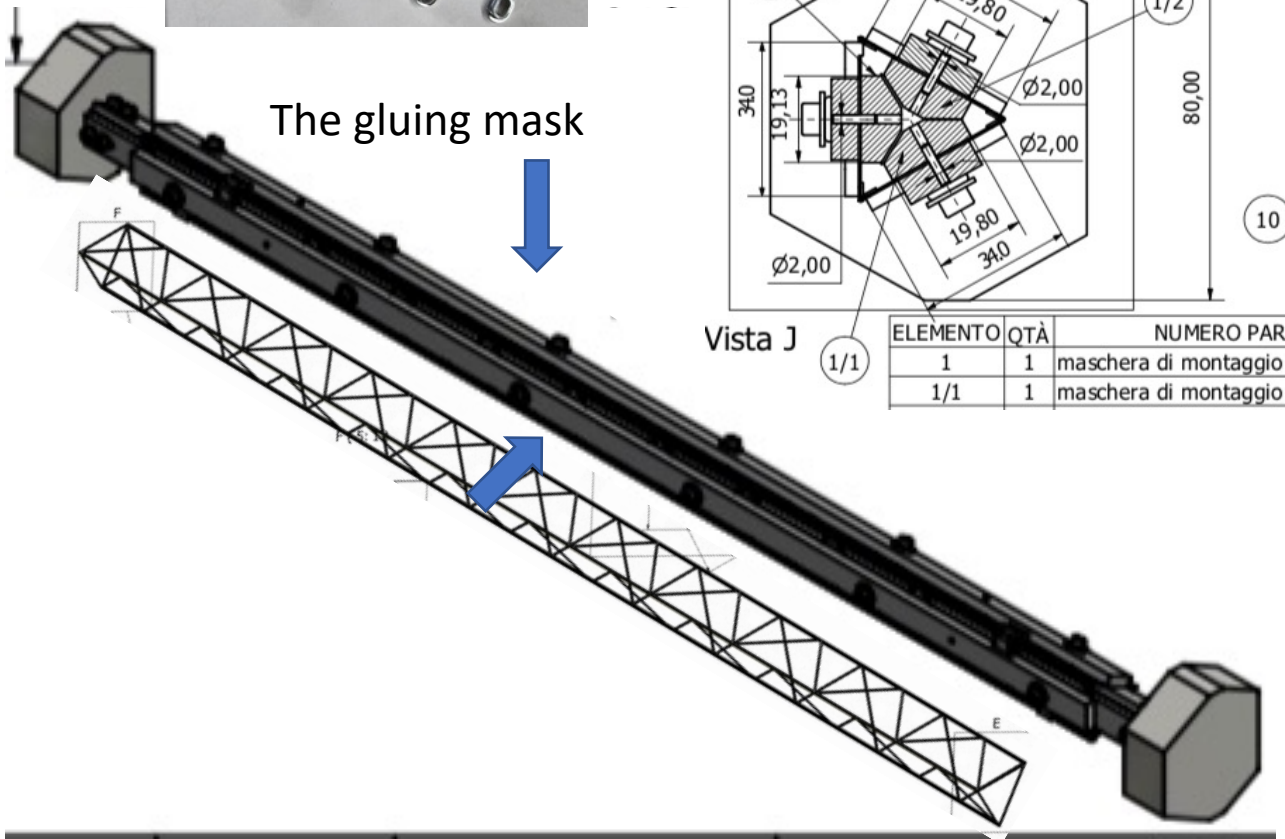
Thermal Conductivity (*W/mK*)

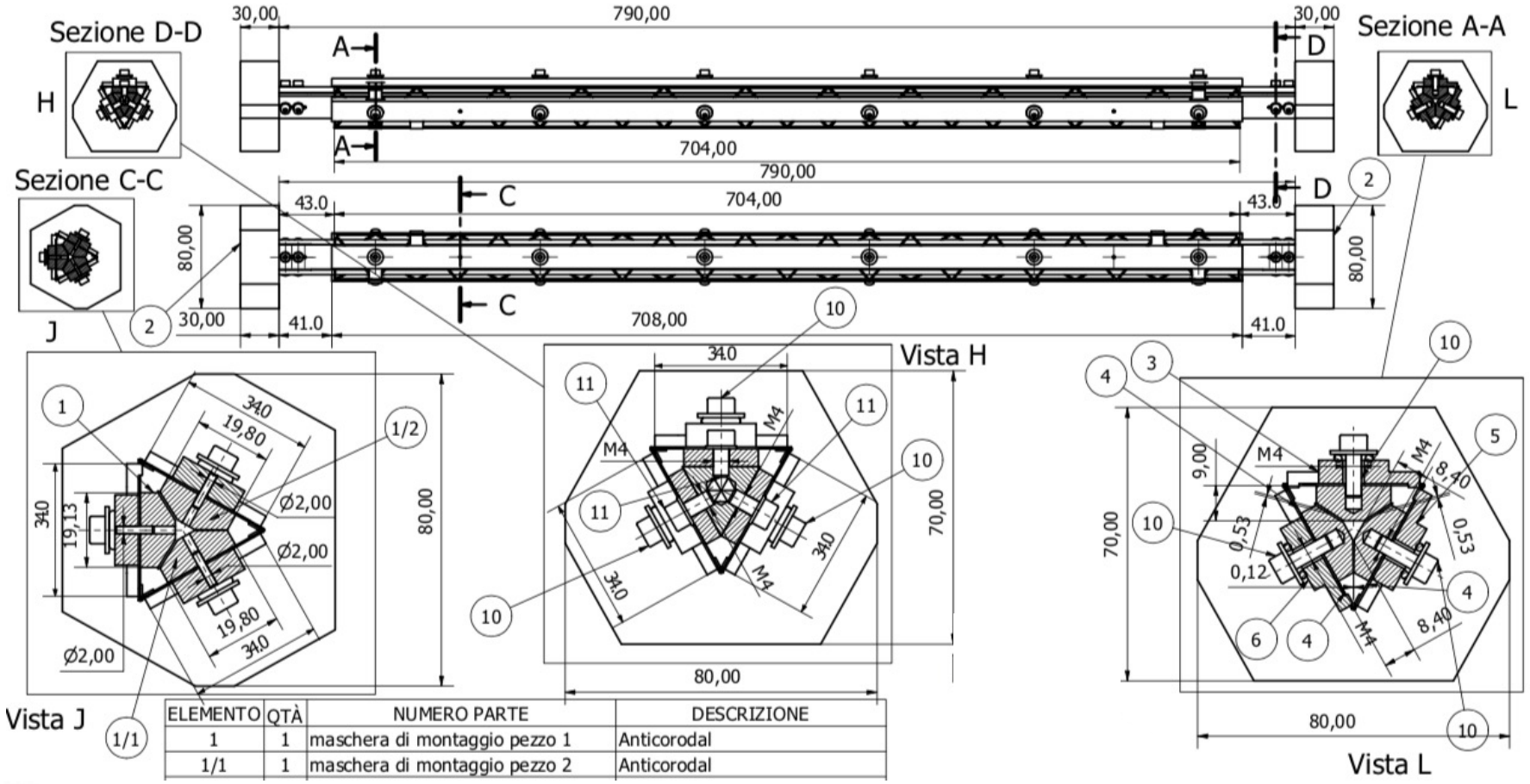
- **Carbon Fleece**: No Information – *Hypothesis*: 5 in plane – 1 out of plane
- **Carbon Paper**: From data sheet – 1600 in plane – 15 out of plane
- **K13D2U+EX1515**: measured values from Purdue University - 376 and 7.5 in plane – 1.4 out of plane
- **M55J+EX1515**: No Information – *Hypothesis*: 1 in plane – 0.2 out of plane
- **Polyimide pipes**: From Gargiulo’s talks – 0.2

Mask ready to be assembled@INFN-Pisa

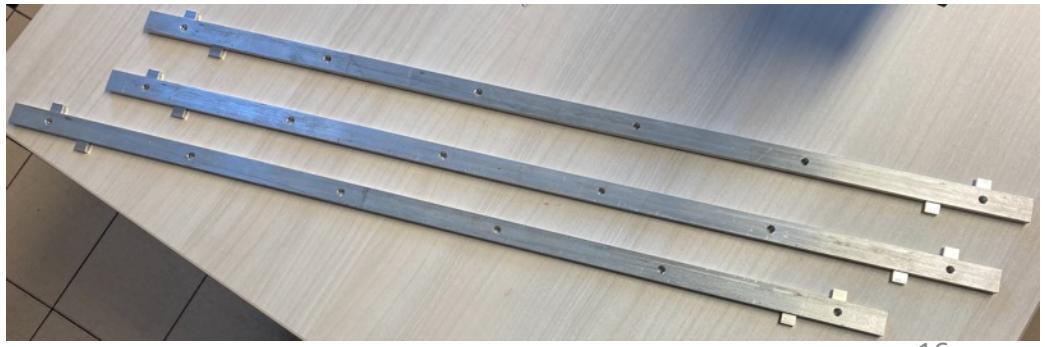


The gluing mask





ELEMENTO	QTÀ	NUMERO PARTE	DESCRIZIONE
1	1	maschera di montaggio pezzo 1	Anticorodal
1/1	1	maschera di montaggio pezzo 2	Anticorodal

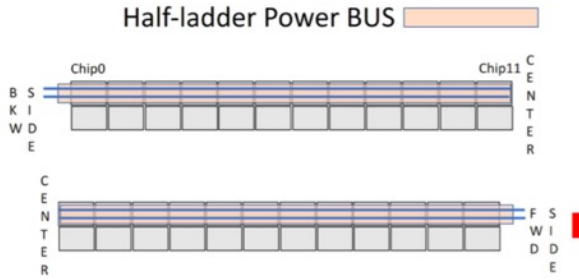


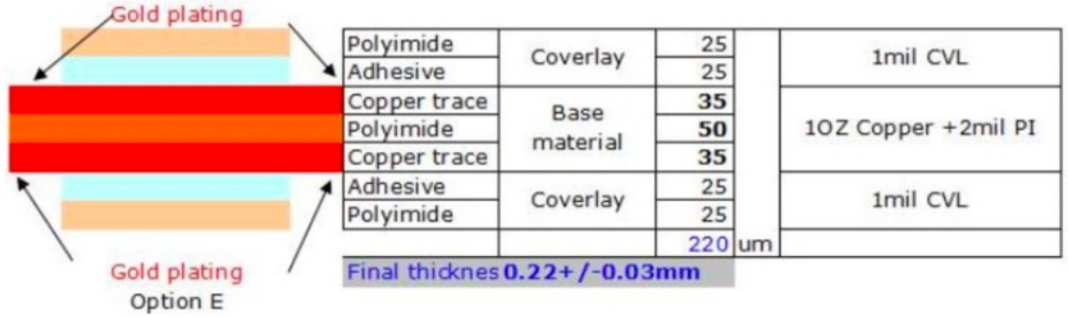
Preliminary study on the material budget estimate

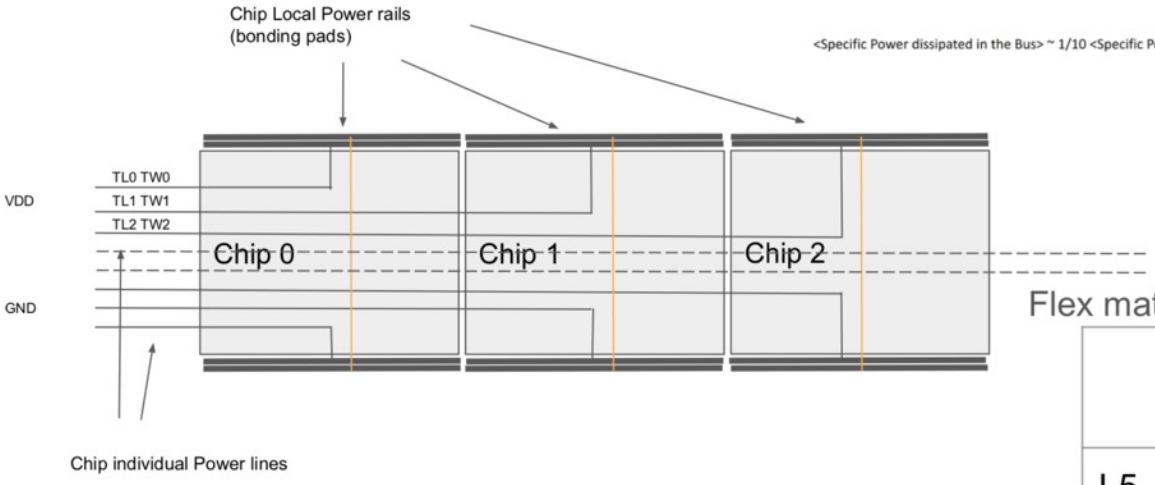
for the Power and Signal Bus (“FPC”): ½ L5 ladder (oVTX)

VTX Upgrade L3-L5 Flex Analysis

Multiline Power Bus layout Sketch







<Specific Power dissipated in the Bus> ~ 1/10 <Specific Power dissipated by the chip>

Copper FPC Total Budget 0.176 % X0

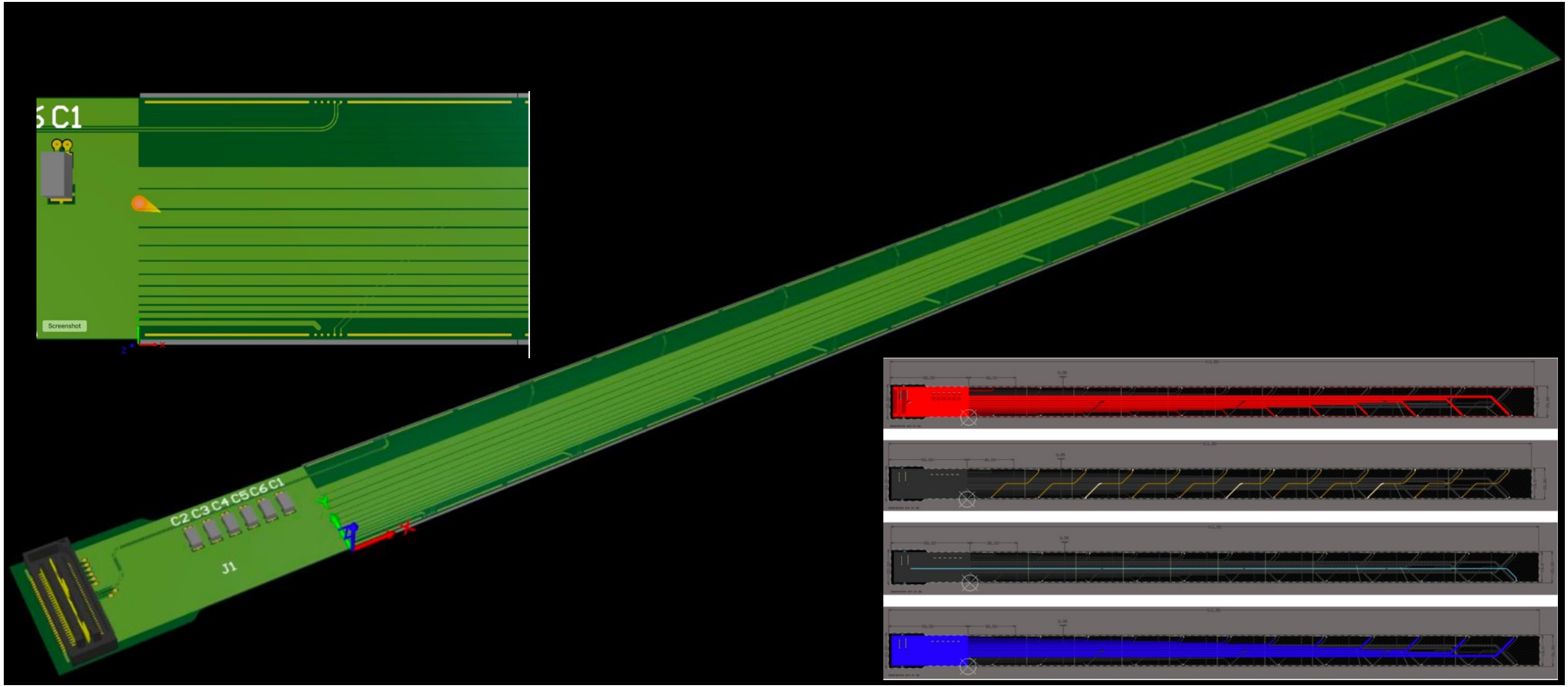
Aluminum FPC Total Budget 0.083 % X0

Total #chips@L5 = 23 (69cm)
200mW*cm^-2 Power
100mV(VDD)+100mV(GND) maxVdrop
Both Side Ladder Access
½ L5 Ladder length = 33cm
½ L5 Ladder Width = 2.0cm
FPC with 2 Layers 35u

Flex material budget Summary

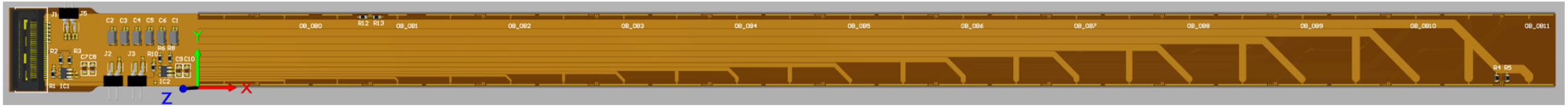
	Full (L, W, #chips)	Analysis (L/2, W, #chips)	Cu	Al	Conditions
L5	(70.041cm, 2.0cm, 24)	(36cm, 2.0cm, 12)	0.176%X0	0.083%X0	200mV, 200mWcm-2
L4	(44.526cm,2.0cm, 15)	(24cm, 2.0cm, 8)	0.117%X0	0.068%X0	
L3	(19.511cm,2.0cm, 7)	(12cm, 2.0cm, 4)	0.083%X0	0.058%X0	
L3	(19.511cm,2.0cm, 7)	(19.511cm,2.0cm, 7) One side access	0.106%X0	0.068%X0	

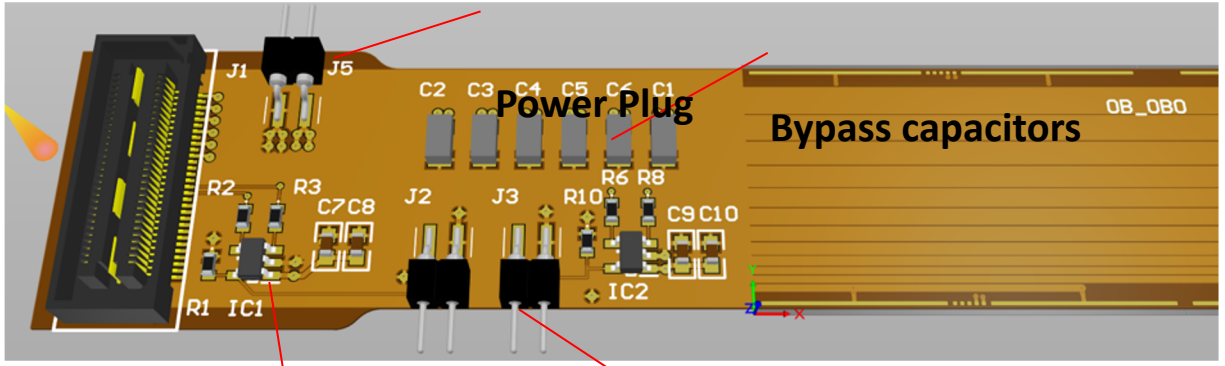
First design of the Power and Signal Bus (“FPC”)

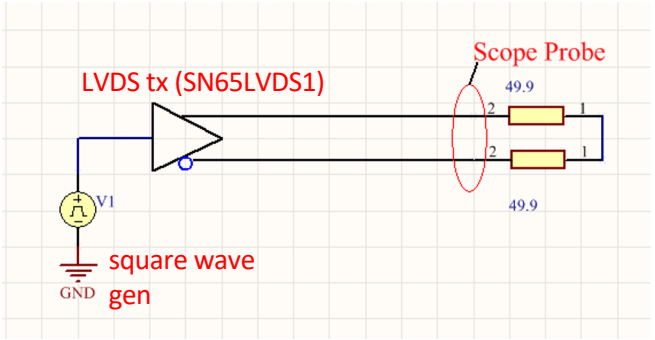


Design by M.Minuti-INFN-Pisa (specifiche: vedere backup-slide)

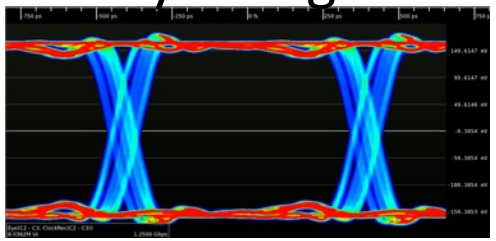
Electrical Test on the Layer-5 Cu-prototype Flex





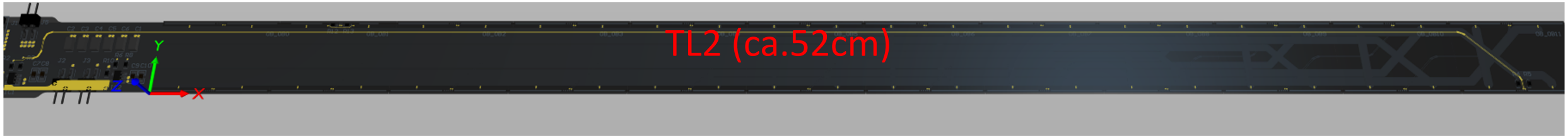


Eye-diagram



TL1 and TL2 are two 100 Ohms differential striplines.
The signals injected at J2 and J3 are translated to LVDS and transmitted over TL2 and TL1 respectively.

Orden done @ Artel → Receive the Flex in September. Test:
- verify signal integrity at the far end
- estimate BER at 160MHz (baseline frequency: see RD53A readout)
- estimate a reasonable max frequency.



Piano dei lavori dell'R&D di VTX

Meccanica:

- Stiamo ricevendo dalla ditta i pezzi: assemblaggio della maschera di incollaggio: entro fine Settembre
- Realizzazione struttura di supporto (traliccio) ed test caratterizzazione meccanica: metà/fine Ottobre
- Entro metà Settembre eseguire ordine alla ditta per la realizzazione dei prototipi della cold-plate.
- Da metà Ottobre: caratterizzazione termica cold-plate.
- Da inizio Novembre: assemblaggio della parte meccanica di supporto e della cold-plate per caratterizzazione meccanica e termica del ladder, da concludersi entro il 2021.

Sulla base dei risultati sperimentali che otterremmo e dal confronto con le simulazioni, vogliamo aver la possibilità nel 2022 di implementare le migliorie e testarle:
Richiesta di materiale (Consumo) di meccanica per il 2022: 5 kE

Parte elettrica (FLEX):

- Stabiliti Contatti con il CERN (R. DE Oliveira): offerta preliminare per la realizzazione di (minimo numero 9) prototipi di FLEX in Al. ~ 20 k CHF. Attesa una riduzione sostanziale (-40%) dei costi nel 2022, quando il CERN potrà Fare ("in casa) la deposizione dell'Al.

Richiesta (Consumo) per contributo per la realizzazione del Flex in Al per il 2022: 5 kE

Riepilogo richieste SVD Pisa 2022

Capitolo	Categoria	Descrizione	Richiesta	Richiesta SJ	Anticipabile
missioni	D	Turni di sotto-rivelatore (SVD)	6		
missioni	C	SVD manager	5		
missioni	C	Attività Shutdown 2022	36		
manutenzione	D	Manutenzione annuale Power Supply crates, boards e PDP di SVD	6		no
apparati	A	1 Crate + grupp PDP spare (controller,LV, HV)	8.5		si
consumo	A	Materiale (CF, foams, u-tubi) per assemblaggio moduli prototipo meccanici per CDR	5		
consumo	A	Dissipatori, sensori di temperatura, collettori per la caratterizzazione termica dei prototipi nel lab. di termo-fluido-dinamica di sezione	2		
consumo	A	Produzione prototipi di circuiti flex in Cu/Al	5		
missioni	A	Partecipazione VTX workshop in Eu per 5 persone (viaggio + 3 gg)	3		
missioni	A	Viaggi per contatti presso Labs (CERN) o ditte per procurement materiali e realizzazione circuiti flex	2		
missioni	C	Upgrade Working Group convener	5		
missioni	C	Test-beam sensore CMOS ?	0		
consumo	A	Cofinanziamento 25% sottomissione CMOS CHIP Obelix (sinergia con AIDAInnova)	50		

← Da restituire a CMS-PI

Non comporta un impegno di costruzione, è ancora solo R&D. I fondi dovrebbero venire da quelli dedicati da INFN agli sviluppi AIDAInnova (NON direttamente dal progetto europeo che non prevede fondi di sottomissioni).

BACKUP SLIDES

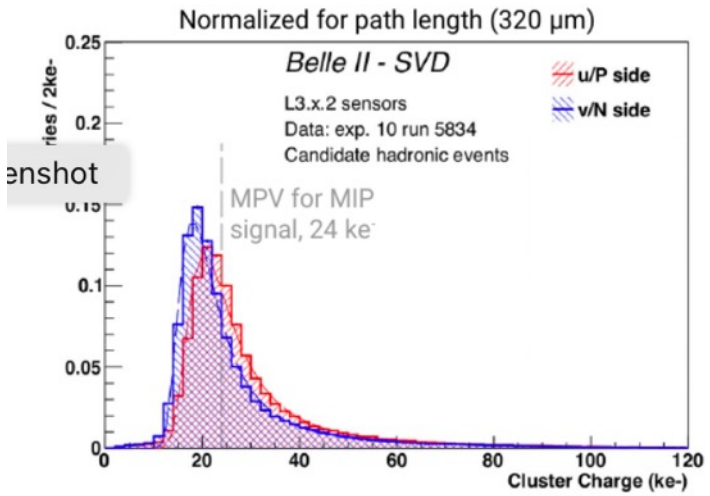
Signal charge and signal to noise ratio

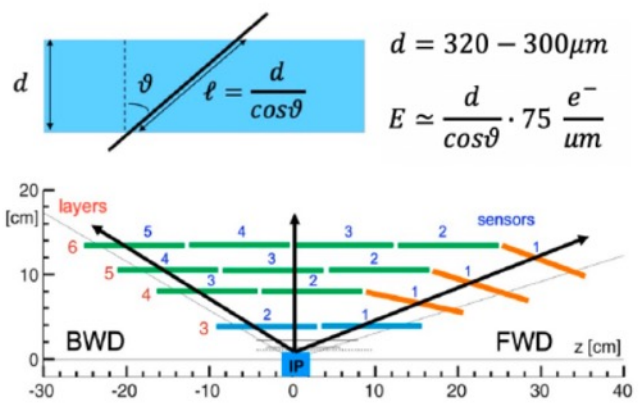
Signal charge normalised for the track path length in silicon similar in all sensors and matches expectations

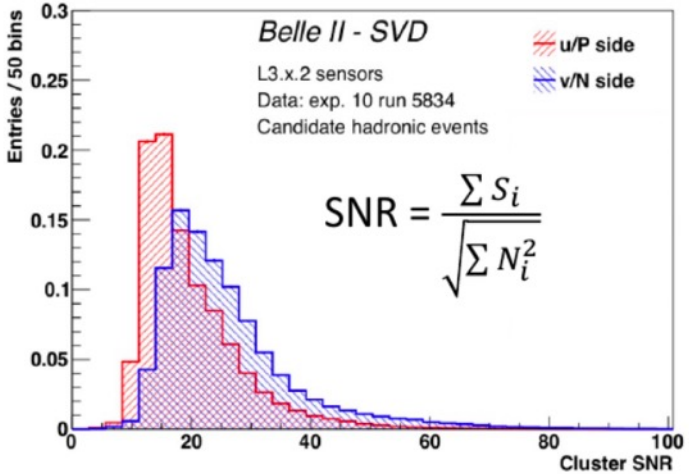
- u/P side: charge in agreement with expectation from MIP taking into account ~ 15% uncertainty in APV25 gain calibration
- v/N side: 10%-30% signal loss due to large pitch and presence of floating strip

Very good SNR in all 172 sensors (most probable value: 13-30)

- u/P side: larger noise due to longer strip length (larger inter-strip capacitance)

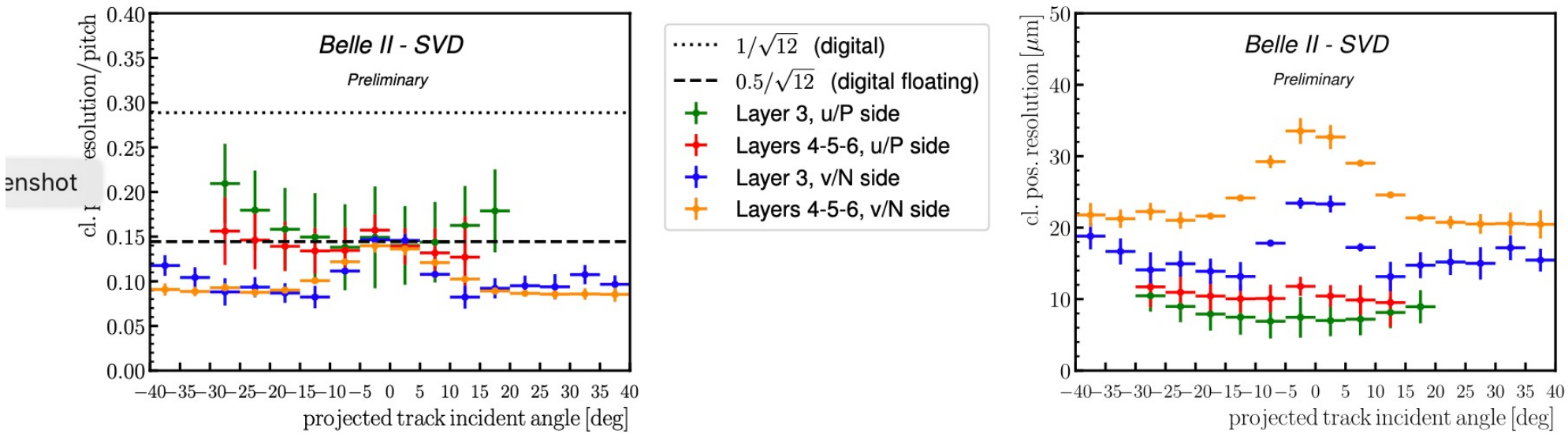






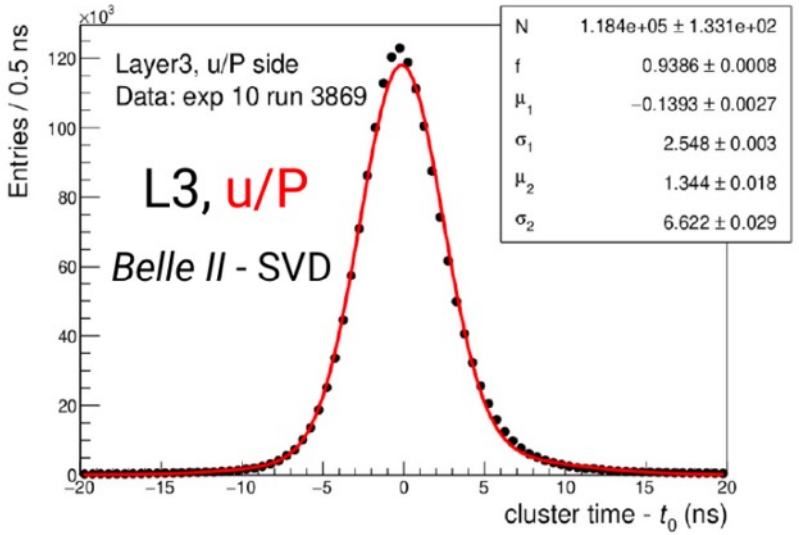
Cluster position resolution

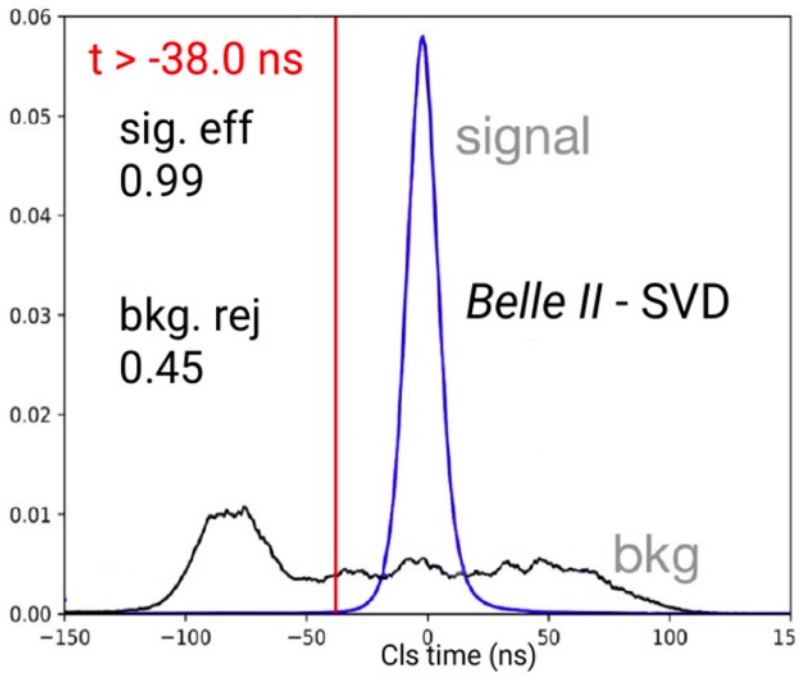
- Preliminary cluster position resolution measured on data
- Estimated from the residuals of the cluster position with respect to the track (unbiased) using $e^+e^- \to \mu^+\mu^-$ events
- Effect of the track extrapolation error subtracted
- Excellent position resolution in agreement with the expectations from the pitch
- Still room for improvement for the u/P side (work ongoing)



Hit time resolution

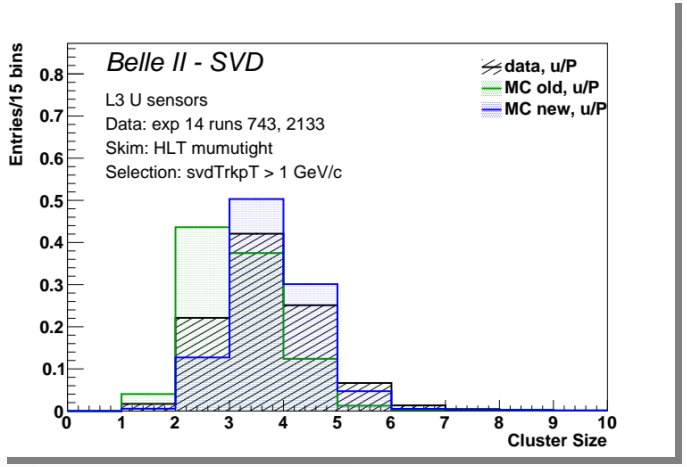
- Excellent hit time resolution wrt event time provided by CDC (~ 2.9 ns u/P, ~ 2.4 ns v/N)
- Possible to efficiently reject off-time background hits
  - Will be used for higher luminosity and background levels

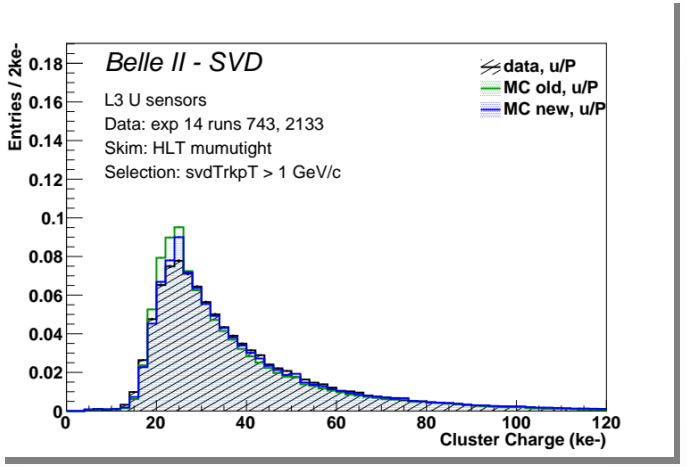


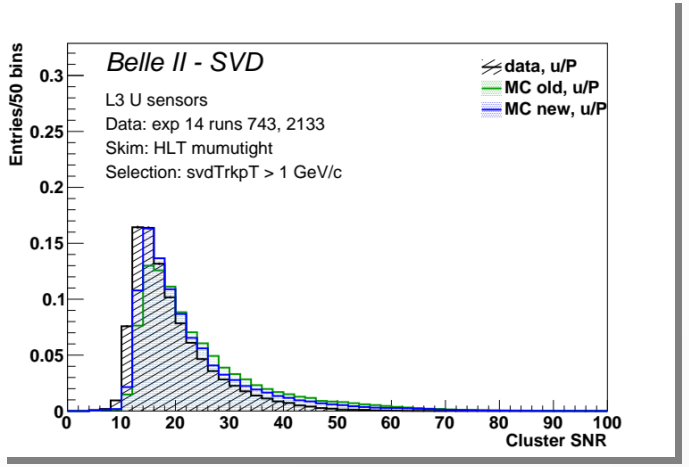


Improvements/Activities on offline SW

- Better modeling of the signal formation in simulation improved matching data/MC for cluster properties
  - Charge sharing & APV channel coupling measured on data now in MC
  - Further optimization of some parameters ongoing







- A lot of activity on cluster position resolution:
  - exploring different cluster position algorithms, overlap method, best method to extract correctly the resolution from residuals … still work in progress
  - Before: resolution on data was already good enough for physics performance but there was room for improvement & MC resolution was too optimistic
  - Now: improved resolution on data and MC resolution also getting more realistic… still work in progress

Note: SVD SW Coordinator change: G. Casarosa served as SVD SW coordinator since June 2017, now moving on tracking responsibility.
F. Tenchini recently joined the Pisa group and he took over (since 1st July).
Giulia will be still in the SVD SW group, helping in the transition in the next months.

“FPC” Spec’s:

Belle-II VTX Upgrade L5 Flex

4 layers
Top and Bottom 20u Al used for power distribution
Internal Layers 10u Al tracks used for signals
100 um diameter MicroVias
0.7mm/0.20mm Plated Through Hole Vias
80um minimum Track Width/Isolation
50um Polyimide Core
60um Dielectric layers (Polyimide + glue)

	Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant
	Top Overlay 1	Overlay				
	Top Solder 1	Solder Mask/Co...	Surface Material	0.001	Solder Resist	3.5
1	Top	Signal	Copper	0.02		
	Dielectric 1	Dielectric	Prepreg	0.06	polyimide+glue	3.75
2	Signal Layer 1	Signal	Copper	0.01		
	Dielectric 3	Dielectric	Core	0.05	Polyimide	3.5
3	Signal Layer 2	Signal	Copper	0.01		
	Dielectric 2	Dielectric	Prepreg	0.06	polyimide+glue	3.75
4	Bottom	Signal	Copper	0.02		
	Bottom Solder 1	Solder Mask/Co...	Surface Material	0.001	Solder Resist	3.5
	Bottom Overlay 1	Overlay				

Finishings:
-)Anything compatible with wedge microbonding in the chip Area (Top Layer)
-)Anything compatible with thin soldering in the connector area
-)passivations

- After some “interactions” with the CERN Workshop (Rui De Oliveira) we are ready to recevice a quotation for some (1→5) Aluminum FPC prototypes.
- Looking for other companies willing to perform R&D on Aluminum FPC
- The goal is to optimize the design to the test signal integrity@the target speed for signals and stability for the power voltage.