TIIMM0/1 prototype: Cadence mixed simulation/verification

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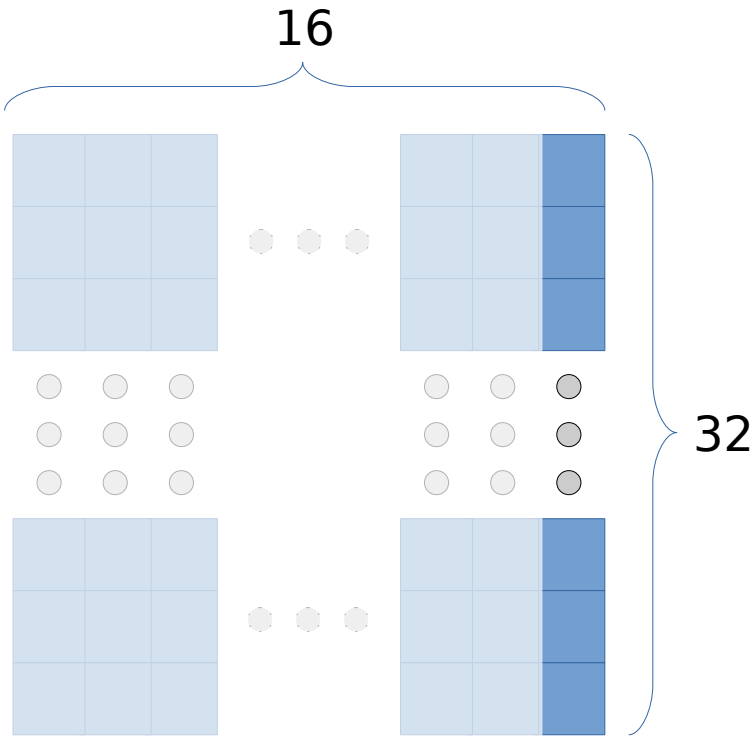
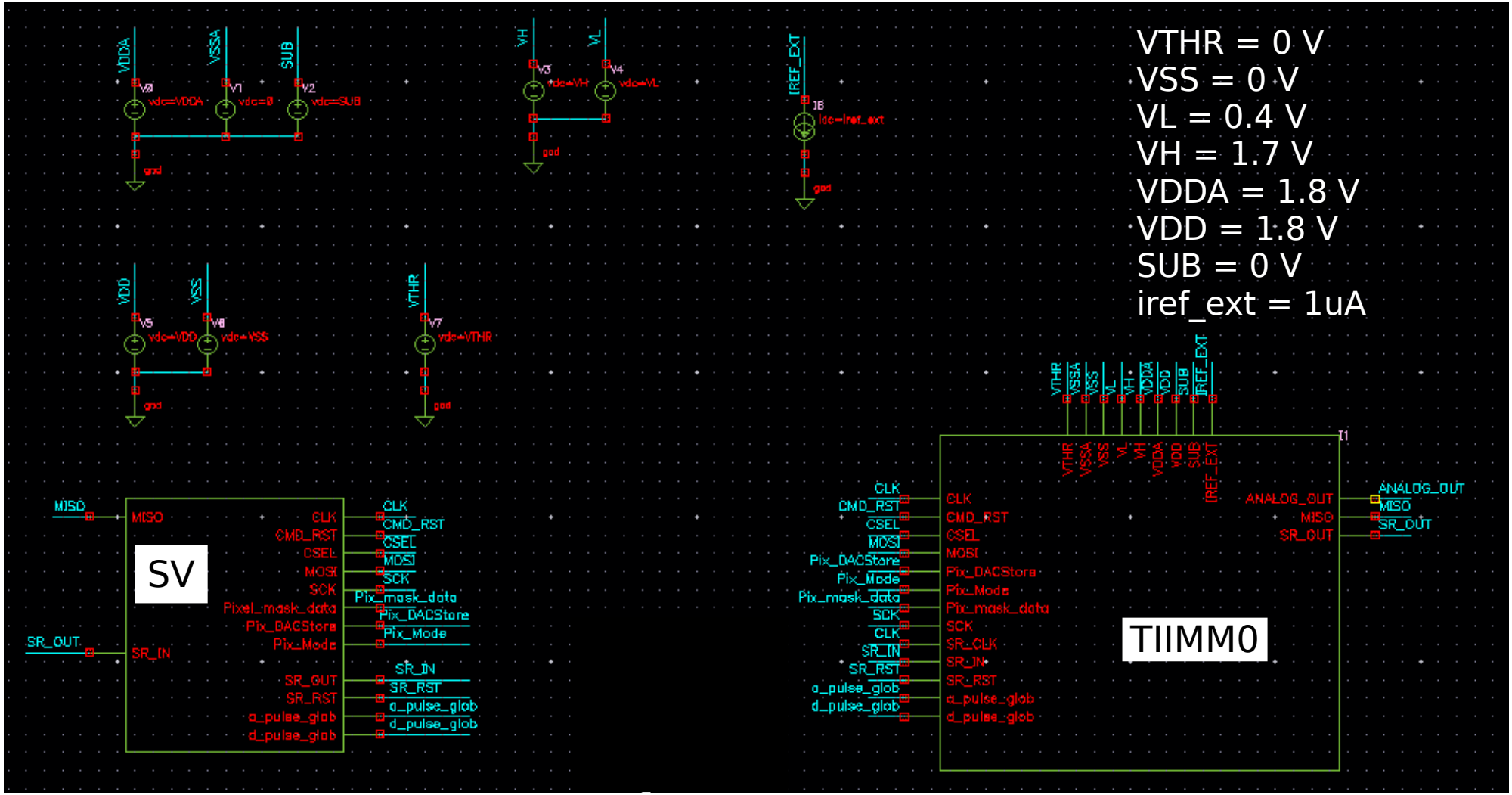
Outline

- TIIMM0 AMS simulation testbench

- First TIIMM0 simulation outcomes



TIIMM0
testbench schematic



TIIMM0
testbench cell views

Library	Cell	View Found
TIIMM0_SIM_01_07_20...	stim_SPI	systemVerilog
TIIMM0_SIM_01_07_20...	tb_TIIMM0	schematic
TIIMM0_master	AmpRefCur	schematic
TIIMM0_master	AnalogOutput	schematic
TIIMM0_master	Bandgap	schematic
TIIMM0_master	BiasAmpRef	schematic
TIIMM0_master	COLAnOut	schematic
TIIMM0_master	CSA	schematic
TIIMM0_master	DAC_CompIB	schematic
TIIMM0_master	DAC_IAnout	schematic
TIIMM0_master	DAC_IBS	schematic
TIIMM0_master	DAC_IKrumm	schematic
TIIMM0_master	DAC_PixelDACIref	schematic
TIIMM0_master	DAC_Vbscasc	schematic
TIIMM0_master	DAC_Vfbk	schematic
TIIMM0_master	DAC_Vpcasc	schematic
TIIMM0_master	DAC_cell	schematic
TIIMM0_master	FEEDBACK	schematic
TIIMM0_master	IntFace_Comp_Ib	schematic
TIIMM0_master	IntFace_IAnout	schematic
TIIMM0_master	IntFace_IKrumm	schematic
TIIMM0_master	IntFace_Ibs	schematic
ts018_prim	cpwnmos_thn	spectre
ts018_prim	ddwnps18	spectre
ts018_prim	ddwnpw18	spectre
ts018_prim	ndio_nosal	spectre

Library	Cell	View Found
TIIMM0_master	IntFace_PixelDACIRef	schematic
TIIMM0_master	IntFace_Voltage	schematic
TIIMM0_master	RefCurrent	schematic
TIIMM0_master	STRONG0_Column	schematic
TIIMM0_master	STRONG0_ColumnAno...	schematic
TIIMM0_master	STRONG0_Matrix	schematic
TIIMM0_master	Strong0_DAC	schematic
TIIMM0_master	TOP_STRONG0_core	schematic
TIIMM0_master	TOP_TIIMM0	schematic
TIIMM0_master	TrimDAC_v1	schematic
TIIMM0_master	ad_ELT_050	schematic
TIIMM0_master	ad_ELT_6	schematic
TIIMM0_master	comparator	schematic
TIIMM0_master	csa_and_comp	schematic
TIIMM0_master	csa_with_feedback	schematic
TIIMM0_master	pixel_cell_analog	schematic_sim
TIIMM_DIGITAL	RowSelect	External HDL
TIIMM_DIGITAL	S0CommandDecoder	External HDL
TIIMM_DIGITAL	StrongPixelReader	External HDL
analogLib	cap	spectre
analogLib	idc	spectre
analogLib	vdc	spectre
ts018_prim	nmos_18	spectre
ts018_prim	pmos_18	spectre
ts018_prim	rpmpoly3t	spectre
ts018_prim	vnpn18_5	spectre

TIIMM0 AMS simulation Warning from spectre during hierarchy flattening

WARNING (SPECTRE-8527): some nodes and instances removed from the netlist topology check

Total removed instances 8 (dangling 0, terminals connected together 8)

Warning from spectre during hierarchy flattening.
WARNING (SPECTRE-8531): Floating node. tb_TIIMM0.I1___dUmmY_pORt_**0**_ is removed.
WARNING (SPECTRE-8531): Floating node. tb_TIIMM0.I1___dUmmY_pORt_**1**_ is removed.
WARNING (SPECTRE-8531): Floating node. tb_TIIMM0.I1___dUmmY_pORt_**2**_ is removed.
WARNING (SPECTRE-8531): Floating node. tb_TIIMM0.I1___dUmmY_pORt_**3**_ is removed.
WARNING (SPECTRE-8531): Floating node. tb_TIIMM0.I1___dUmmY_pORt_**4**_ is removed.
Further occurrences of this warning will be suppressed.

TIIMM0 AMS simulation Notice from spectre during topology check.

No connections to node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**0**'.
No connections to node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**1**'.
No connections to node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**10**'.
No connections to node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**11**'.
No connections to node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**12**'.
Further occurrences of this notice will be suppressed.

No DC path from node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**0**' to ground,
Gmin installed to provide path.
No DC path from node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**1**' to ground,
Gmin installed to provide path.
No DC path from node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**10**' to ground,
Gmin installed to provide path.
No DC path from node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**11**' to ground,
Gmin installed to provide path.
No DC path from node `tb_TIIMM0.I1.I0.I1__RowSelectMask__26__**12**' to ground,
Gmin installed to provide path.
Further occurrences of this notice will be suppressed.

TIIMM0 AMS simulation

Notice from spectre at time = 99.5057 us during transient analysis `tran'.
    Found **trapezoidal ringing** on node **tb_TIIMM0.I1.I0.DAC_Ref_b[2]**.
Notice from spectre at time = 99.5067 us during transient analysis `tran'.
    Found trapezoidal ringing on node tb_TIIMM0.I1.I0.DAC_Ref_b[2].
Notice from spectre at time = 99.5084 us during transient analysis `tran'.
    Found trapezoidal ringing on node tb_TIIMM0.I1.I0.DAC_Ref_b[2].
Notice from spectre at time = 99.5493 us during transient analysis `tran'.
    Found trapezoidal ringing on node tb_TIIMM0.I1.I0.DAC_Ref_b[2].

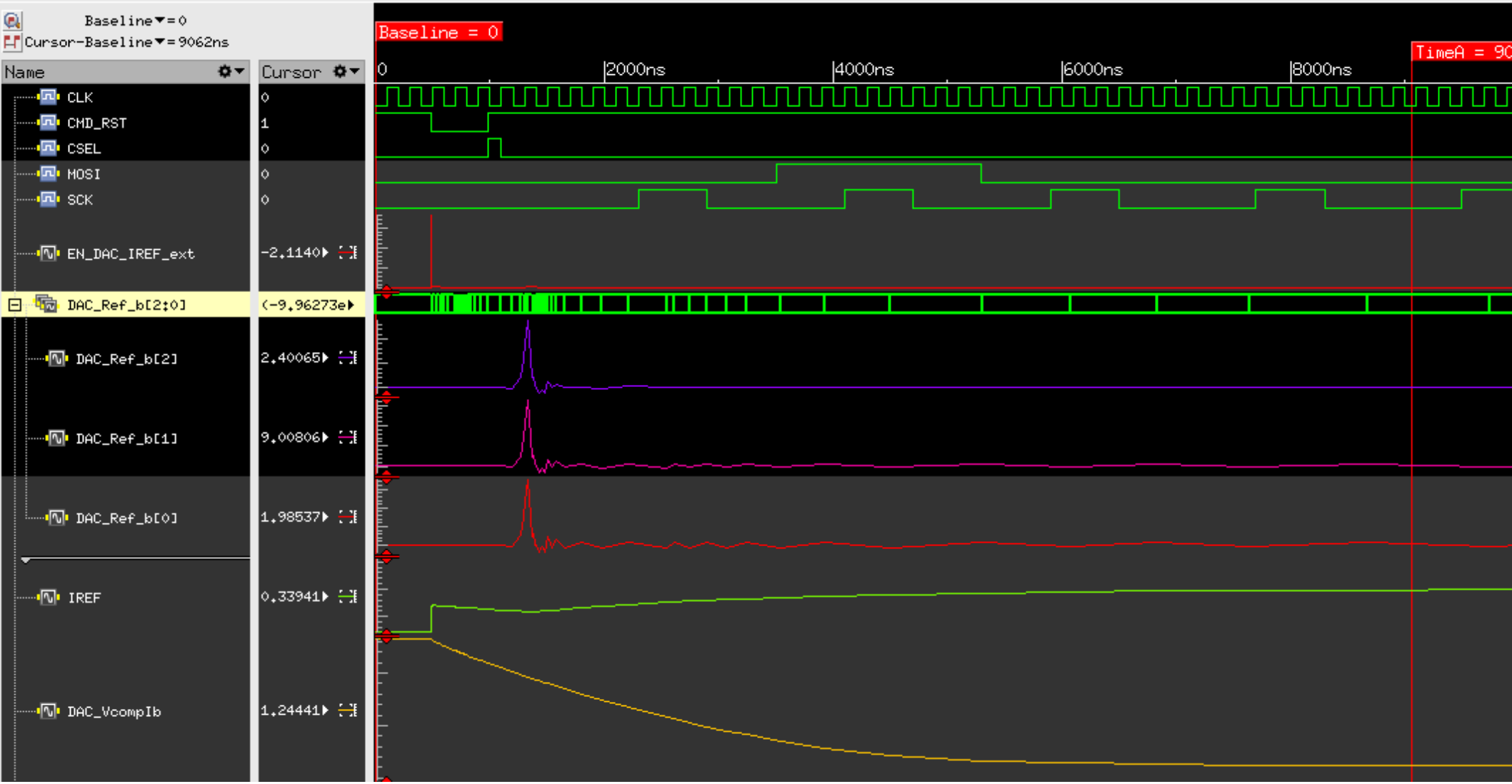
Notice from spectre at time = 127.681 us during transient analysis `tran'.
    Found **trapezoidal ringing** on node **tb_TIIMM0.I1.I0.DAC_Vfbk**.

TIIMM0 AMS simulation timing violation

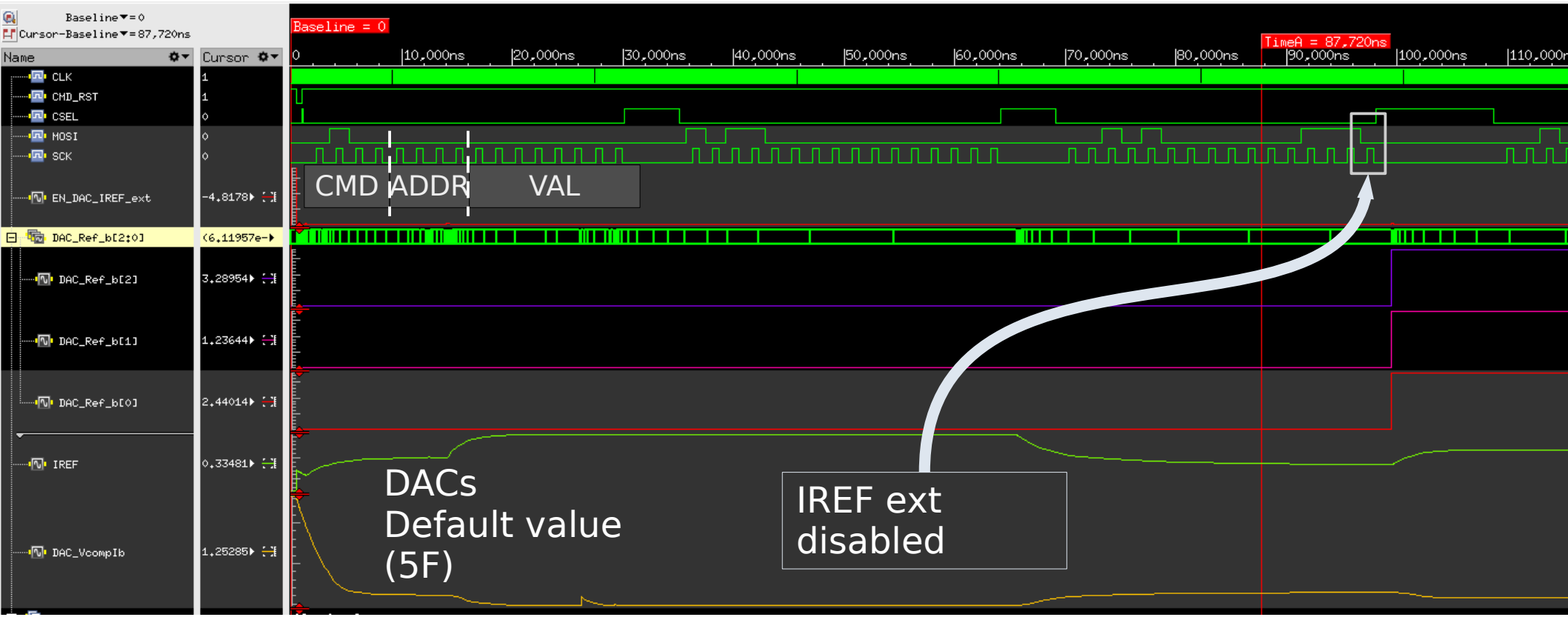
Warning! Timing violation
$setuphold<hold>(posedge CP:148902 NS, negedge D:148902 NS, 1.000 : 1 NS, 1.000 : 1 NS);
File: /Dkits/Cds_6.0/TOWER/TS18IS/IP_TOWER/SRC/Std_cells/tsl18fs120_Rev_2015.11/lib/verilog/tsl18fs120.v, line = 9191
Scope: tb_TIIMM0.I1.I0.I8.\SPI_MOSIr_reg[0]
Time: 148902 NS

Warning! Timing violation
$setuphold<hold>(posedge CP:152502 NS, posedge D:152502 NS, 1.000 : 1 NS, 1.000 : 1 NS);
File: /Dkits/Cds_6.0/TOWER/TS18IS/IP_TOWER/SRC/Std_cells/tsl18fs120_Rev_2015.11/lib/verilog/tsl18fs120.v, line = 9188
Scope: tb_TIIMM0.I1.I0.I8.\SPI_MOSIr_reg[0]
Time: 152502 NS

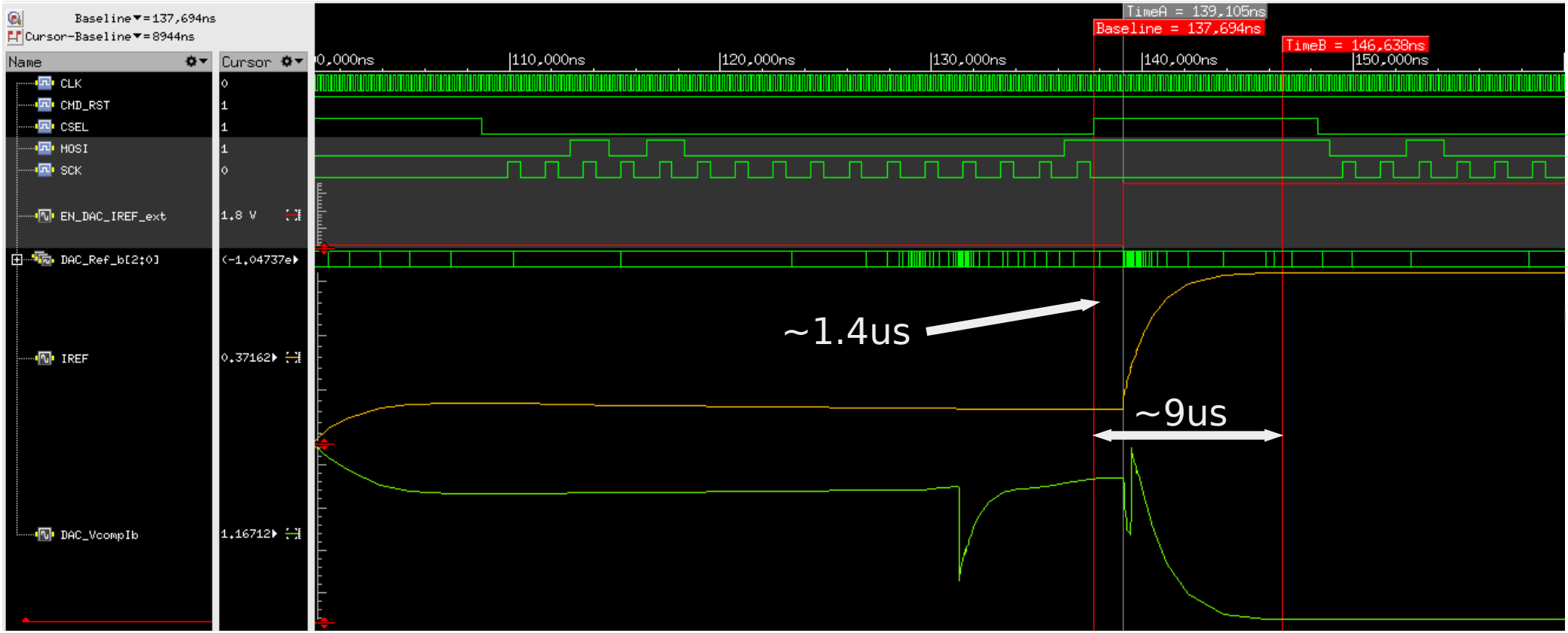
TIIMM0 AMS simulation
Reset



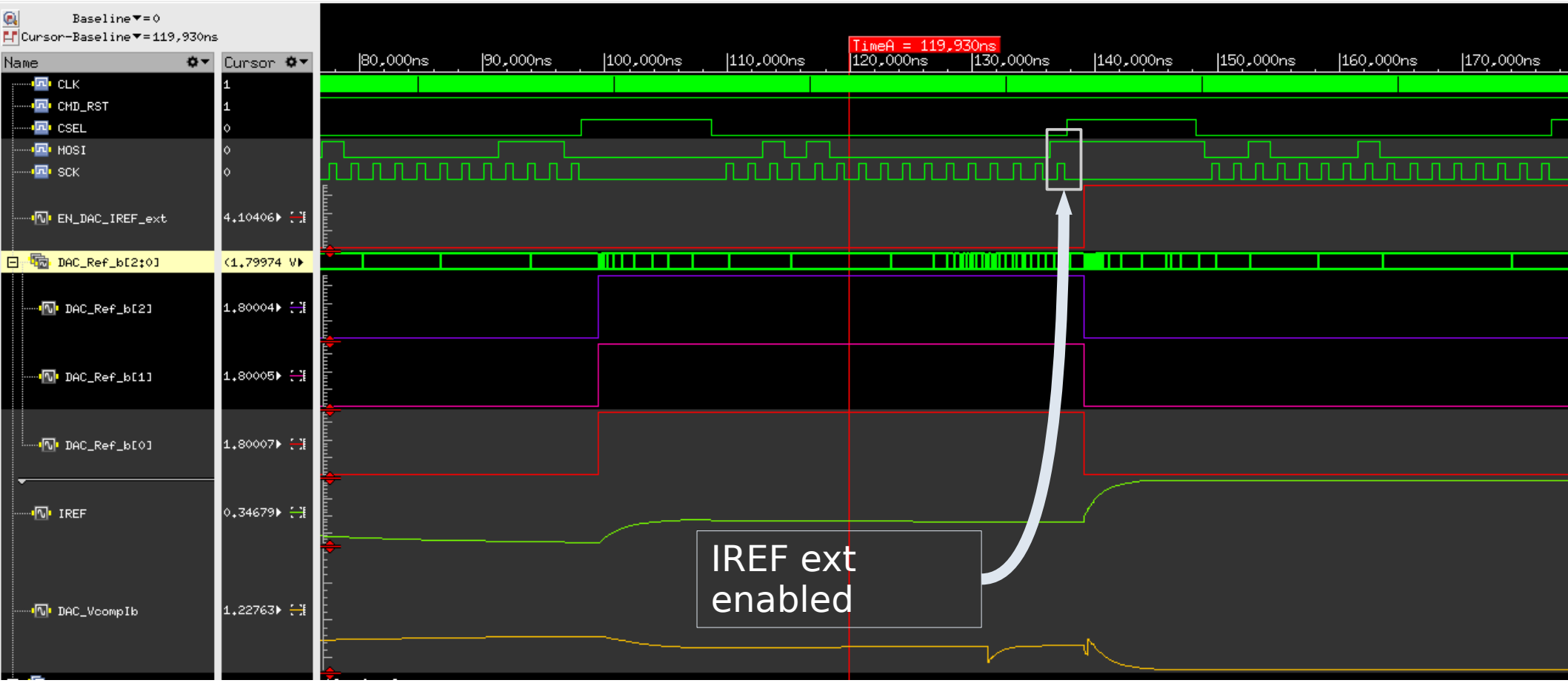
TIIMM0 AMS simulation
BandgapReset – IREF set



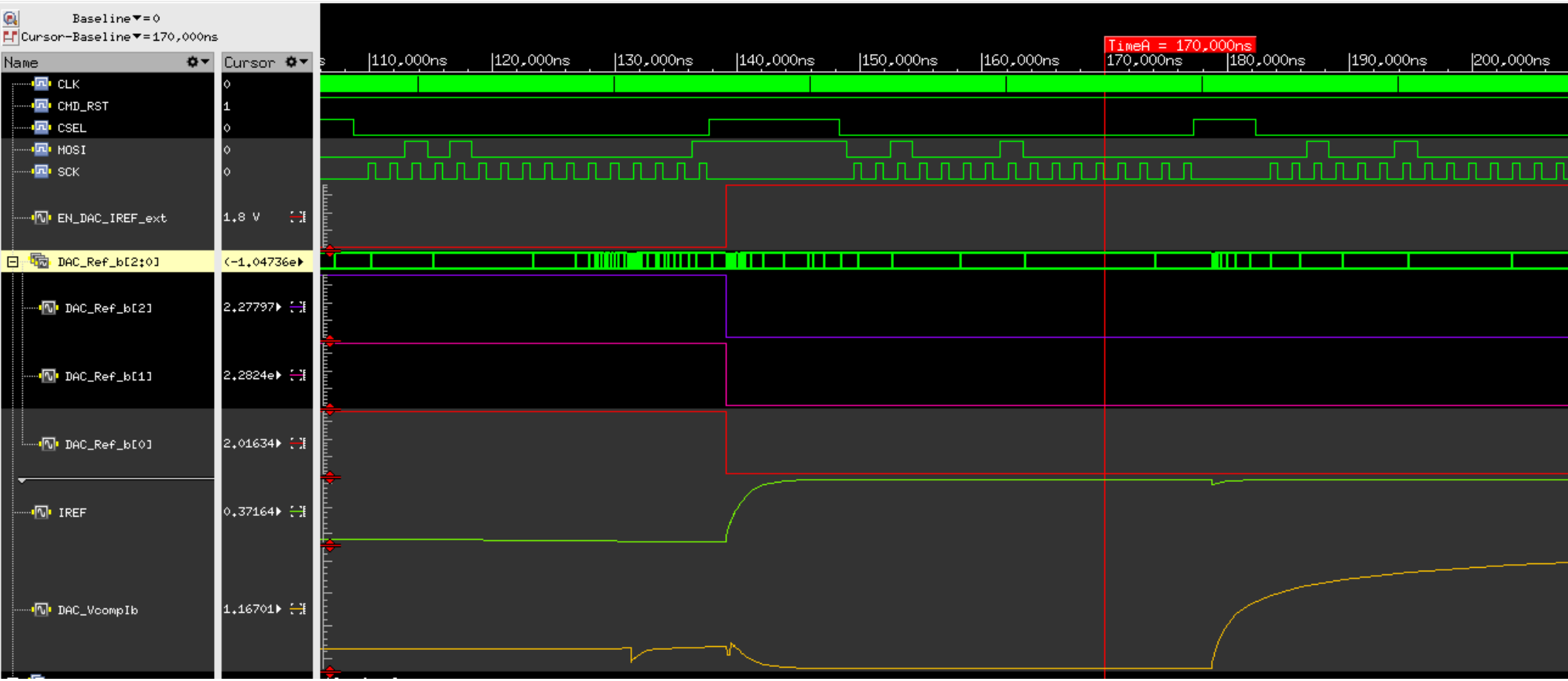
TIIMM0 AMS simulation
IREF set - timing



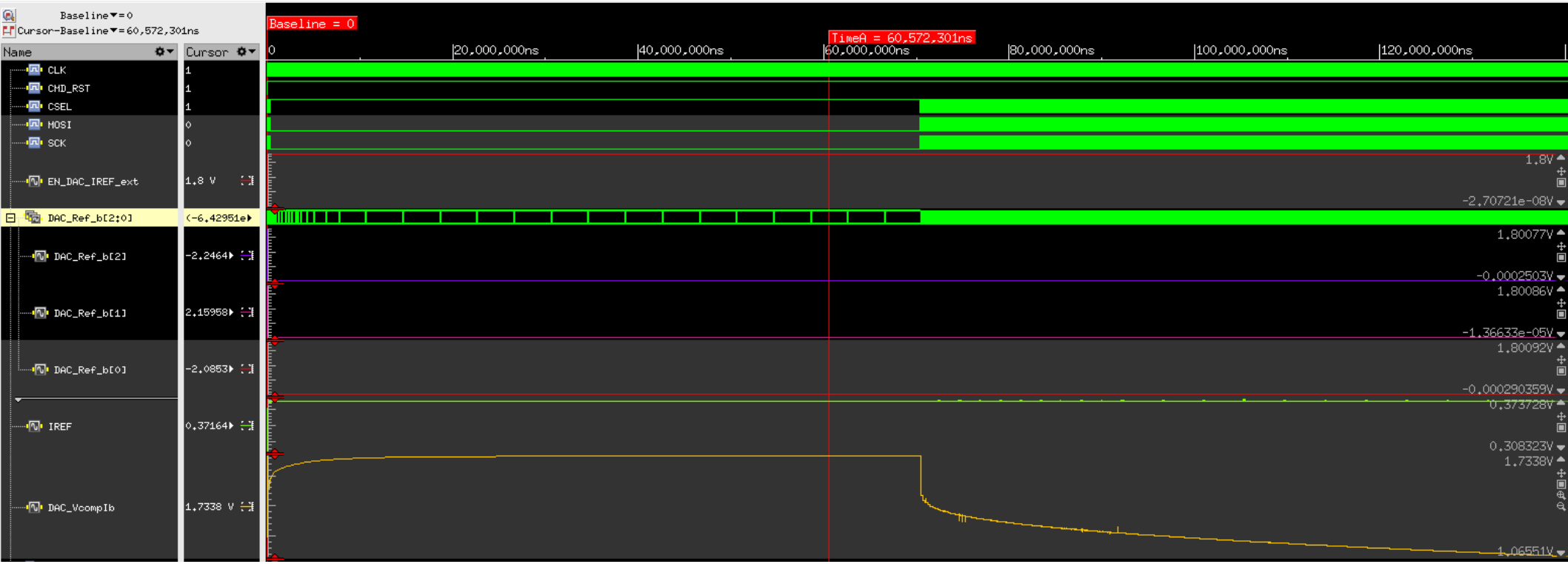
TIIMM0 AMS simulation
IREF ext (1uA) enabled



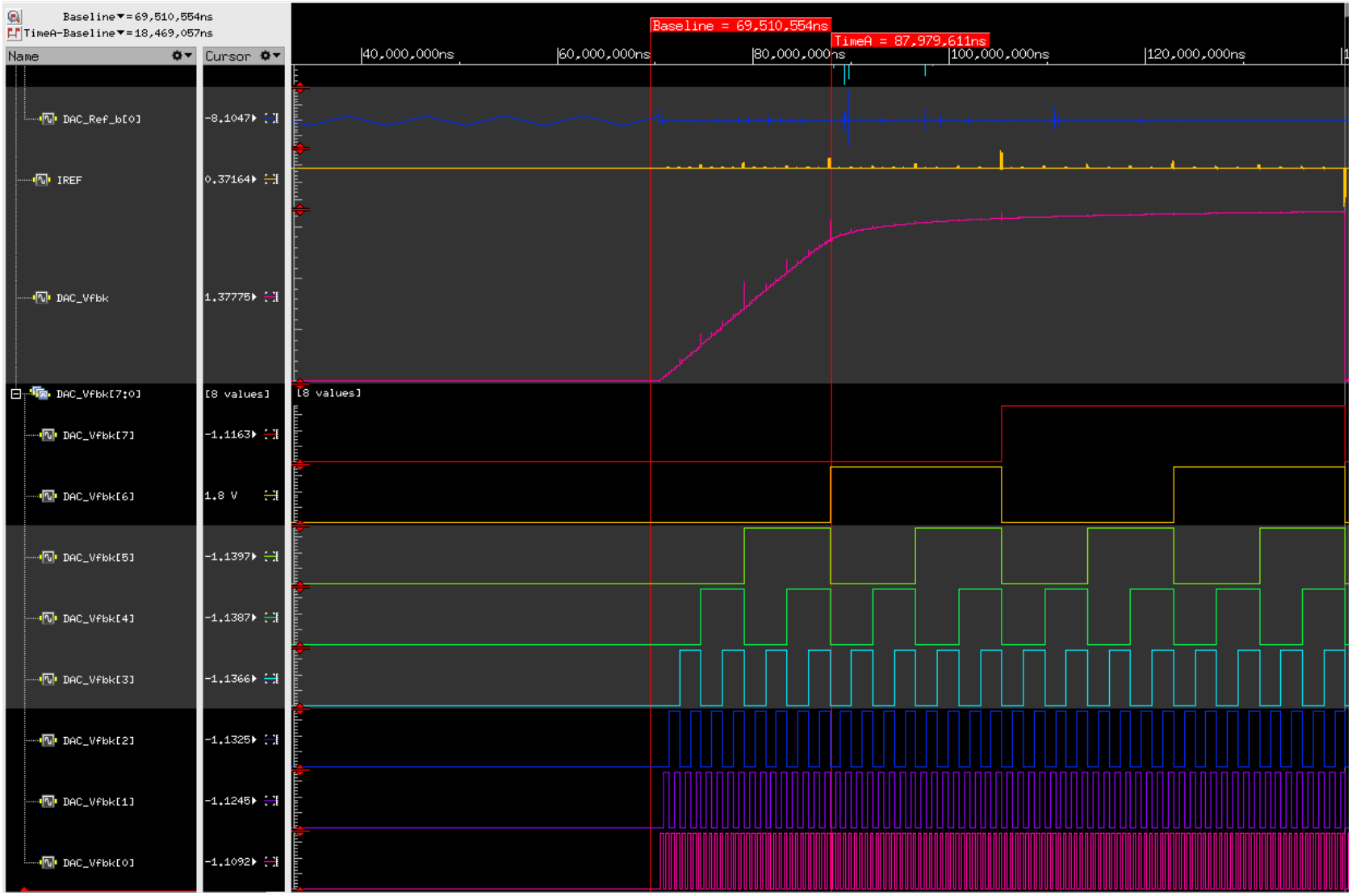
TIIMM0 AMS simulation
Vcomplb DAC – 0



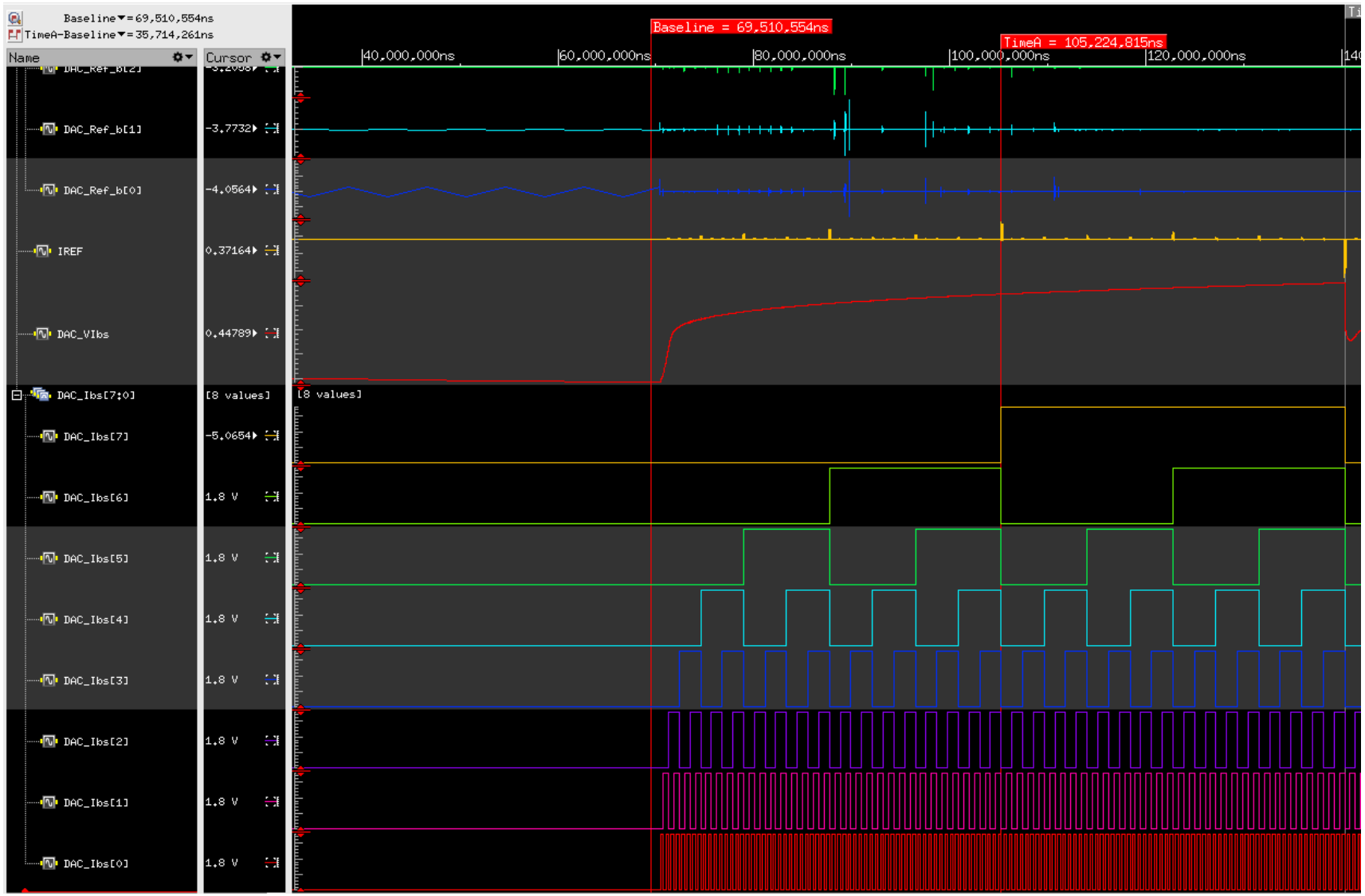
TIIMM0 AMS simulation
Vcomplb DAC – whole range



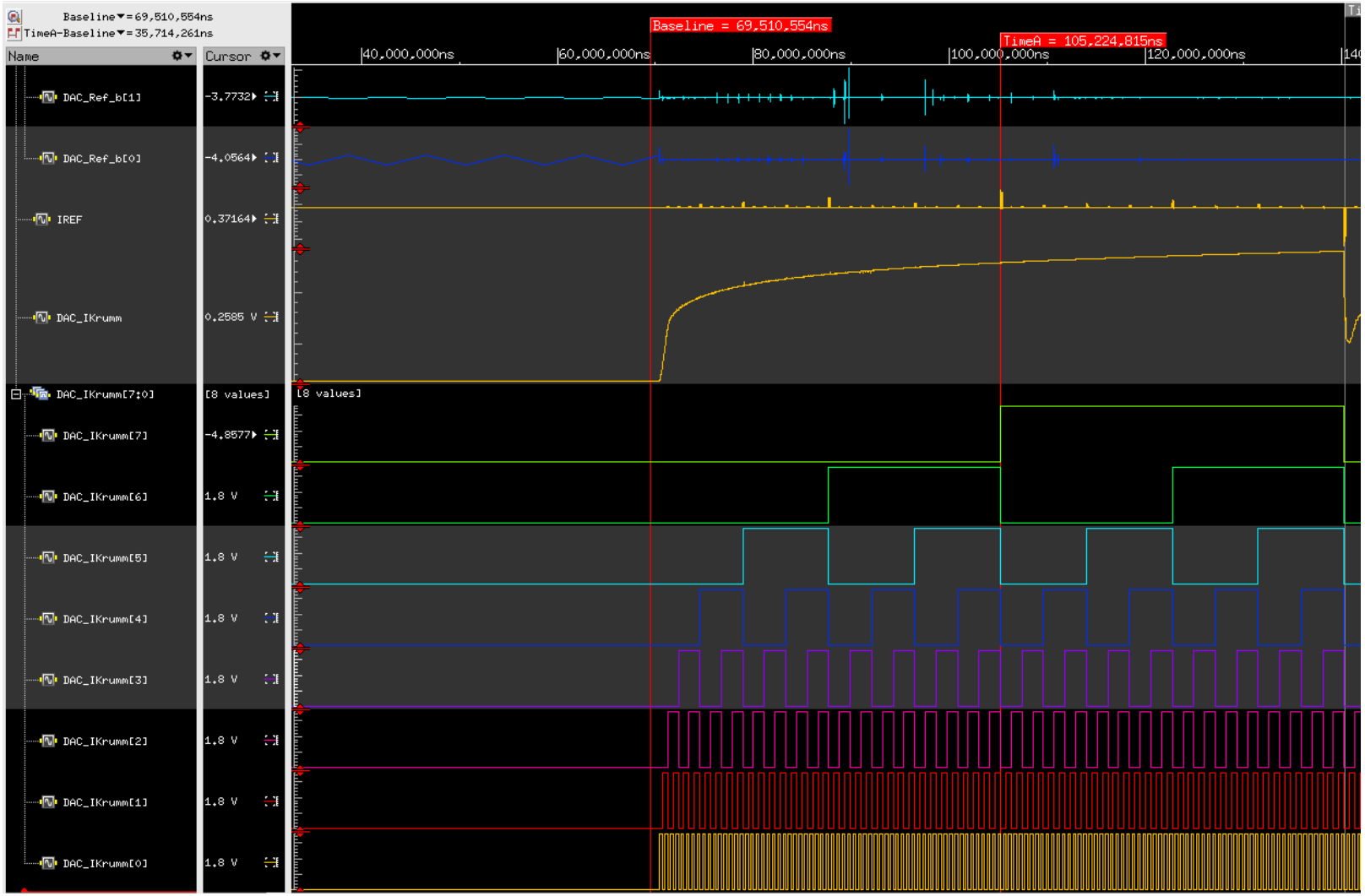
TIIMM0 AMS simulation
Vfbk DAC – whole range



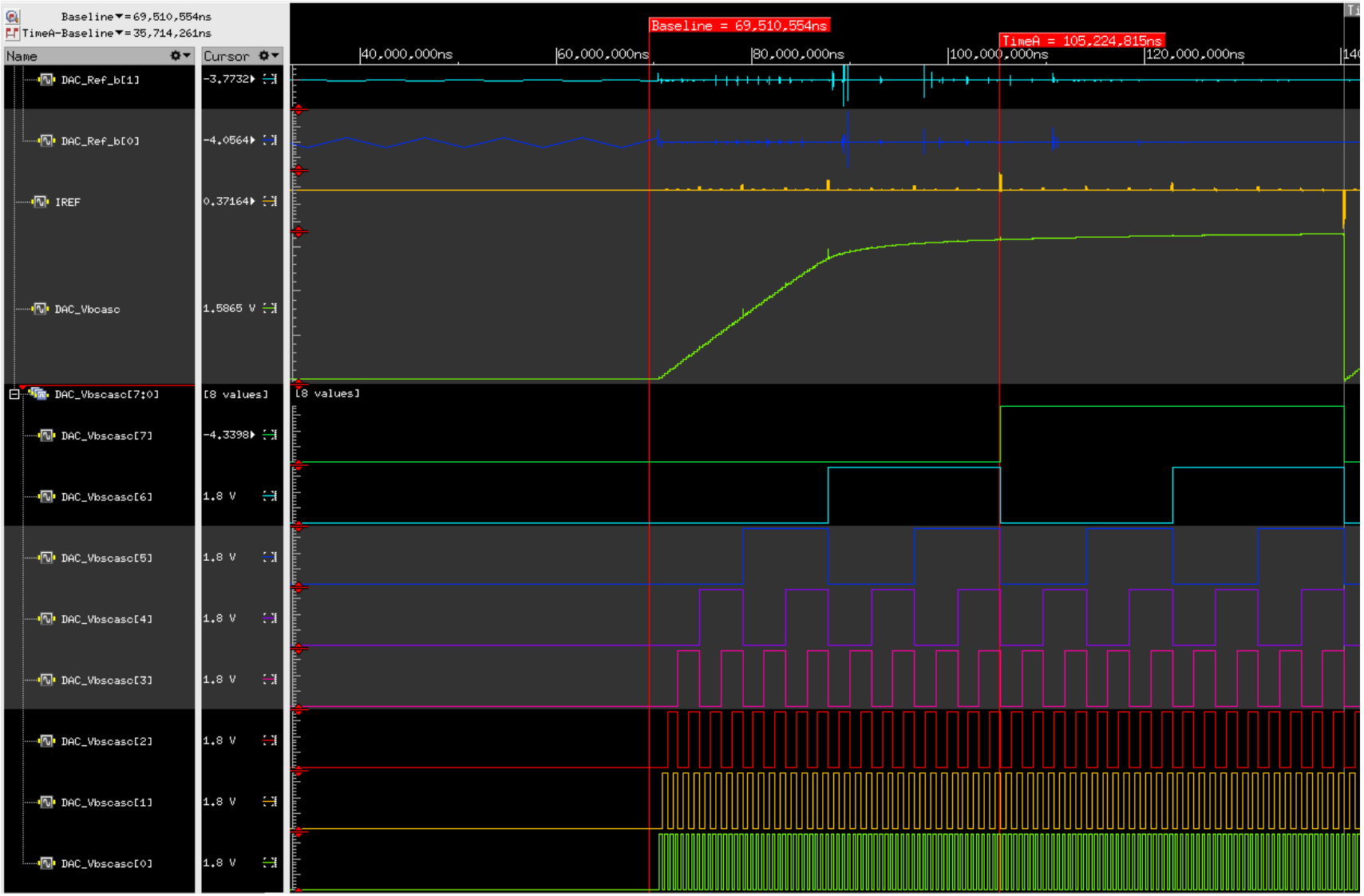
TIIMM0 AMS simulation
VIbs DAC – whole range



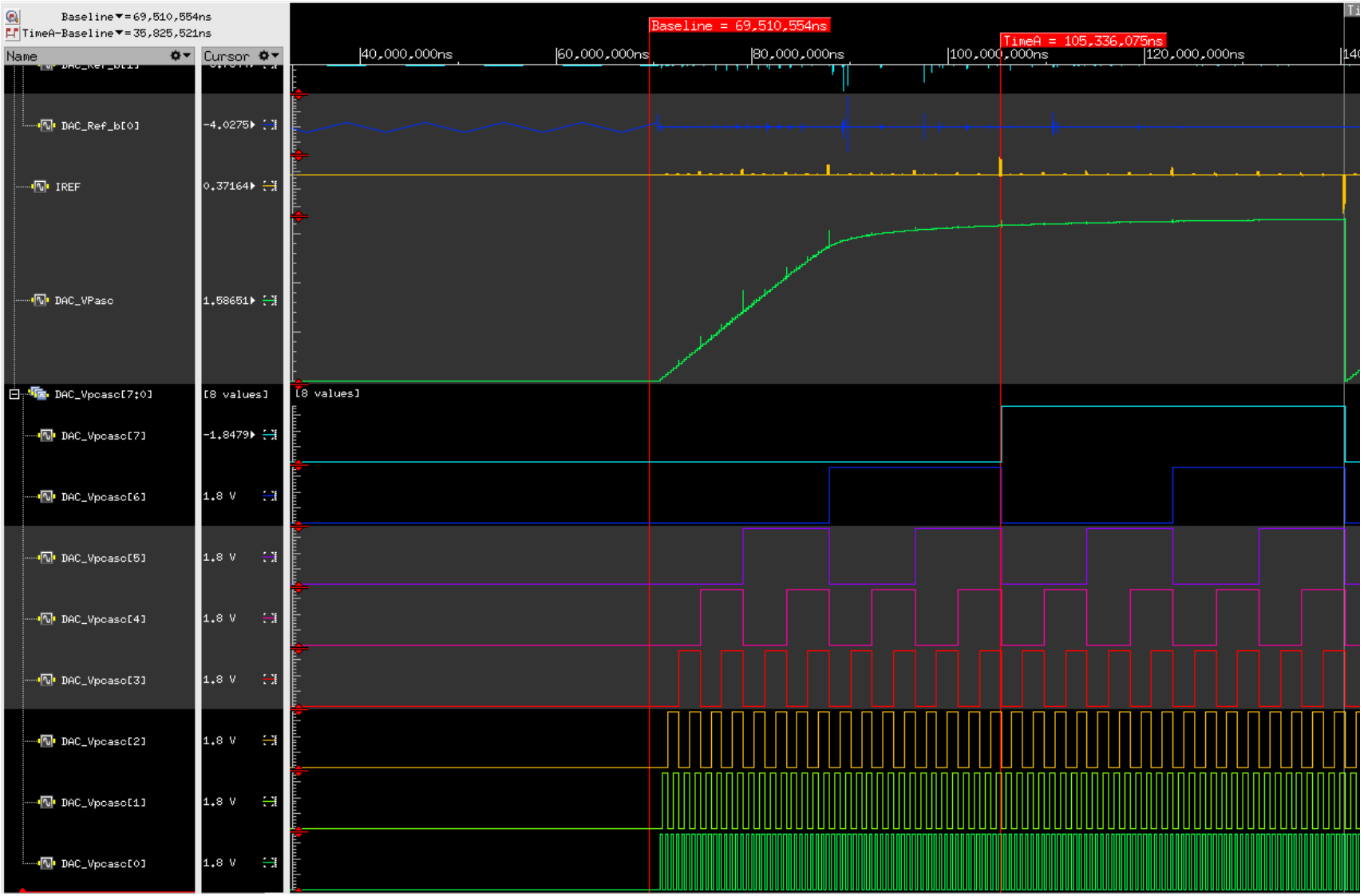
TIIMM0 AMS simulation
VIkrumm DAC – whole range



TIIMM0 AMS simulation
Vbcasc DAC – whole range



TIIMM0 AMS simulation
Vpcasc DAC – whole range



Next steps

+ continue with the physical DUT charact. approach to TIIMM0 Full matrix simulation;
+ extend the simulation to the TIIMM1 full and only_analog;