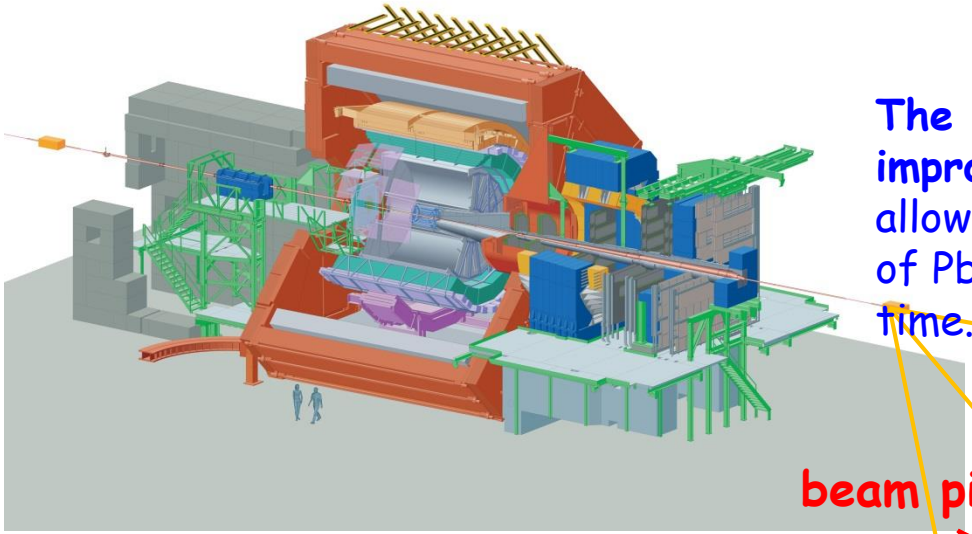
ALICE/ZDC

Il progetto ZDC consiste in 2 coppie di calorimetri adronici (112.5 m da IP2) e una coppia di calorimetri elettromagnetici (7.5 m da IP2).

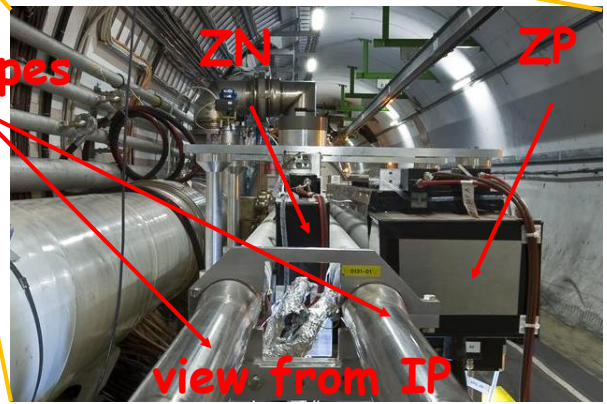
Progetto 100% INFN
Sezione INFN Cagliari
Sezione INFN Torino
(istituti di Alessandria e Torino)

Ruoli di responsabilita':
ZDC Project Leader (N. De Marco)
ZDC Deputy Project Leader (P. Cortese)
ZDC Offline Coordinator (C. Oppedisano)
ZDC Technical Coordinator (P. Mereu)

ALICE/ZDC



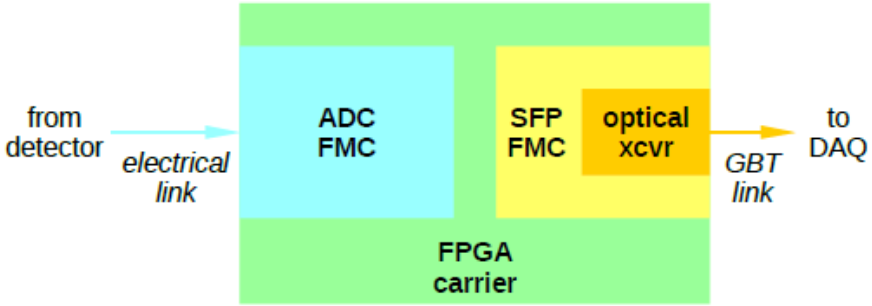
The main target of ZDC upgrade is the improvement of the readout performance, allowing to read out the detector at 50 kHz of PbPb hadronic interactions without dead time.



The continuous readout mode without dead time is very challenging for the ZDC in Pb-Pb collisions due to EMD processes
-> resulting trigger rates of ~2.5 MHz

ZDC readout Upgrade

The solution identified to read the ZDC in continuous readout mode is based on **FMC digitizer ADC_3112 IOxOS** (12 b, 1GSps) combined with the use of FPGA. The **Carrier is the IFC_1211 IOxOS**.



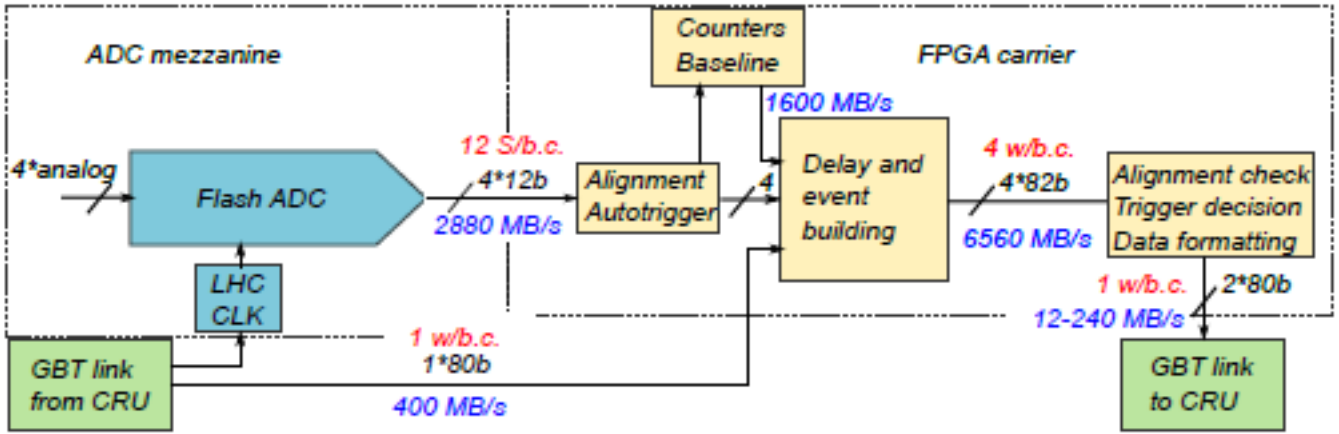
Carrier

	FMC ADC_3112
sample rate (MSps)	900 (1000)
resolution depth (b)	12
module price (KCHF)	5
channel number	4
input coupling	DC
input voltage (Vpp)	500 mV
enob ~1GHz (b)	9,8

FMC digitizer

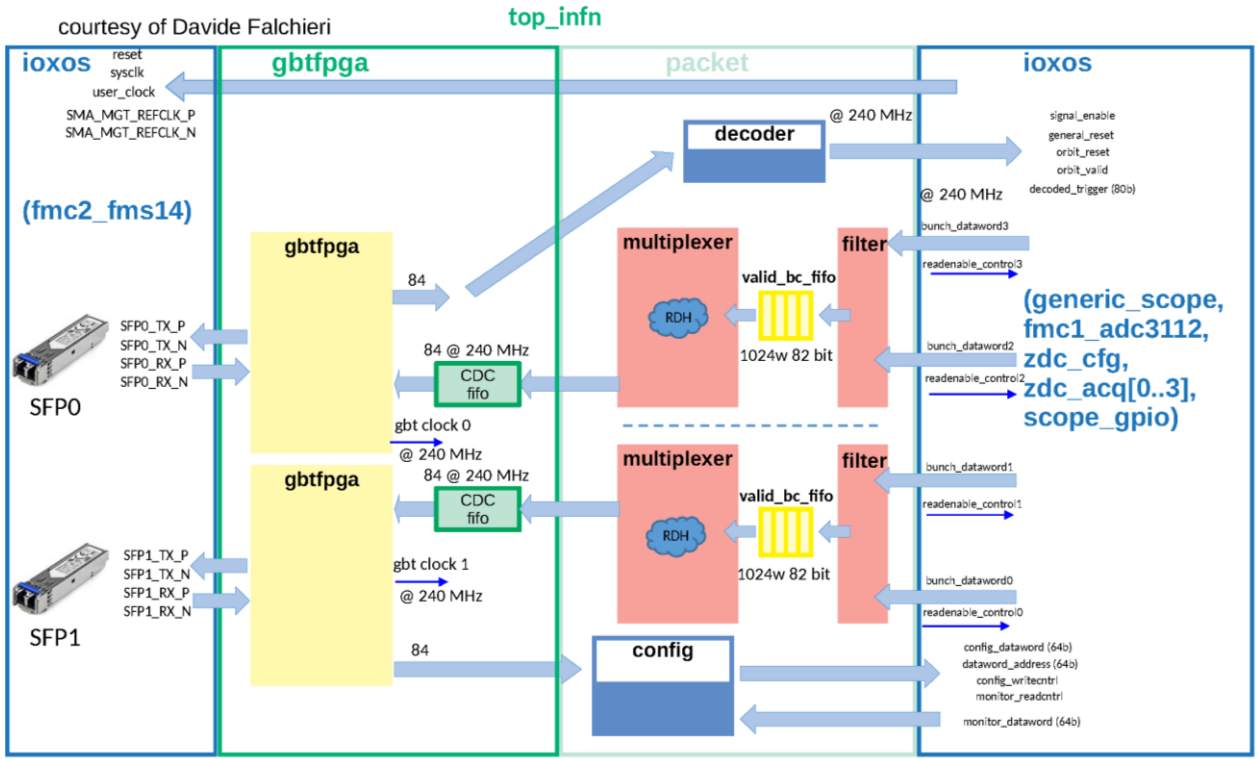
Equipped with two ADCs ADS5409 (Texas Instruments)

Firmware Architecture



The logic is working at ~240 MHz (6 times larger than LHC frequency).
GBT link from CRU provides commands to configure electronics and readout modes, start/stop commands, synchronization signals, orbit and bunch crossing (b.c.) counter…
Clock recovered from the GBT link used to synchronize the clock of the ADC.
Digitizer data are aligned with the b.c. and autotrigger algorithm is applied -> if satisfied the bunch is flagged for acquisition
Ring buffer delay used to synchronize the digitizer output with trigger information -> end of synchronous stage
A FIFO divides the synchronous world from the asynchronous one
Final selection algorithm: check of data stream alignement, check of autotrigger condition or presence of ALICE trigger, data formatting…
GBT link to CRU transmits triggered bunch crossing (3 GBT words) + previous b.c. for pedestal estimation (3 GBT words)

Current status of INFN firmware



Implemented in ZDC firmware:
GBT FPGA firmware + dual clock fifo (ClockDomainCrossing) , Data Packet Manager (multiplexer, filter, fifo, trigger decoding)
To be implemented: hardware configuration, already simulated in standalone mode

Attivita' Upgrade

2020-2021

-Luglio/ottobre 2020 -> primi test in hardware dell'implementazione di 2 links GBT tra carrier e CRU.

-Fine Ottobre 2020 -> catena di readout completa a Torino (FLP, CRU, LTU) e inizio integrazione dei 2 firmware (IOXOS+INFN).

- -IOXOS rilascia nuovo firmware e progetto di simulazione ModelSim (test bench installato a Torino)
- -Passaggio da clock generato sulla transceiver card a clock recuperato dal GBT
- -Inserimento di una dual clock FIFO (ClockDomainCrossing) prima della porta TX del GBT
- -Inserimento decodifica triggers ricevuti da CRU e predisposizione del packetized readout
- -Configurazione della LTU che permette di emulare i diversi trigger di ALICE

Prossimi passi

-Test stabilita' del link GBT con attuale schema di clock.

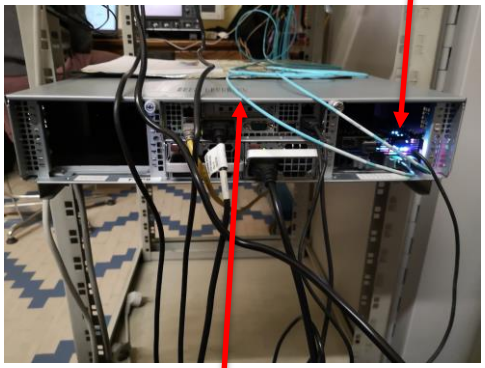
-Messa a punto della gestione di eventuali errori e eventuale data loss e gestione del flusso di informazioni dalla CRU al FEE sul link GBT (configurazione dell'elettronica).

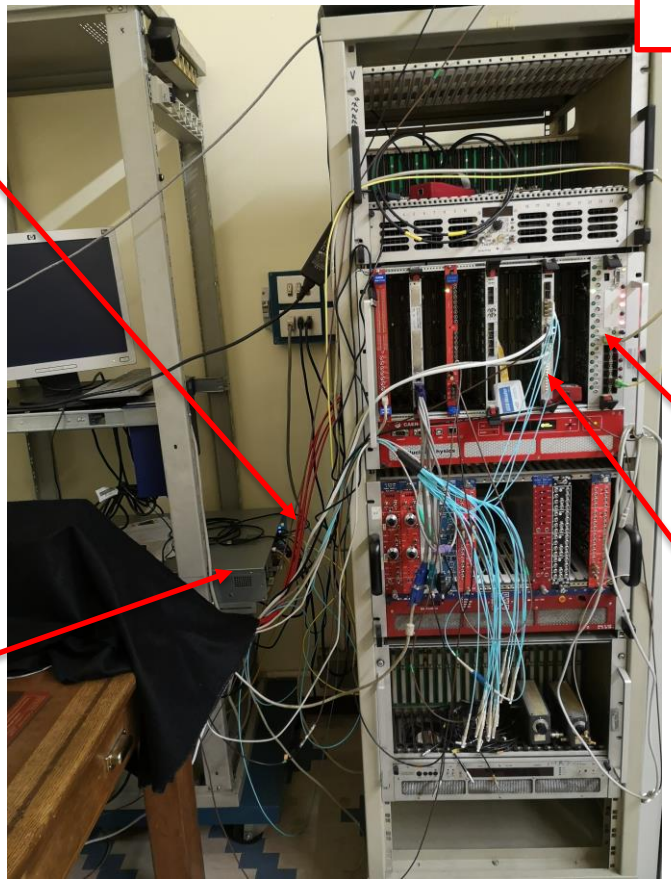
-Nell'autunno-inverno 2021, con una prima versione di firmware funzionante, prevediamo l'installazione del nuovo readout e l'inizio del suo commissioning al Cern (l'attuale scenario prevede il termine di LS2 il 21 Febbraio 2022).

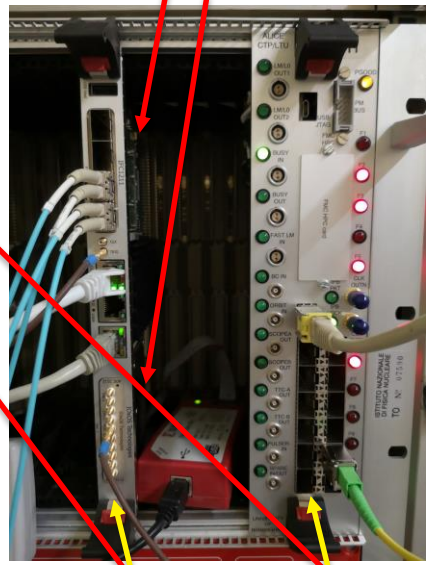
Prevista nel 2022

Continuazione del commissioning in laboratorio a Torino e al Cern del sistema di readout e sua messa a punto con fascio di protoni in modalita' standalone (lo ZDC e' previsto entrare in misura nelle collisioni PbPb a fine 2022).

Torino lab







CRU

FMC2 transceiver
fms14

FMC1 digitizer
ADC3112

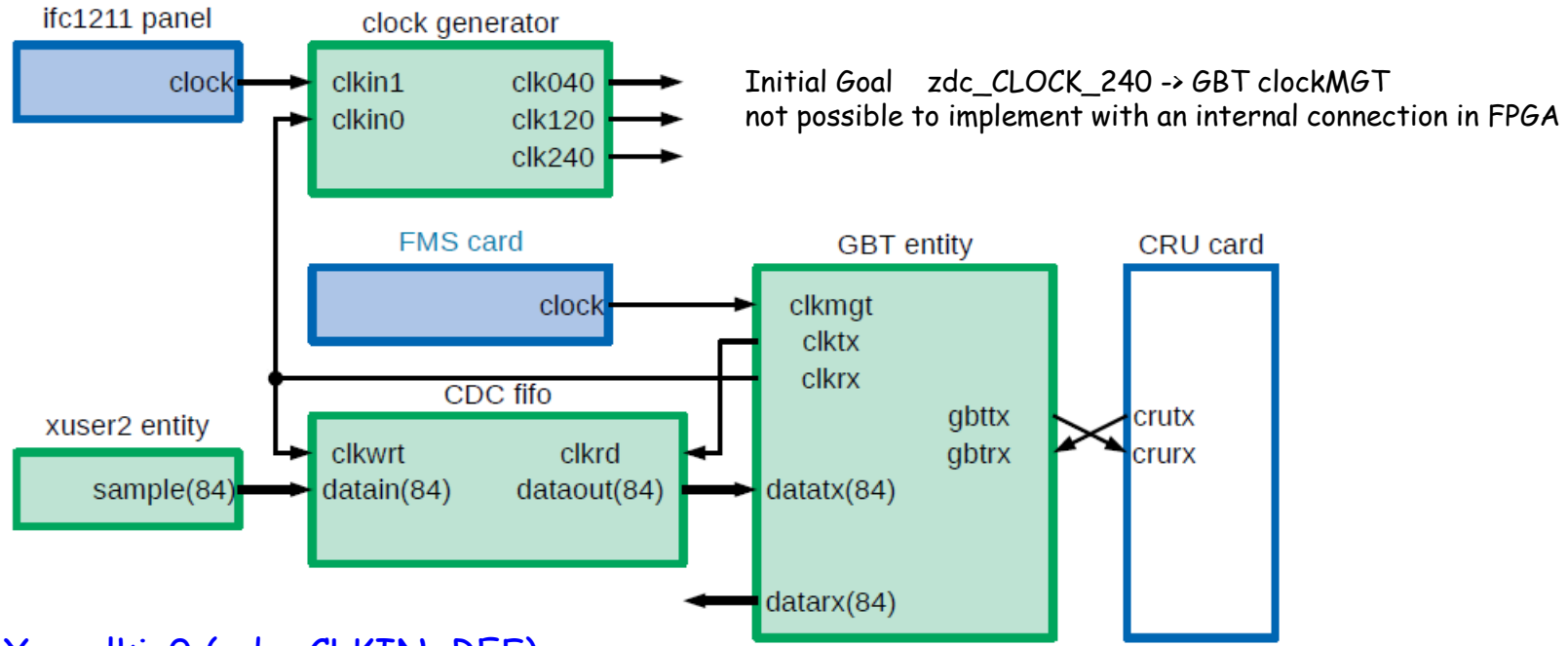
FLP

Ifc1211
Carrier

LTU

Clock Scheme

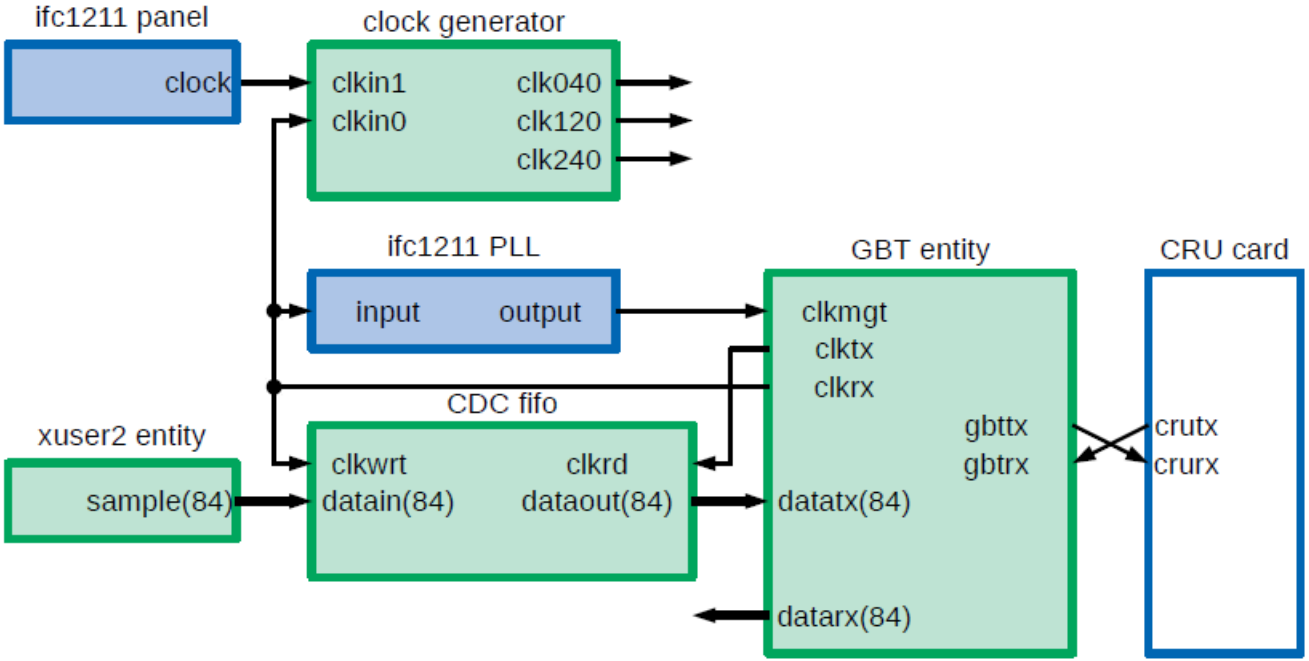
The logic is working at 240,47 MHz
Clock from fms14 card oscillator -> GBT clockMGT
-> dual clock fifo (ClockDomainCrossing) needed in order to cross the clock domain



GBT clockRX -> clkin0 (zdc_CLKIN_REF)

Alternative Clock Scheme

IOXOS proposed a small component modification of IFC_1211 carrier
-> change the VCXO from a 100.0 MHZ to 100.197 MHZ that would allow to have an external clock source.
The modification would open up the possibility to loop with the recovered clock.



If we will have problems of stability of the GBT link with the present clock scheme this seems to be a good solution.

Manutenzione

Attivita' 2020-2021

Causa delle limitazioni covid19 non e' stato possibile terminare l'attivita' legata al rinnovo dell'elettronica di controllo delle piattaforme dei calorimetri adronici, che richiede la presenza al Cern. L'attivita' e' ripartita nella primavera 2021 e si prevede di ultimare la programmazione PLC e la configurazione dei driver entro l'estate.

Prossimi passi

-Sostituzione dell'elettronica nei 2 tunnels di servizio LHC (side A e C) e e il suo successivo commissioning movimentando le piattaforme.

-Rimontaggio e allineamento del calorimetro elettromagnetico ZEM nel nuovo mainframe di ALICE antistante le porte di L3 (in corso).

-Riaccensione dei calorimetri ed eventuali interventi nel caso di problemi.

Attivita' prevista 2022

-Eventuale continuazione attivita' relativa a rinnovo dell'elettronica di controllo delle piattaforme dei calorimetri adronici;

-Manutenzione ordinaria delle piattaforme ZDC ed eventuale sostituzione di PMT nel caso si evidenziassero dei problemi.

Sviluppo temporale: entro la chiusura del tunnel LHC in vista di run3 (l'attuale scenario prevede il termine di LS2 il 21 Febbraio 2022) e nei periodi di technical stop dell'acceleratore.

ZDC platforms

ZN and ZP are fixed on movable platforms controlled via ALICE DCS

- Vertical position adjusted to follow crossing angle
- Garage position (20 cm lower than the beam plane) during injection

New servo motor controllers

Replacement of the servo motor controllers (PLC + Masterdrives) for the 4 ZDC platforms necessary since the old ones are no longer supported by Siemens.

The PLC test environment is in Meyrin and because of software licenses limitations and CERN's security policies, it was not possible to move it to Torino.

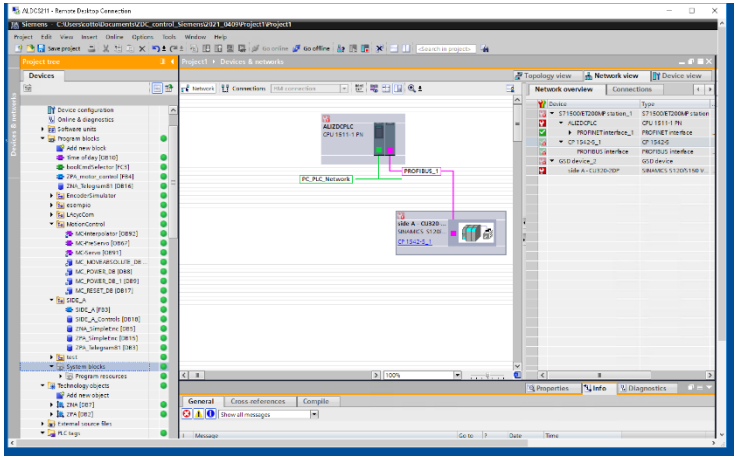
Due to covid19 limitations this activity was slowed down since it would require the presence at CERN for the test phase in real environment.

New servo motor controllers

The new system is configured and the plc programming will be finalized in few days. Development of the debug user interface is still in progress; it will be used for testing purposes when the PLC and the motor drivers will be installed.

Next steps

Complete the development of the debug user interface
Replace in the LHC service tunnel side A the old system with the new hardware
Test the new environment extensively
Duplicate the "A-side" system on the "C-side" and test the whole system
Compare the measured position by the new system with the nominal beam position
Update the user interface on WinCC
Test the integration of the new control system with ALICE's DCS system



O2 Software Activities

ZDC

TASK	STATUS
Geometry	Done
Hits and digits	Done
Pile-up	
Digits to raw	Done
Raw to digits	Done
Reconstruction	In progress
Digits to CTF	Done
CTF to Digits	Done
Read & decode data on FLP	
Electronics channel mapping	
QC	In progress
Calibration	In progress

Introduced protection for missing time frames (to be merged)
First version of reconstruction has been inserted in O2:

- Reconstructed data stream
- TDC (arrival time and amplitude)
- ADC with average pedestal subtraction

Development of event-pedestal correction is in progress
Pile-up detection and correction has been started

The QualityControl (QC) development machine has been configured
The code concerning the raw data histograms is being written
Histograms defined for reconstructed data
Histograms defined for real-time monitoring of the detector for both experts and shifters
Development raw data Task and Checker with simulated data on going

Milestones 2020

30/9/2020 -> 31/12/2020

ZDC Upgrade - Test in laboratorio delle 8 coppie FMC+Carrier

31/12/2020 -> 50% Causa restrizioni Covid, solo una parte dei test previsti è stata effettuata

30/6/2021 -> 100 % Raggiunta. Effettuati test di funzionalità di base e di accesso ai componenti

31/12/2020

ZDC Upgrade - Installazione e inizio commissioning del sistema di acquisizione al CERN

31/12/2020 -> Rinviata al 2021 a causa delle restrizioni Covid

30/6/2021 -> Rinviata al 2021 a causa delle restrizioni Covid

Milestones 2021

30/6/2021

ZDC Upgrade - Installazione e inizio commissioning del sistema di acquisizione al CERN

30/6/2021 -> 0% Problemi nell'implementazione dello schema di clock previsto, legati all'utilizzo di GBT in modalità non standard (GBT-FPGA sia dal lato FEE come sorgente e sia dal lato DAQ come ricevitore). Soluzione in fase di test. Identificata eventuale alternativa che richiede piccola modifica hardware -> 31/12/2021

31/12/2021

Commissioning del nuovo readout all'interno della struttura di controllo O2 (Online-Offline) dell'esperimento ALICE sia in triggered che in continuous mode

30/6/2021 -> 0% Legata alla milestone precedente.

Milestones proposte 2022

31/10/2022

Commissioning con fascio in parallelo alla presa dati p-p

31/12/2022

Partecipazione presa dati Pb-Pb

Richieste specifiche ZDC 2022

Missioni estere ZDC upgrade
2 KE per contatti con ditta IOxOS
9 KE per commissioning del sistema di readout al Cern (1 mese x 2 persone)

Licenze -> 1 KE
per licenza Xilinx Vivado

M&OB ZDC 2022 -> 16 KCHF (cambio 1,08 CHF/Euro) -> **15 KE**

M&OB ZDC (KCHF)

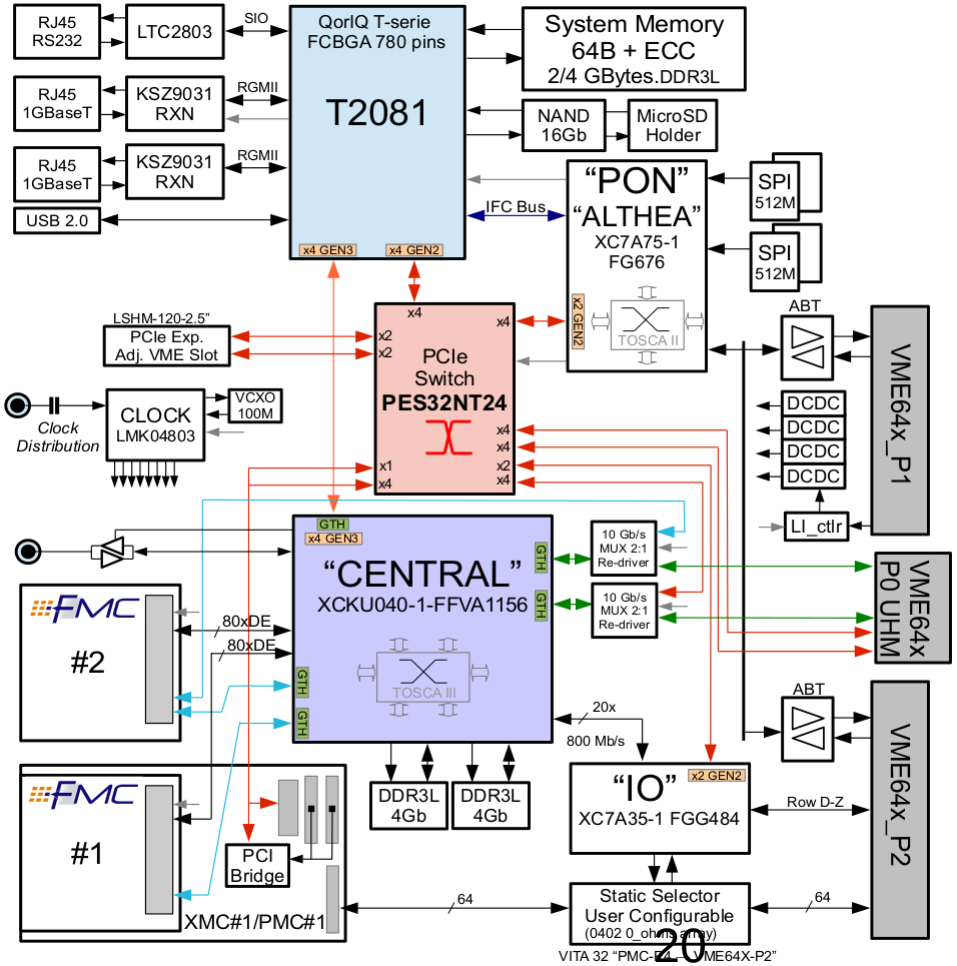
Ref.	Description	2022	2023	2024	2025
A01	Mechanics	0,5	0,5	0,5	0,5
A02	Gas Systems				
A03	Cooling Systems				
A04	FEE spares	**1,5**	1,5	1,5	1,5
A05.1	Standard Electronics LV/HV PS				
A05.2	Standard Electronics Crates				
A05.3	Standard Electronics R/O modules	1	1	1	1
A06	Controls (DCS & DSS)				
A07	Sub-Detector spares				
A08	Areas				
A09	Communications	**1**	1	1	1
A10	Store Items	6	6	6	6
A11.1	Technical Manpower @ CERN: Industrial Support				
A11.3	Technical Manpower @ CERN from Collaborating Institutes	**6**	6	6	6
Total		16	16	16	16

BACKUP

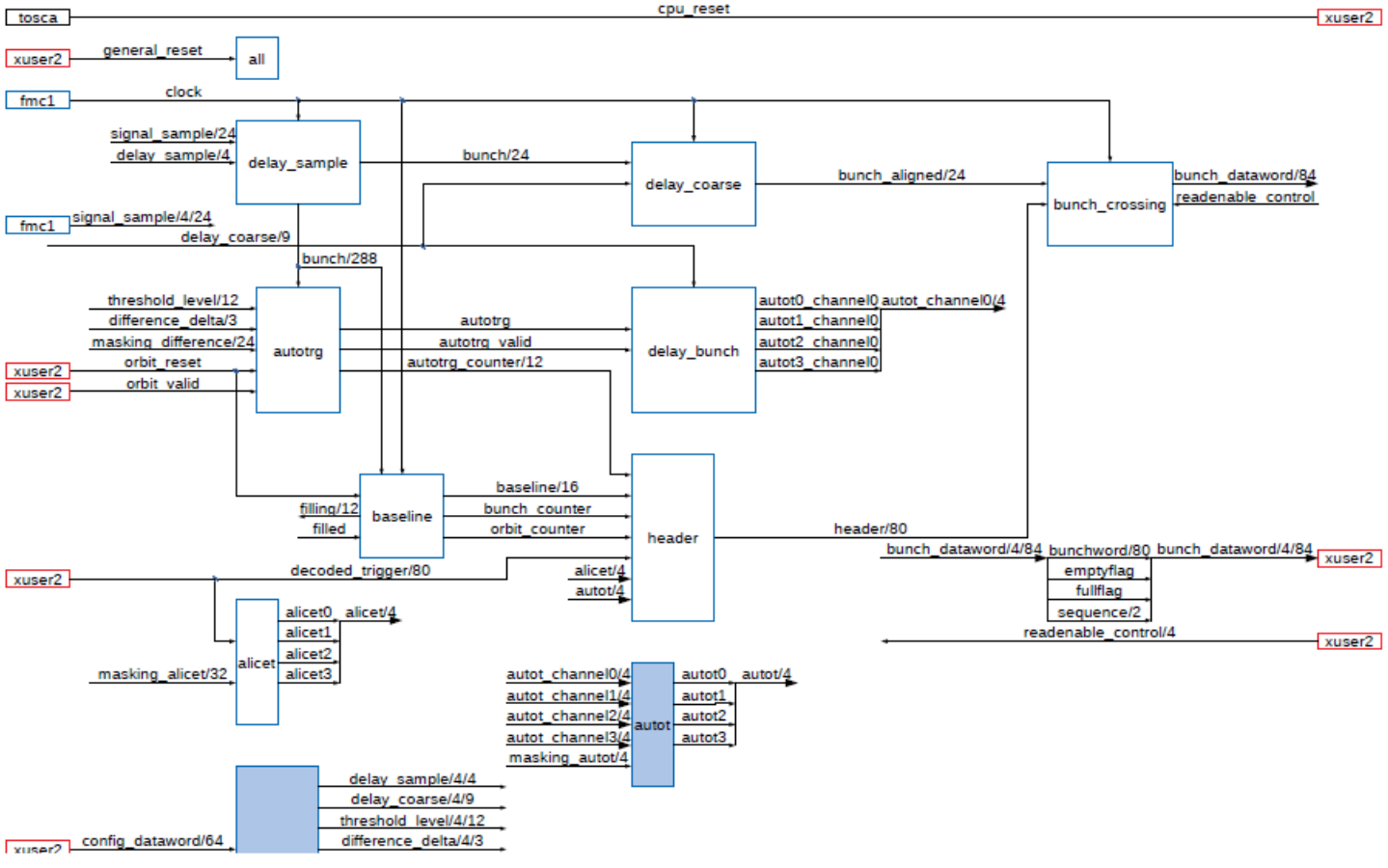
IOxOS IFC_1211 Carrier

Key Features

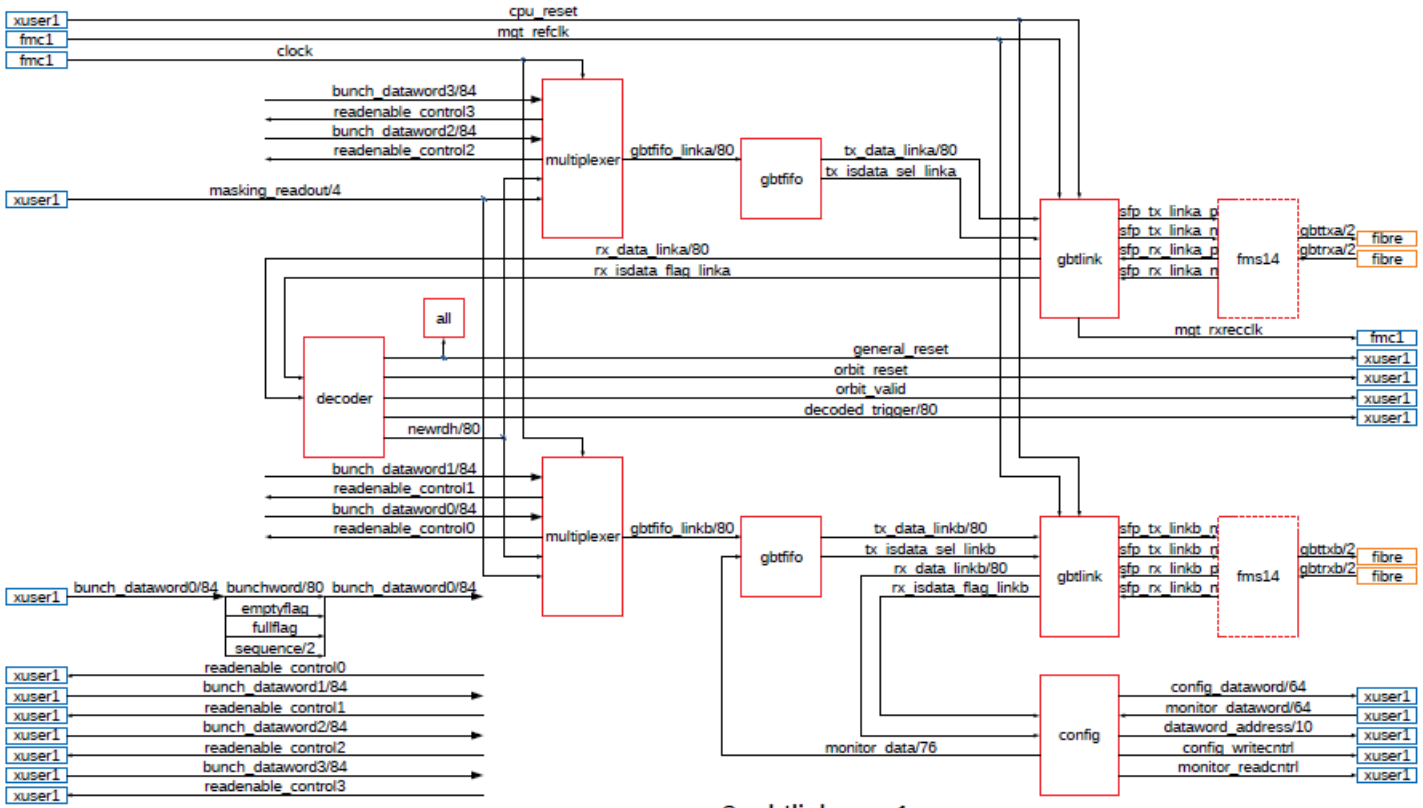
- 6U VME64x Single Board Computer
  - Freescale PowerPC e6500 computing core
  - QorIQ T2081 1.4 (1.8) GHz
  - 2 / 4 GBytes DDR3L System Memory
  - NAND Flash, NOR Flash
  - Dual 10/100/1000 BaseT Ethernet
  - Single RS232
- PCIe GEN2 24-port switch PES32NT24
  - Eight NTB ports
  - Multicast support
  - Embedded DMA Controller
  - SSC / CFC clocking
- Single VITA 42.3 XMC/ PMC Mezzanine
- Dual VITA57.1 HPC FMC Mezzanines
- Quad/Octal Tx/Rx 12.5 Gb/s JESD204B
- UHM VME P0 extension (7 Gb/s)
- VME64x Master/Slave with 2eSST support
- Thermal and Power supplies monitoring
- Xilinx Kintex UltraScale CENTRAL FPGA
- Xilinx Artix-7/ FF484 IO FPGA
- Powered by TOSCA III FPGA Design Kit
- Linux / EPICS / VxWorks BSP



XUSER1 (IOxOS)



XUSER2



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