EMC update, status and request

C. Cecchi

OUTLINE:

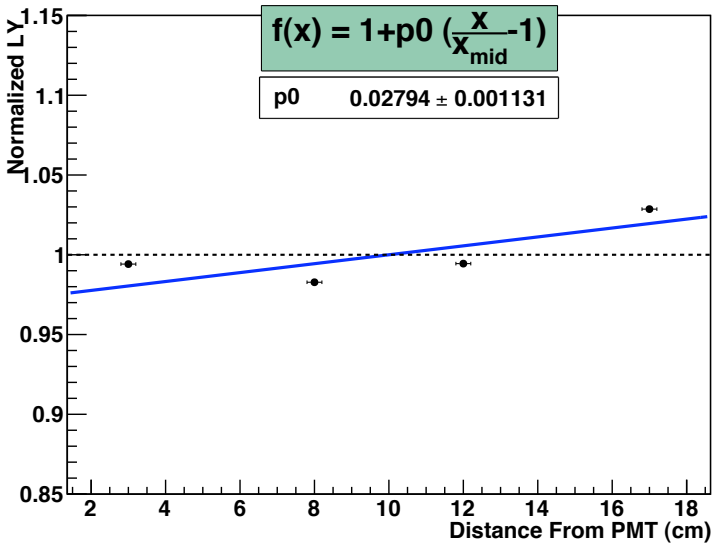
- **crystals**
- **mechanics**
- **electronics**
- **test of the electronics at BTF**
- **plans**
- **request**

CRYSTAL STUDY

Perugia INFN

St. Gobain: 12 crystals received for the beam test

- Metrology to check dimension ok, new production within +0, -200μm (goal +0, -100 μm)
- LY measurement ok, 1000 pe/MeV
- Uniformity very preliminary measurement, very good



SIPAT: new production (3 samples L10-L11-L12) has just been tested

- Dimensions OK (improvement w.r.t. L8-L9)
- L10 absorption problem (will return to SIPAT)
- L11-L12 good transmittance, LY and resolution

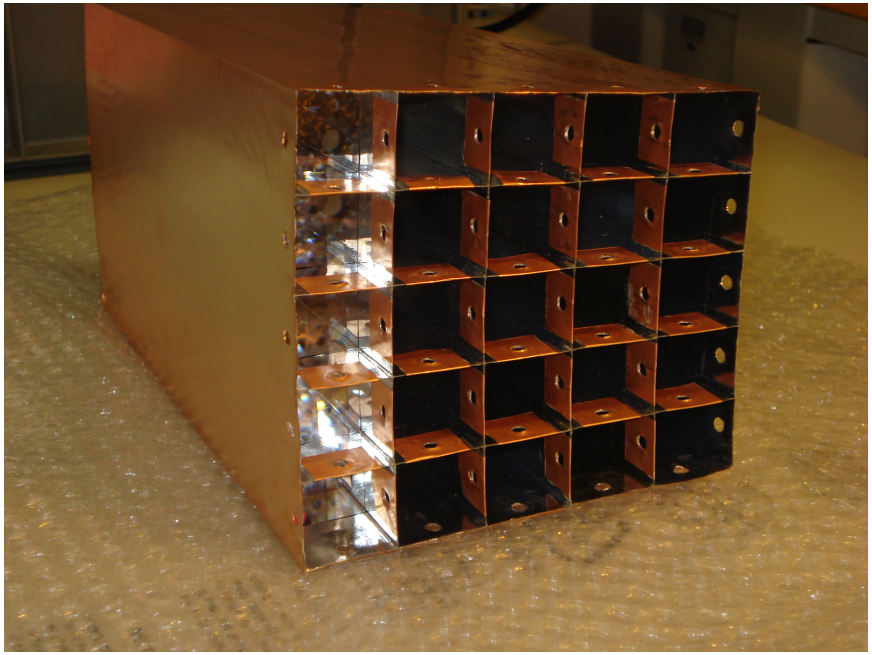
After resolving absorption issue their LY is increased by 35%
Improvement of the LY uniformity is still necessary
Schedule is to be ready for October TB

NEXT:

exchange SIPAT crystals with St. Gobain ones to compare results (Perugia – Caltech should agree on set of measurements and procedure)

We have started in Perugia the measurement of LY uniformity of all the samples

- Prototype structure for BT ready
- Development is ongoing for the whole structure
  - Production method working
  - Precision within tolerances



What remains:

- Cost estimate in view of the 180 modules of a full endcap is available (1M euro)
- production schedule 1 year
- optical performance (to be studied with single cells)
- structural behaviour (module elastic characterisation, FEA of the support shell….)

We have ordered a second prototype structure for stress test at CERN

Measurement of single crystals in a single cell is starting to test LY uniformity →
will allow to study optical properties of the material

We are well on the way towards the construction of the whole structure.

READOUT, VFE, DAQ

Final choice between PiN diodes (as in the Barrel) and APD's has not yet been done:

- **PiN would require intermediate step with PMT during uniformity measurements**
- **APD's strong temperature dependence**

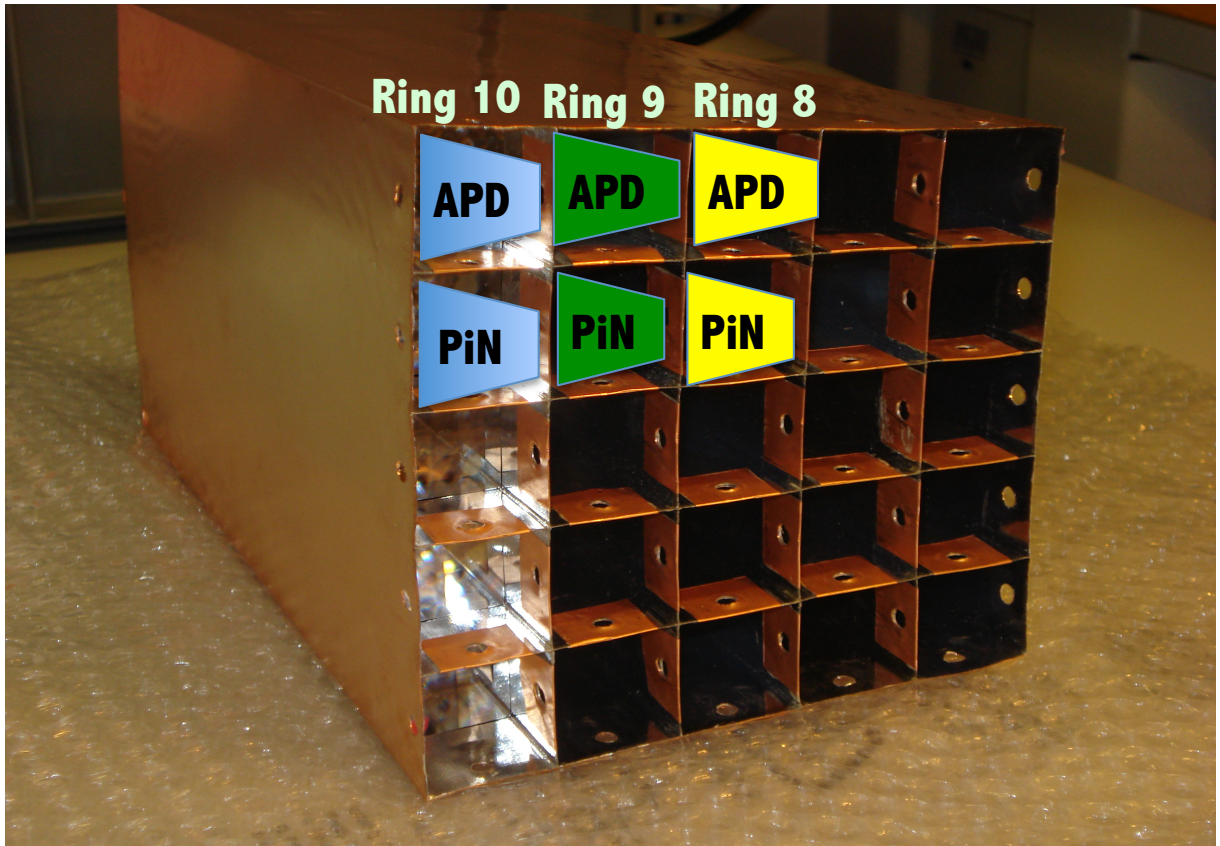
New: neutron induced signal in APD's worse by a factor of 10 in PiN than in APD's

To solve this problem it would be sufficient to read separately the signal from photodetectors and compare them, is it possible to do it also with PiN diodes?

Study if the signal (w.r.t. noise) at low energy is sufficient → we are going to test it in September.

VFE board delivered June 7th

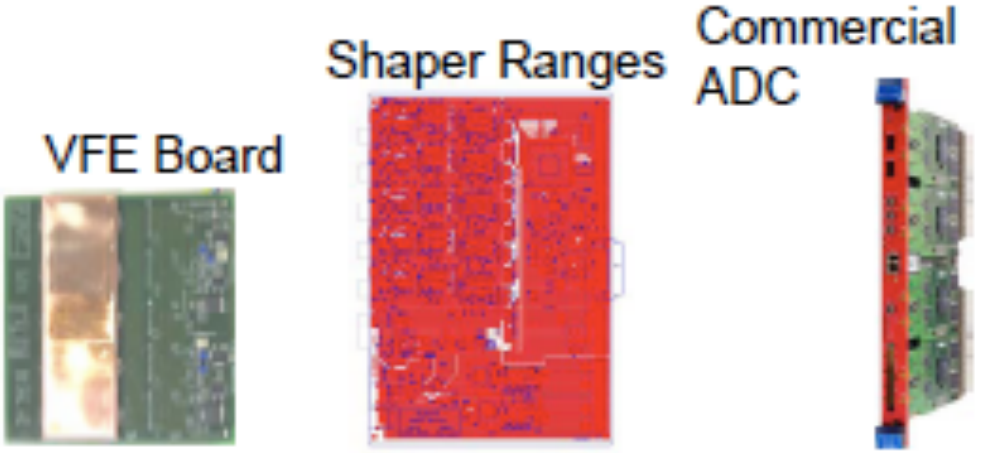
Test in lab + Frascati of these new electronics board has started June 21st



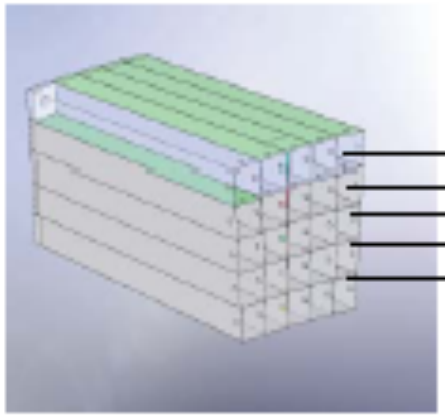
TEST OF THE VFE AT BTF JUNE 21st

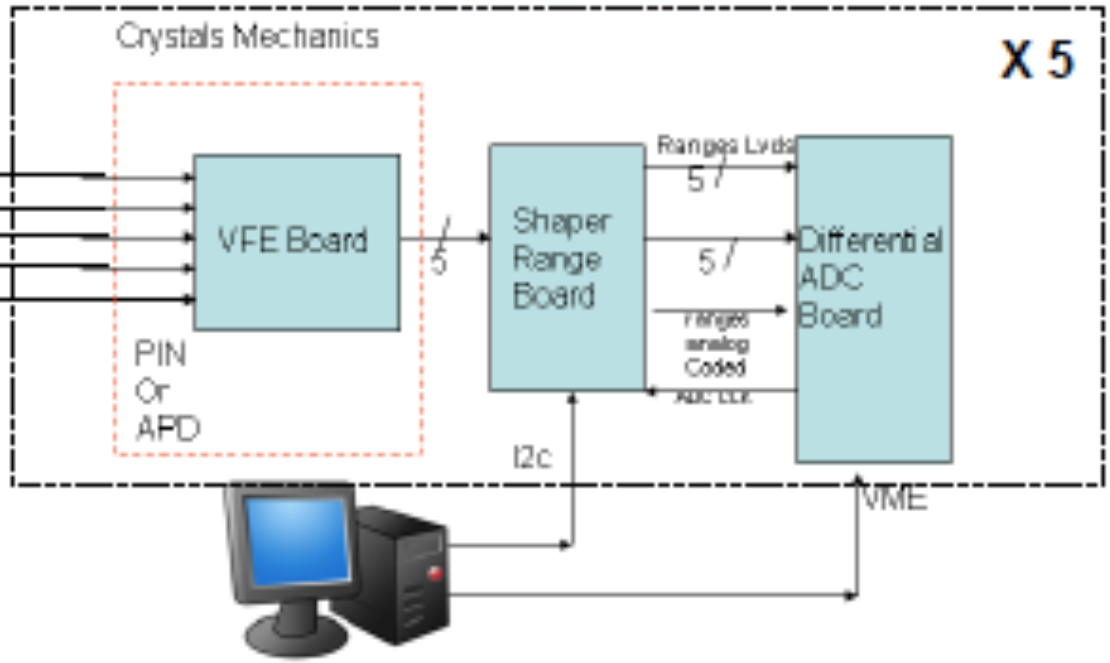
MANY THANKS to V. Bocci and A. Papi and people working with them in the shops for the effort they have put to have everything ready and functioning in a very short time!

ELECTRONICS READOUT USED IN FRASCATI



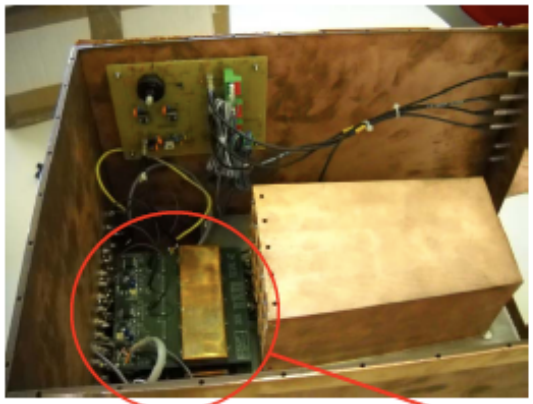
5x5 crystals

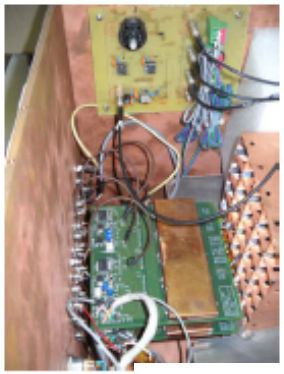




VIEW OF THE SYSTEM

Perugia INFN Istituto Nazionale di Fisica Nucleare

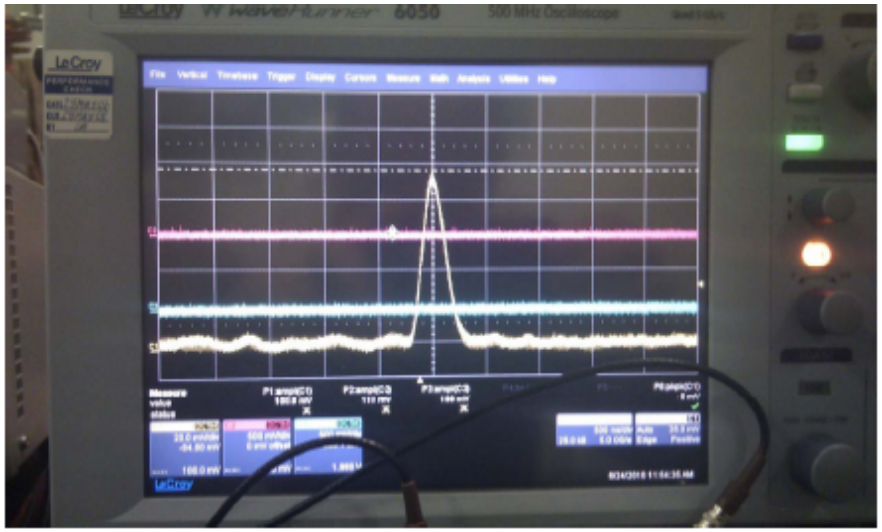


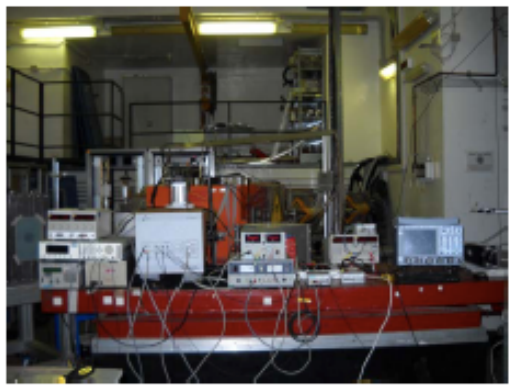


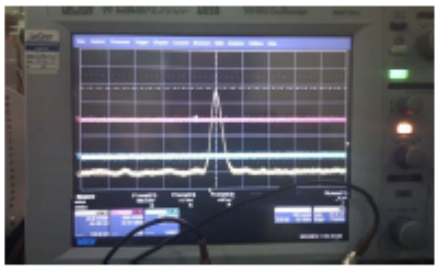
•VFE Up for PIN
•VFE Down for APD

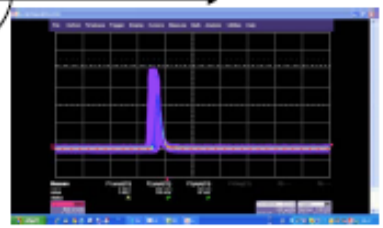
2 VFE boards connected to PiN and APD's, signal goes to the shapers. Range boards where not available, they are now in Rome for test.

NOISE LEVEL LESS THAN 20 mV









WHERE WE ARE.....

- VFE boards received and tested (refer to next slides for results)
  Small optimization is needed in the cabling and shielding, it has started last week.
- VME has not been tested in Frascati, boards have been delivered and tests have started and will continue during July.

- Software for the VME has to be written (A. Rossi with some help in Rome1 (V. Bocci) + new collaboration with Rome 3 (P. Branchini et al.))

A very important discussion has been started, triggered by the results on the background study in the barrel, due to the long decay time of the CsI(Tl). We need a detailed study based on simulation to understand the best solution for the timing of the EMC to avoid pile up beteween signal and bckg.
DETAILED STUDY OF SHAPING TIME AND TIME WINDOWS.

TEST AT BTF JUNE 21st – 25th

6 crystals type 8, 9 and 10
3 with PiN readout
3 with APD's

APD's have been monitored in temperature with 3 sensors
VFE board has been tested

Ring8	Ring9	Ring10
PiN3	PiN2	PiN1
APD3	APD2	APD1

- **Only 3 shapers (100ns) available**
- **Two different configuration:**
  - **PiNs connected to shapers**
  - **APDs connected to shapers**
- **For each configuration are acquired data at 500, 400, 300 and 200 MeV**

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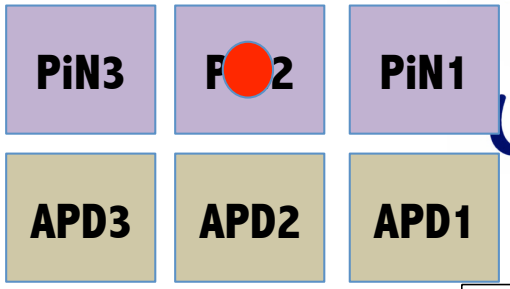
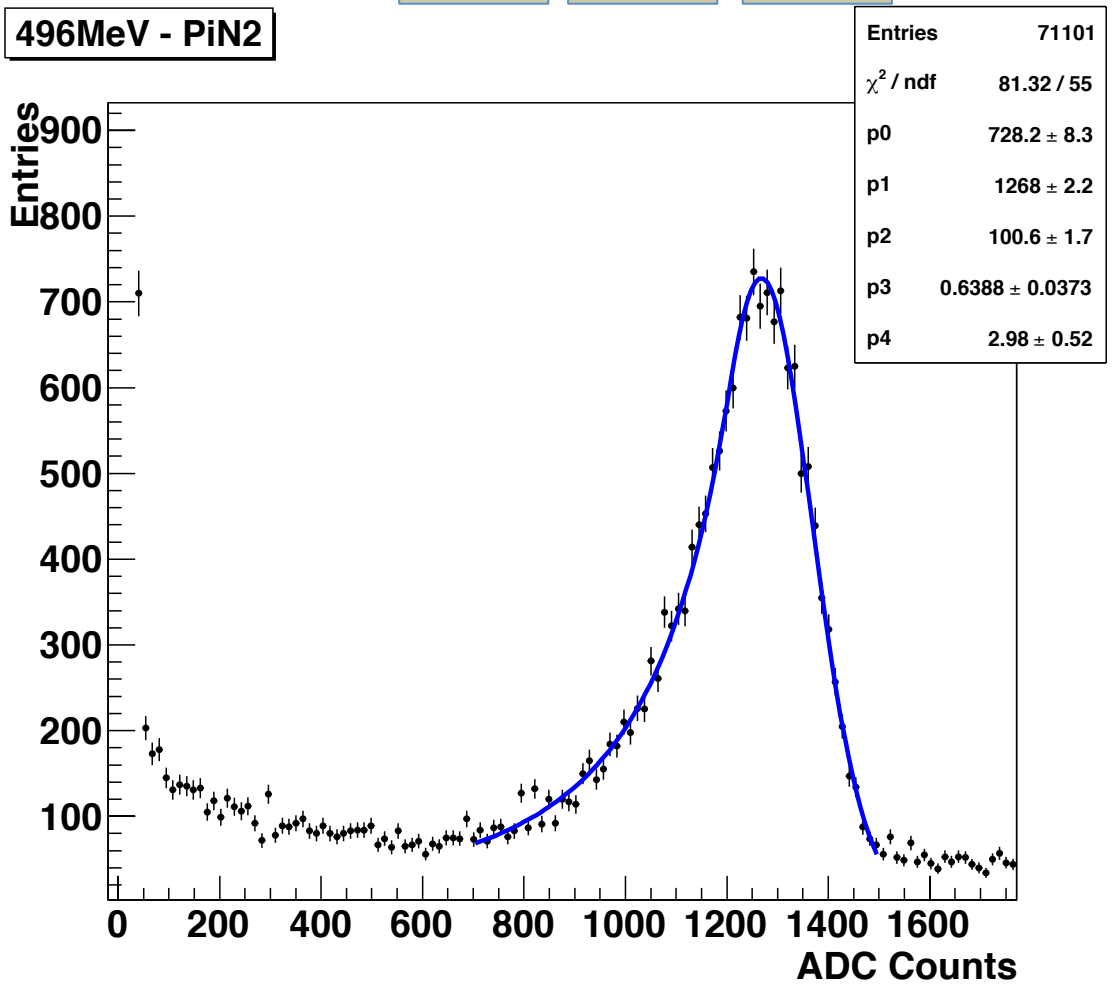
Example: 500 MeV (PiN)



- **CrystalBall fuction:**
  - p1: Mean
  - p2: Sigma
  - p3: Alpha
  - p4: N
- **Resolution:**
  - Using Sigma: 8.0±0.2 %
  - Using FWHM/2.36: 8.9±0.2 %



TEST AT BTF JUNE 21st – 25th

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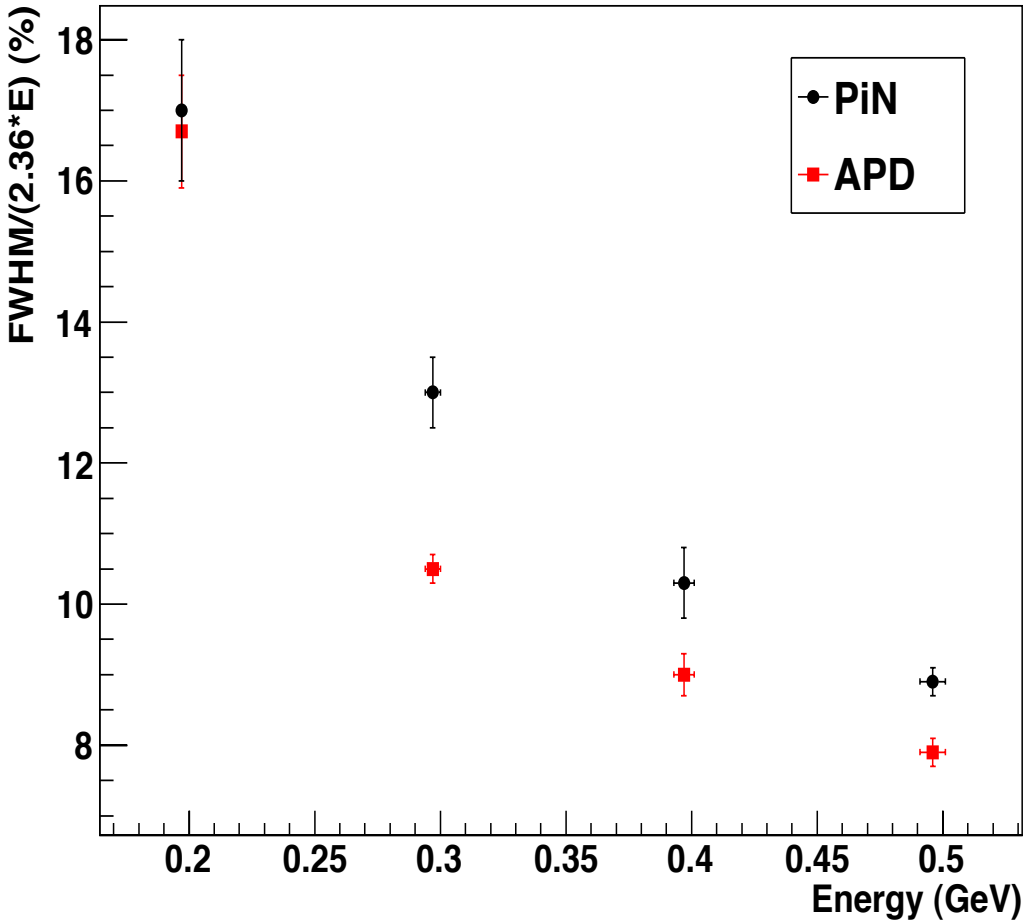
APD vs PIN

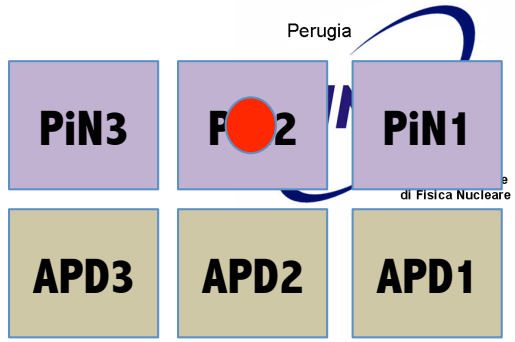
Resolution



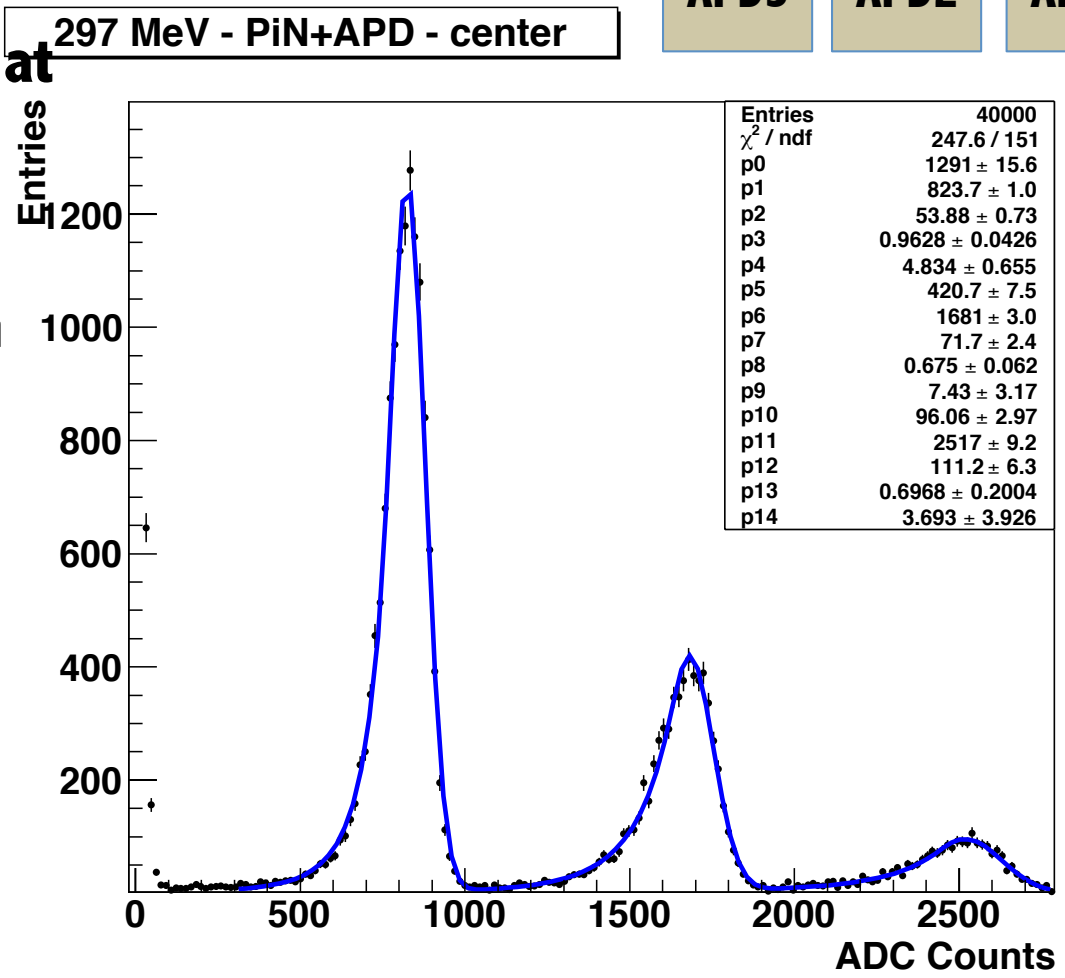
- About the same resolution for PiN and APD
- Difference is due to the fact that for APD beam is centered better than for PiN

TEST AT BTF JUNE 21st – 25th

Example: 300 MeV (PiN+APD)

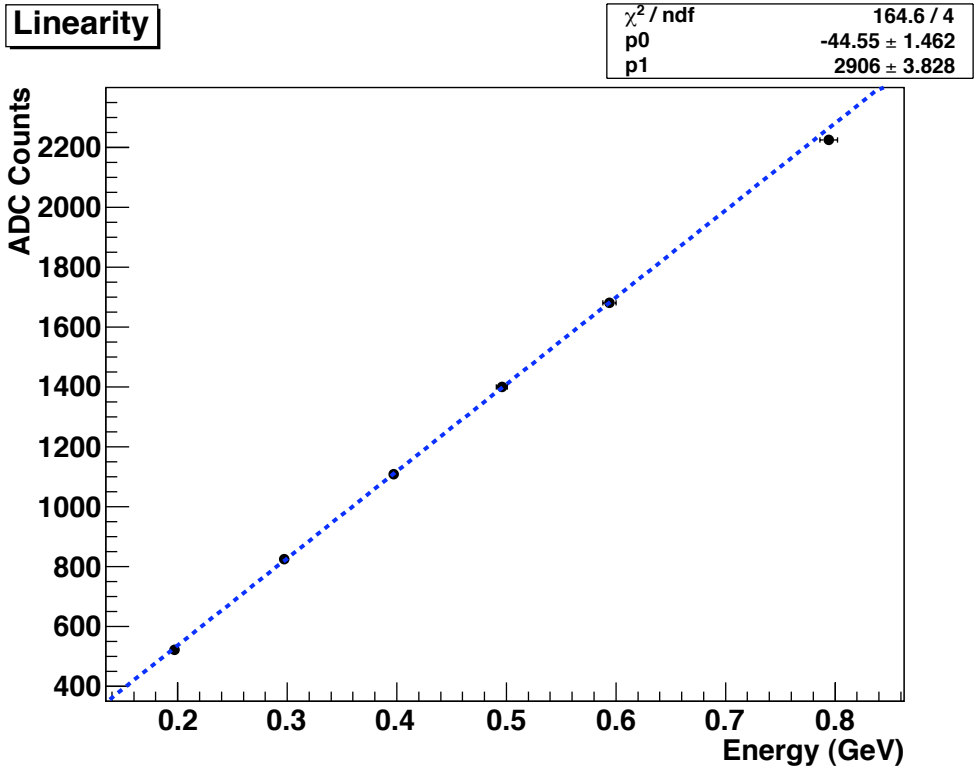


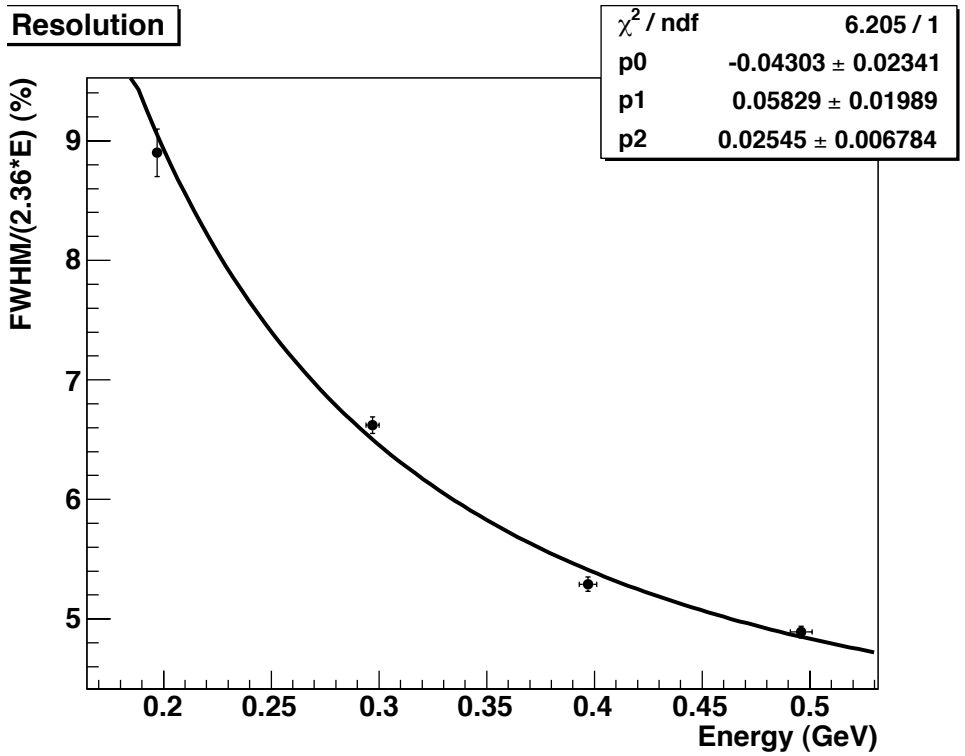
- **Improvement in resolution at all energies**
- **We may use also 2 electron events, more range**
- **Resolution:**
  - **1 e- : 6.62±0.07 %**
  - **2 e- : 4.64±0.17 %**



TEST AT BTF JUNE 21st – 25th

Linearity and resolution





SHORT TERM PLANS

THE GOAL is to be ready with 25 channels of the new electronics for October BT

- Test LY and uniformity of all the cyrstals, exchange with Caltech on type 8 (July)
- Optimization of the VFE (July)
- Test of VME board in lab (to be finished by end of July)

- Modify the front panel for the 25 channels (August)
- Cabling of the 5 boards (August)
- VME software (August)

- Test of VME + cabling + integration of the system (September)

SBLOCCO SJ 2010

	PERUGIA	ROMA1	ROMA3
MI			
	VISITE RIBA 3 keuro		
	TEST BEAM 4 keuro		
ME			
	1 meeting USA 4 persone 10 keuro	TB CERN 7.5 keuro	TB CERN 3 keuro
	TB CERN 3 settimane 17 keuro		
CONSUMI			
	Elettronica + CsI per test 2 keuro		
INV			
			Process. VME 4 keuro

ROMA 3 è una nuova richiesta dopo il loro ingresso in superB e partecipazione al TB al CERN per il DAQ

PLANNING 2011 (PERUGIA)

Continue developing on electronics:

- **background suppression**
- **neutron signal in APD's and PiN's**
- **developing boards in view of the final micro ASIC for the VFE**

Development of analog and digital components of the boards.

Starting procurement of crystals

Start construction of the mechanical structure

Finalize TDR

Convenership of EMC

PLANNING 2011 (ROMA1)

Elettronica EMC (Coordinamento e LAB elettronica):

- **Sviluppo digitizzazione (schede)**
- **Sviluppo pretrigger (sommatori, link ottici)**
- **Schede con differenti shaping times**
- **Ulteriori PIN/APD**

Cristalli EMC:

- **Test con differenti cristalli (CsI)**
- **Scelta e validazione produttori**

ANAGRAFICA

PERUGIA

•	Claudia Cecchi	RU	30% Resp. Loc. [Conv. EMC]
•	Pasquale Lubrano	DR	30%
•	Stefano Germani	art.23	40%
•	Elisa Manoni	Ass.	50%
•	Daniele Rinaldi	Ric	50%

2.0 FTE

+ tecnici Laboratorio Elettronica e officina meccanica

ROMA1

•	Faccini Riccardo	RU	30% Resp. Loc. [Conv. Spettroscopia]
•	Fernando Ferroni	PO	10%
•	Martellotti Giuseppe	DR	20%
•	Pinci Davide	Ric	20%
•	Auriemma Giulio	PO	20%
•	Bocci Valerio	Tecn	10% [Resp. Elettronica EMC]

1.1 FTE

+ tecnici Laboratorio Elettronica

RICHIESTE 2011

	Perugia (2FTE)	Roma1 (1.3 FTE)
MI		
	VISITE RIBA 3 keuro	PG ELETTRONICA 3 keuro
	ROMA ELETTRONICA 5 keuro	COLL. MEETING 2.5 keuro
	COLL. MEETING 3.5 keuro	
ME		
	1 MEETING USA 10 keuro	1 MEETING USA 7.5 keuro
	VIAGGI CRISTALLI 10 keuro	VIAGGI CRISTALLI 10 keuro
CONSUMI		
	SVILUPPO VFE 30 keuro	CRISTALLI 5 keuro
		ELETTR. 30 keuro
COSTR. APP.		
	CRISTALLI 470 keuro	
	MECCANICA 89 keuro	
	PROGETTO MECC. 24 keuro	

Stima costi VFE			
Sviluppo ing Circuito stamp VFE	1	9000	9000
costo attrezzatura	1	2000	2000
setup montaggio	5	800	4000
costo schede	5	400	2000
costo montaggio	5	350	1750
costo componenti	25	350	8750
Consumi vari in laboratorio		2500	2500
		Totale	30000

1 - Sviluppo del PCB circuito compatto a 6-8 layers
2 - Costo della attrezzatura (in ditta) per la realizzazione del PCB
3 - set up per il montaggio delle schede
4 - costo unitario di produzione del PCB VBFE
5 - costo montaggio dei componenti su una scheda
6 - costo unitario a canale dei componenti
7 - consumi vari per cavi, attrezzature ecc.

Stima costo Digitalizzatori	qty	costo unitario	costo totale
costo attrezzatura	1	1500	1500
setup montaggio	1	700	700
costo per schede	6	300	1800
costo montaggio	6	250	1500
stima componenti costo x ch	30	150	4500
		Totale	10000

Digitalizzatori commerciali			
Soluzione commerciale 25 ch	25	650	16250

Sviluppo pretrigger (sommatori, link ottici) – 10K			
costo attrezzatura	1	1500	1500
setup montaggio	1	700	700
costo per schede	4	300	1200
costo montaggio	4	250	1000
costo link tx	1	1500	1500
costo link rx computer	1	1500	1500
stima componenti costo x ch	30	50	1500
		Totale	8900

Costi shaping prototipi			
costo attrezzatura	1	1500	1500
setup montaggio	1	700	700
costo schede	10	40	400
costo montaggio	10	70	700
costo componenti	10	150	1500
		Totale	4800

PIN o APD	40	100	4000