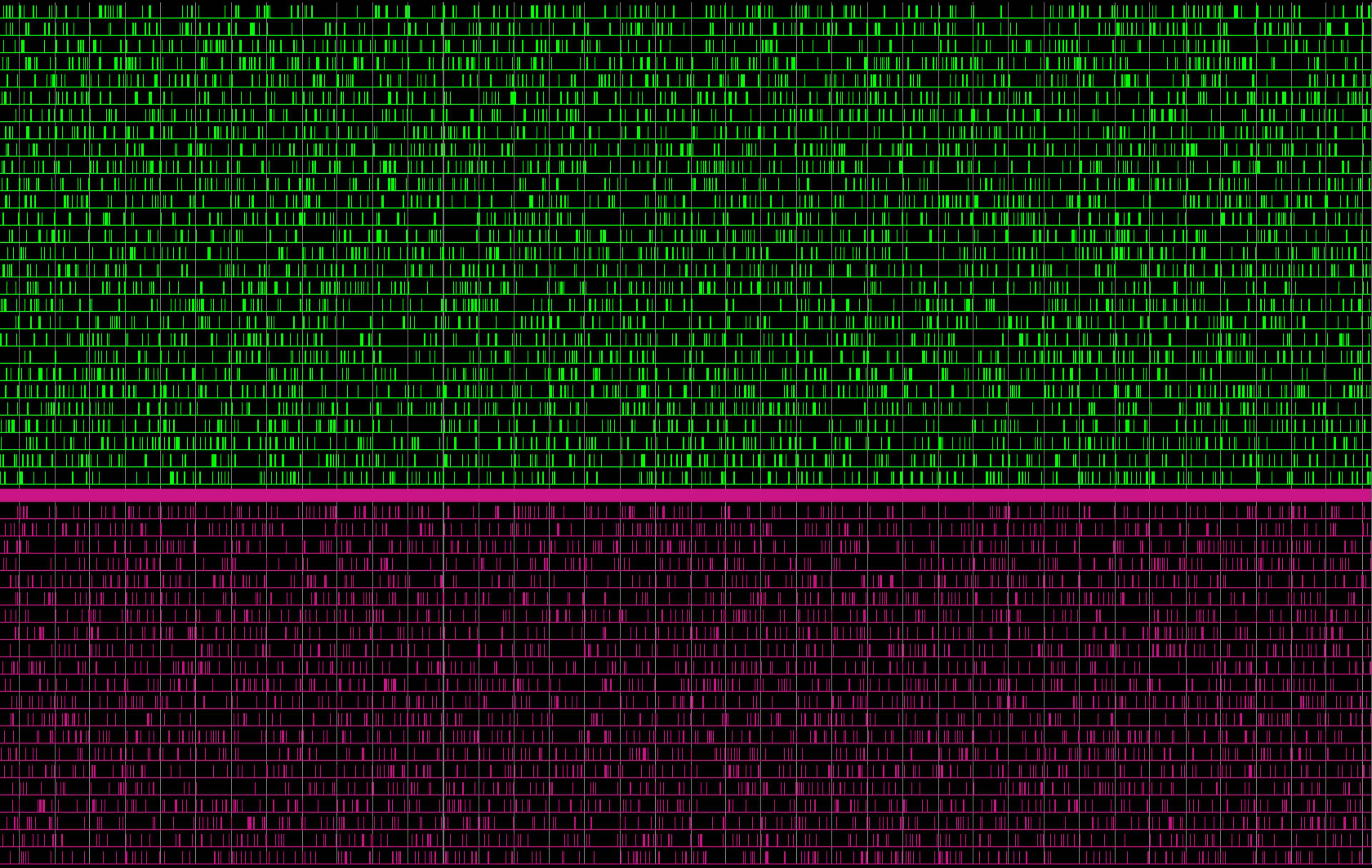
Simulation updates



2-07-2010 F.Giorgi

What’s new

- Matrix dimensions update:
  - 200x256 pixels (50x256 sub-matrices)
  - 50 um pitch

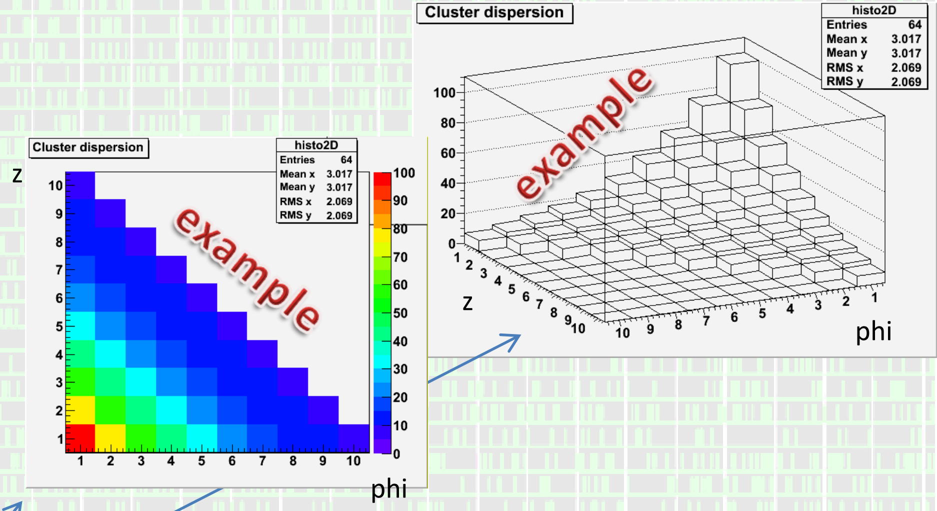
What’s new

- Matrix dimensions update:
  - 200x256 pixels (50x256 sub-matrices)
  - 50 um pitch
- Code optimization
  - Substantial: more robust concentrators
  - Formal: code maintenance

What’s new

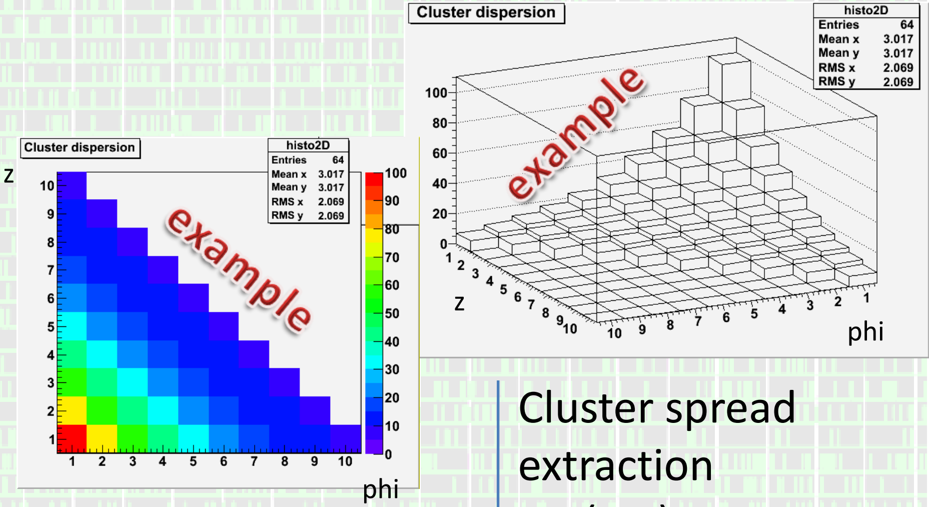
- Matrix dimensions update:
  - 200x256 pixels (50x256 sub-matrices)
  - 50 um pitch
- Code optimization
  - Substantial: more robust concentrators
  - Formal: code maintenance
- Monte Carlo generator
  - Rewritten from scratch
  - Now generation of clustered events
  - Knobs:

    - Cluster dispersion distribution in (z,phi)
    - Physical time resolution (test_clock), hit/miss thresholds =Global hit rate

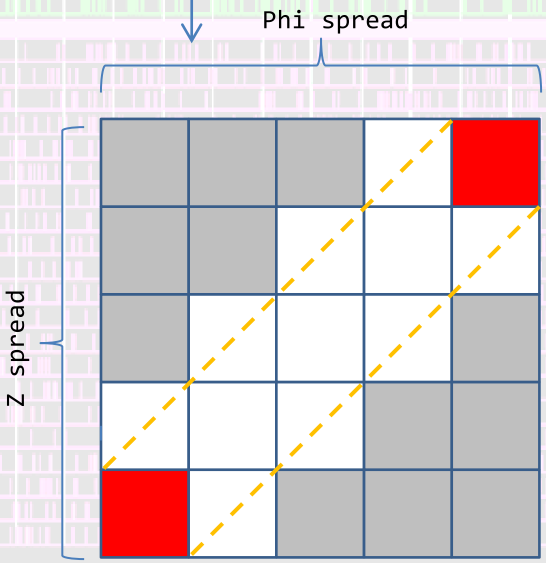


What’s new

- Matrix dimensions update:
  - 200x256 pixels (50x256 sub-matrices)
  - 50 um pitch
- Code optimization
  - Substantial: more robust concentrators
  - Formal: code maintenance
- Monte Carlo generator
  - Rewritten from scratch
  - Now generation of clustered events
  - Knobs:
    - Cluster dispersion distribution in (z,phi)
    - Physical time resolution (test_clock), hit/miss thresholds =Global hit rate
  - Arbitrary pattern extraction by geometrical rules

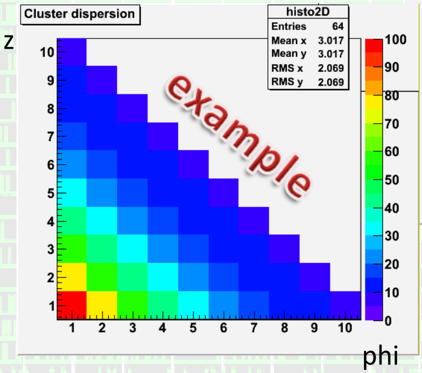


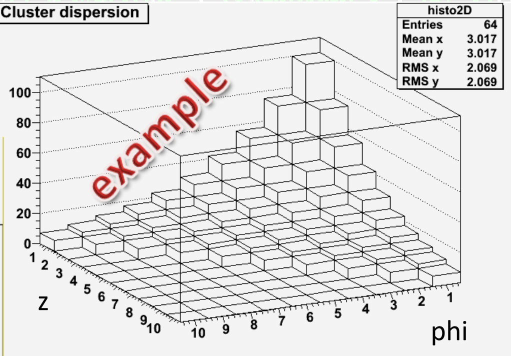
Cluster spread extraction
Es. (5,5)



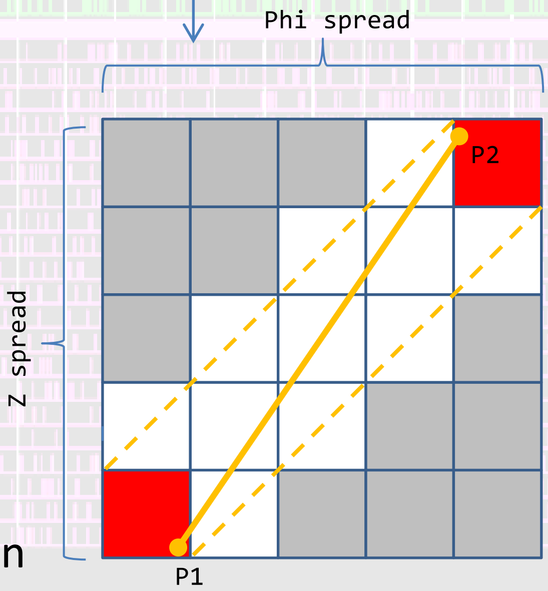
What’s new

- Matrix dimensions update:
  - 200x256 pixels (50x256 sub-matrices)
  - 50 um pitch
- Code optimization
  - Substantial: more robust concentrators
  - Formal: code maintenance
- Monte Carlo generator
  - Rewritten from scratch
  - Now generation of clustered events
  - Knobs:
    - Cluster dispersion distribution in (z,phi)
    - Physical time resolution (test_clock), hit/miss thresholds =Global hit rate
  - Arbitrary pattern extraction by geometrical rules





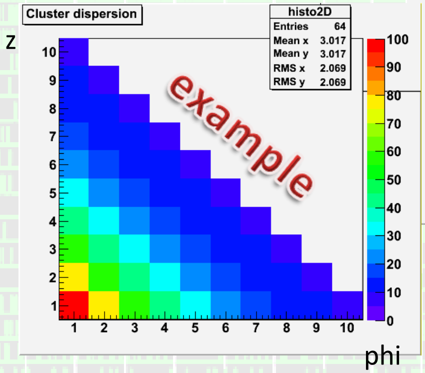
Cluster spread extraction
Es. (5,5)

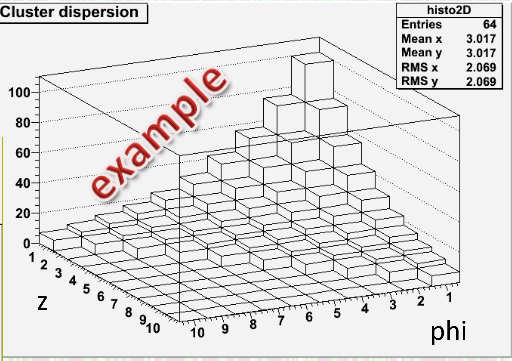


P1- P2 points extraction

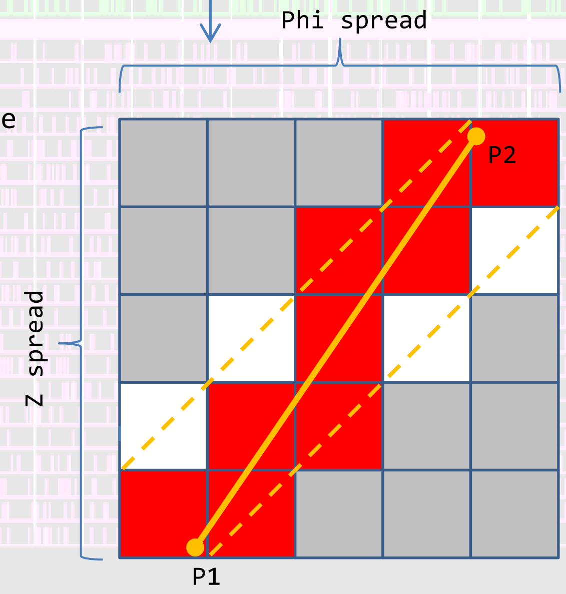
What's new

- Matrix dimensions update:
  - 200x256 pixels (50x256 sub-matrices)
  - 50 um pitch
- Code optimization
  - Substantial: more robust concentrators
  - Formal: code maintenance
- Monte Carlo generator
  - Rewritten from scratch
  - Now generation of clustered events
  - Knobs:
    - Cluster dispersion distribution in (z,phi)
    - Physical time resolution (test_clock), hit/miss thresholds =Global hit rate
  - Arbitrary pattern extraction by geometrical rules





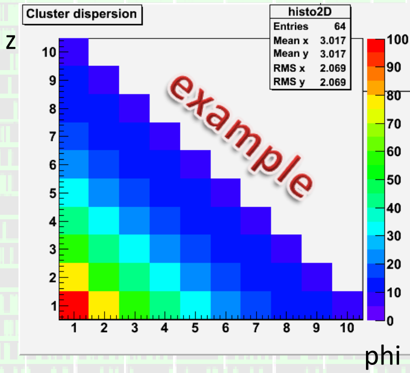
Cluster spread extraction
Es. (5,5)

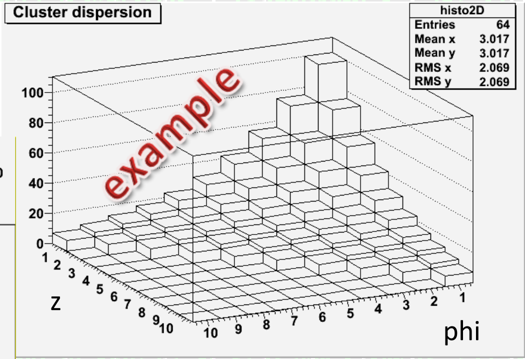


Pattern evaluation

What’s new

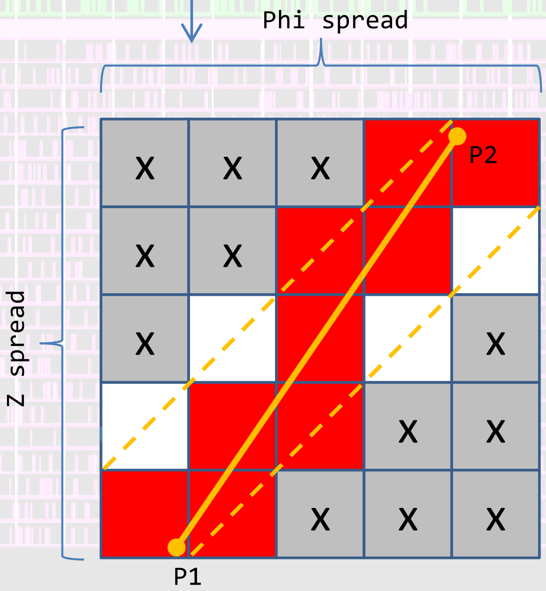
- Matrix dimensions update:
  - 200x256 pixels (50x256 sub-matrices)
  - 50 um pitch
- Code optimization
  - Substantial: more robust concentrators
  - Formal: code maintenance
- Monte Carlo generator
  - Rewritten from scratch
  - Now generation of clustered events
  - Knobs:
    - Cluster dispersion distribution in (z,phi)
    - Physical time resolution (test_clock), hit/miss thresholds =Global hit rate
  - Arbitrary pattern extraction by geometrical rules
  - Pattern check (grey pixels are forbidden)





Cluster spread extraction

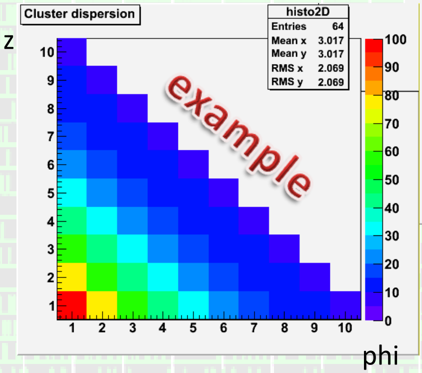
Es. (5,5)

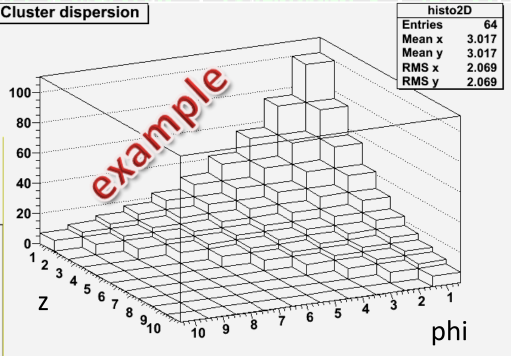


Pattern check

What’s new

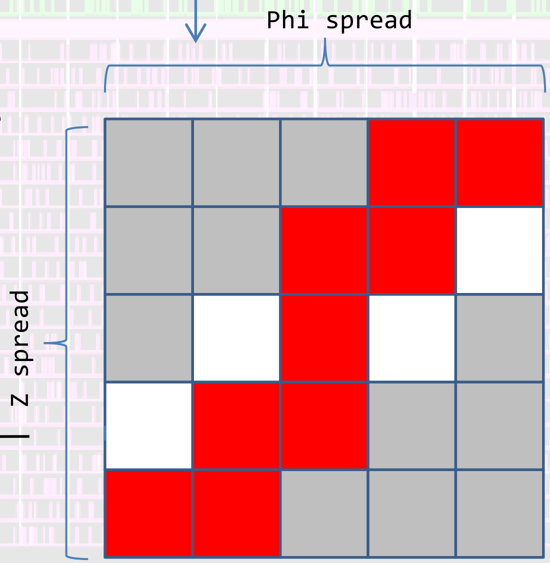
- Matrix dimensions update:
  - 200x256 pixels (50x256 sub-matrices)
  - 50 um pitch
- Code optimization
  - Substantial: more robust concentrators
  - Formal: code maintenance
- Monte Carlo generator
  - Rewritten from scratch
  - Now generation of clustered events
  - Knobs:
    - Cluster dispersion distribution in (z,phi)
    - Physical time resolution (test_clock), hit/miss thresholds =Global hit rate
  - Arbitrary pattern extraction by geometrical rules
  - Pattern check (grey pixels are forbidden)
  - Pattern application to a random pixel of the matrix

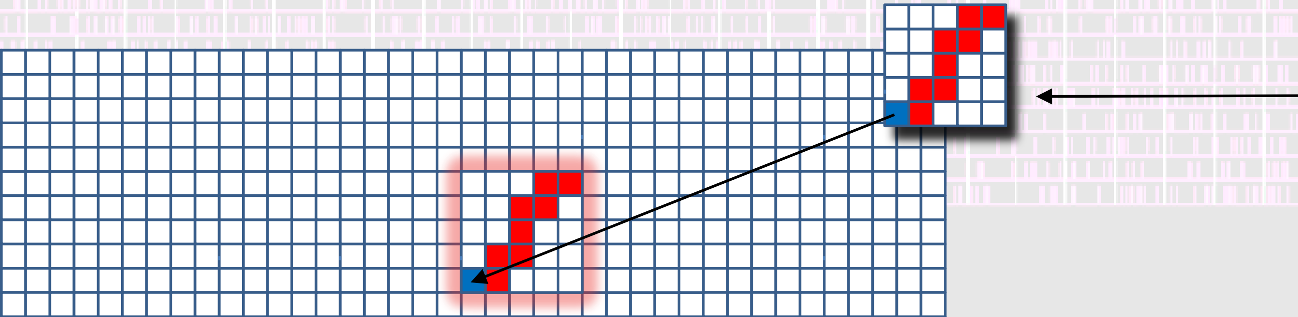




Cluster spread extraction

Es. (5,5)





Matrix interface

- Converging with Fabio and Giulia on a viable matrix interconnection solution
  - TSREQ bus x4 sub-matrices
  - MASK_WRITEb for general pixel reset
  - MaskColSel_b for TSREQ dependent pixel reset

Simulation Diagram

Organization of the VHDL test bench architecture

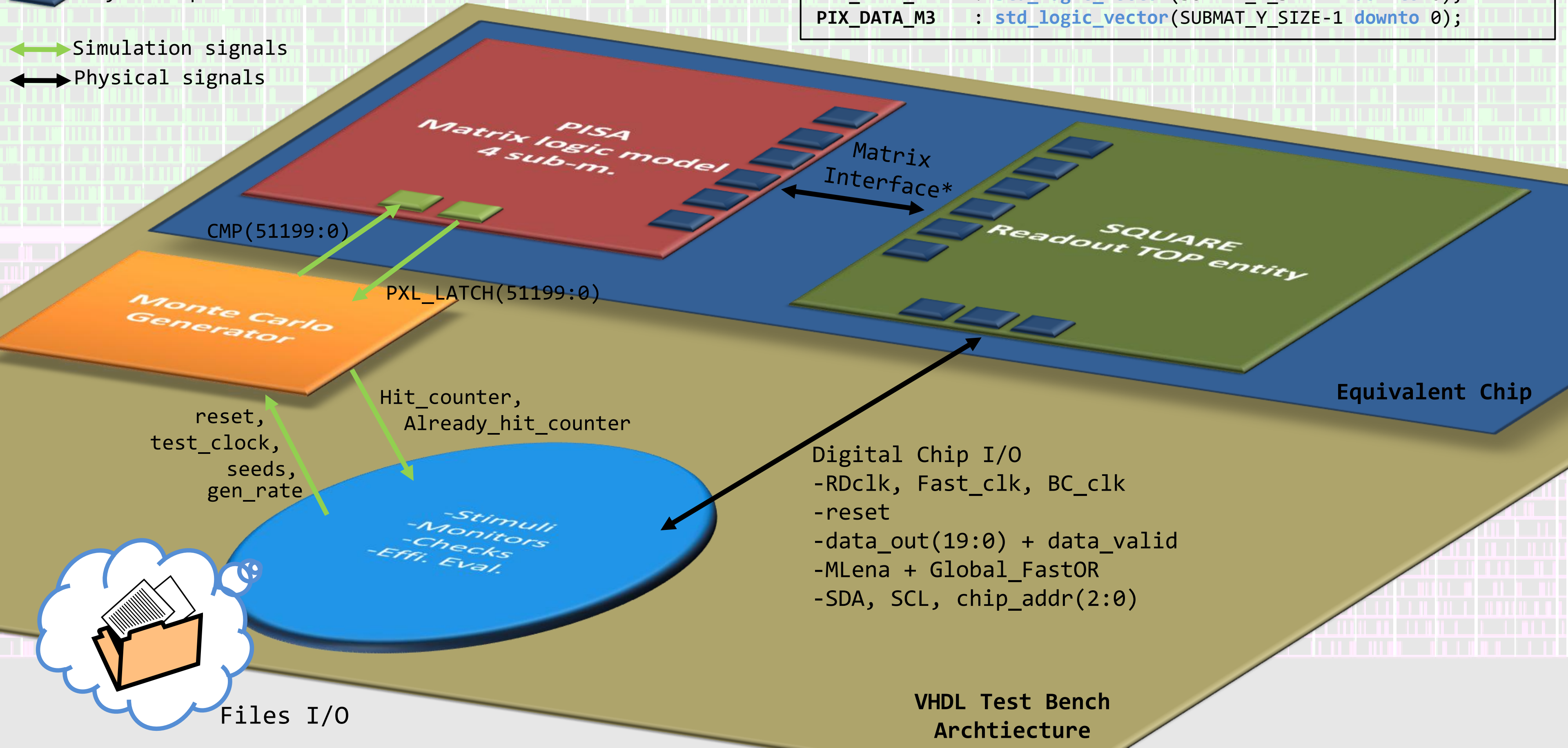
```
--Matrix Interface (*)
ColReadEna_b   : std_logic_vector(MAT_X_SIZE-1 downto 0);
LatchEna_b     : std_logic_vector(MAT_X_SIZE-1 downto 0);
Mask_Write_b   : std_logic_vector(MAT_Y_SIZE-1 downto 0);
MaskColSel_b   : std_logic_vector(MAT_X_SIZE-1 downto 0);
TSCNT          : std_logic_vector(TS_WIDTH-1 downto 0);
TSREQ          : std_logic_vector(N_XSUBMAT*TS_WIDTH-1 downto 0);
FastOr         : std_logic_vector(MAT_X_SIZE-1 downto 0);
PIX_DATA_M0    : std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);
PIX_DATA_M1    : std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);
PIX_DATA_M2    : std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);
PIX_DATA_M3    : std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);
```

🟩 Simulation pads

🟦 Physical pads

↔ Simulation signals

↔ Physical signals



Digital Chip I/O
-RDclk, Fast_clk, BC_clk
-reset
-data_out(19:0) + data_valid
-MLena + Global_FastOR
-SDA, SCL, chip_addr(2:0)

Now SQUARE architecture “ON AIR”:

Preliminary simulations with a matrix model made in Bo

Extracted from the one used for efficiency evaluations presented at Annecy and Biodola

- for test bench structure trial.
- ~100MHz/cm^2

Try-outs (3000 us, 350k/400k hits):

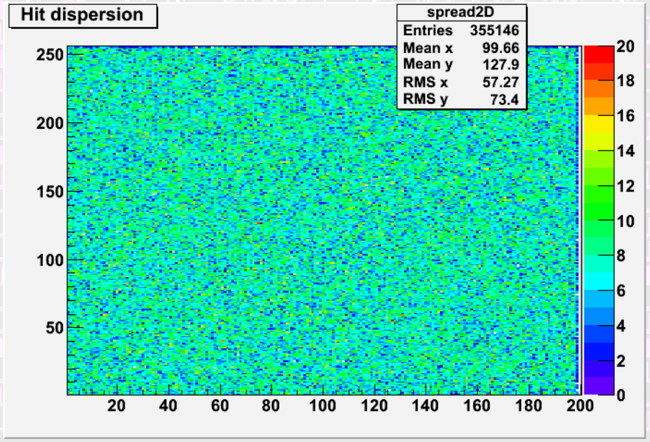
Cluster spread in zeta/phi

	1	2	3	4
1	100%	0%	0%	0%
2	0%	0%	0%	0%
3	0%	0%	0%	0%
4	0%	0%	0%	0%

classic

CF=1

Generated hit distribution



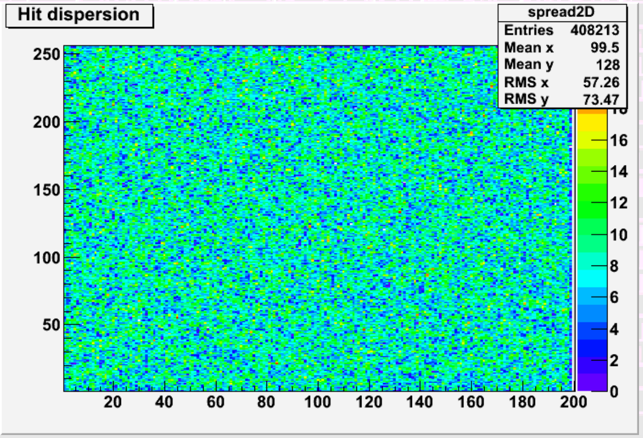
About optimization: 350k hits → ~350k words

Cluster spread in zeta/phi

	1	2	3	4
1	50%	12.5%	4%	1%
2	12.5%	4%	1%	0%
3	4%	1%	0%	0%
4	1%	0%	0%	0%

CF~1.4

Generated hit distribution



400k hits → ~300k words

Rule of thumb area estimations for the final front-end chip

Synthesized a SQUARE readout architecture fitted for a 200 x 256 matrix (50x256 sub-matrices)

Synthesis :

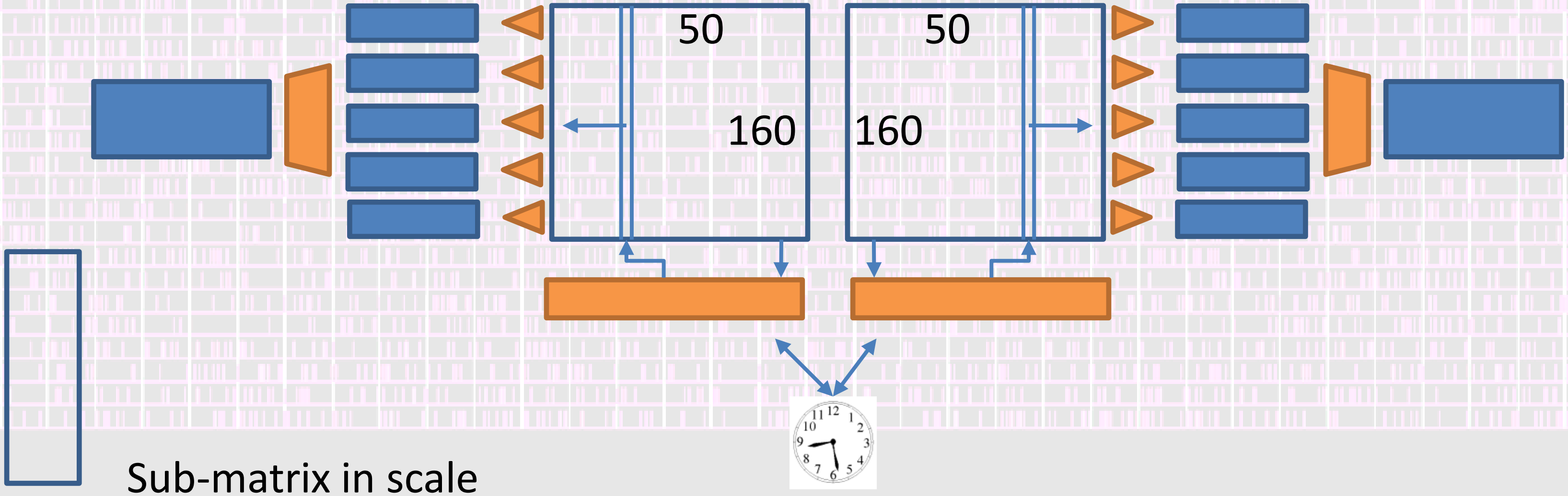
HCMOS9GP library (ST 130 nm like APSEL4D, 4D_1, FE32x128)
240k logic cells
3.5 mm^2 **only** of std-cells area.
60 hours of 100% processor time.

	Cells	Readout Area	density
APSEL4D	100k	6 mm^2	17k cell/mm^2
FE4D32x128	60k	2.5 mm^2	20k cell/mm^2
APSEL3D_TC	12k	1.3 mm^2	9.2k cell/mm^2
FINAL (ST130)	**240k**	**(est) ~ 14 mm^2** ←	**(lowest ST) 17k cell/mm^2**
TC subm.(100x160)	**(est. 31%FINAL)~ 75k**	**(est) 8.2 mm^2** ←	**(TC) 9.2k cell/mm^2**

A layout without matrix interconnections geometry can be misleading.
The estimations above represent the most probable BUT NOT SURE values (especially for TC process that is also changing design kit).

Readout for ApselVI_1D

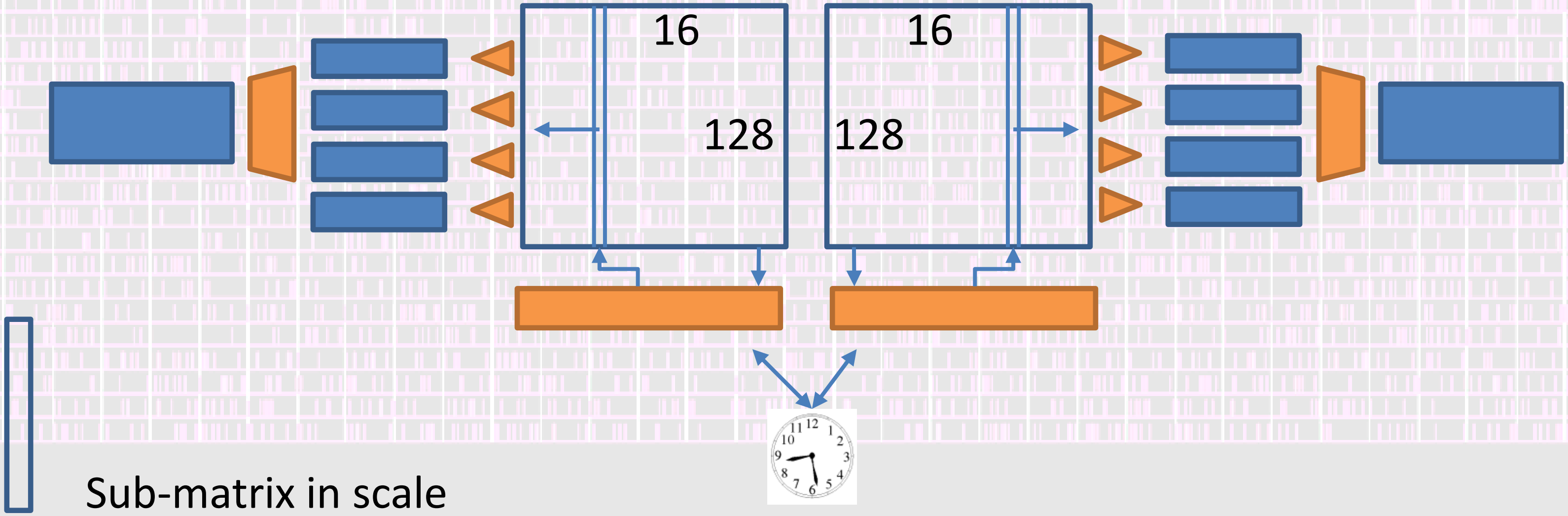
- MATRIX 100x160 (2 sub-m. 50 x160)
- Column divided in:
  - 5 sparsifiers
  - 32 rows for each sparsifier
  - 8 zones for each sparsifier (W_{zone}=4 pixels)



Sub-matrix in scale

Readout for Superpix1

- MATRIX 32x128 (2 sub-m. 16x128)
- Column divided in:
  - 4 sparsifiers
  - 32rows for each sparsifier
  - 8 zones for each sparsifier (W_{zone}= 4 pixels)


16
128
16
128
Sub-matrix in scale