TIIMM0/1 prototype: Cadence mixed simulation/verification

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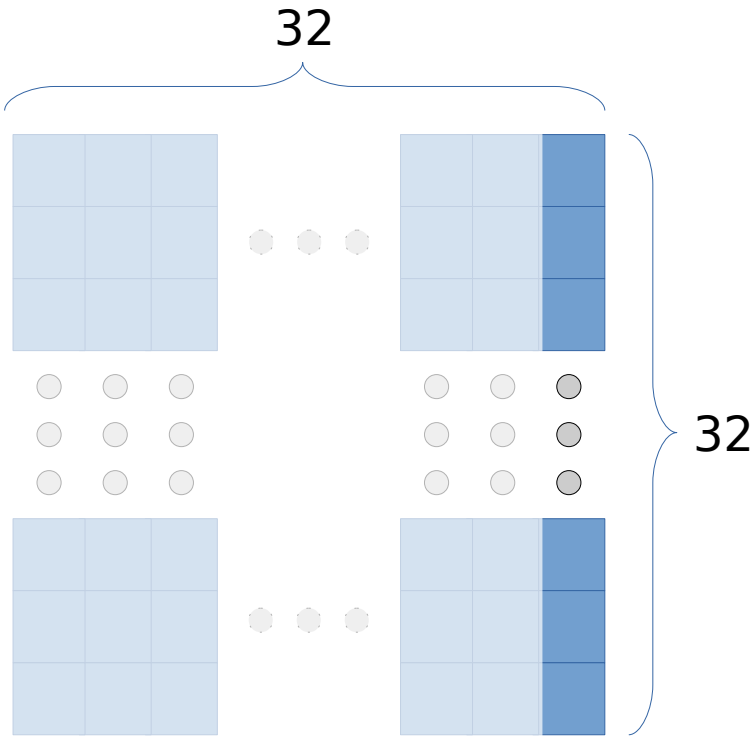
Outline

TIIMM0 Architecture setup

TowerJazz Technology access

SystemVerilog testbench top

xrun AMS flow completed



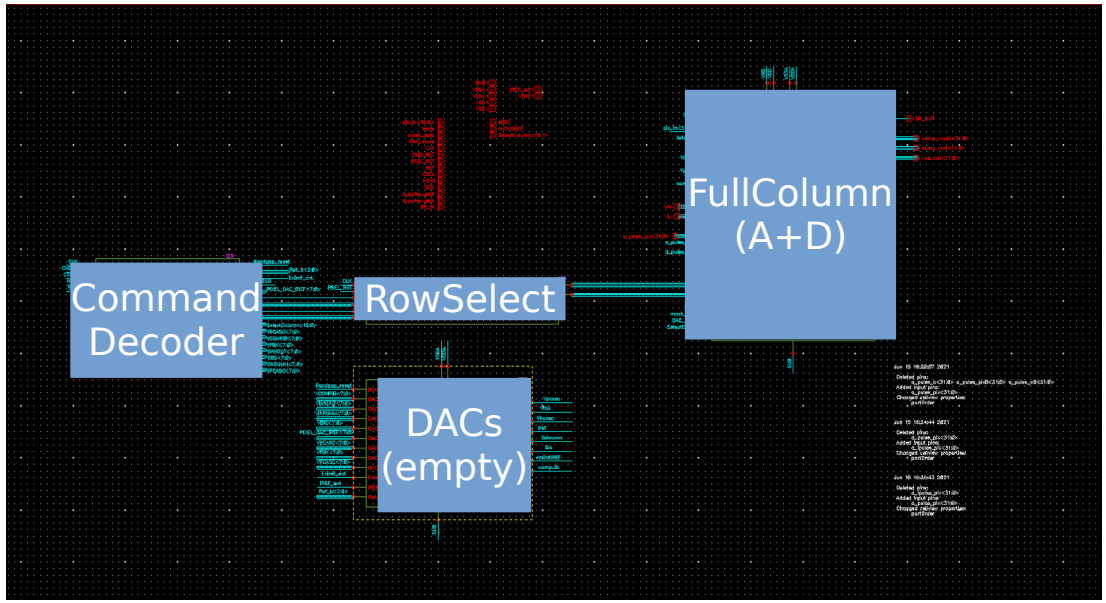
TIIMM0 architecture on INFN PC (!TJ technology)

TIIMM0 analog:

+ pixel architecture replicated from Weiping project pdf (schematic)
  (with locally accessible technology, other than TowerJazz)
- missing (column) DACs architecture, but TrimmDAC (pixel)

TIIMM0 digital:

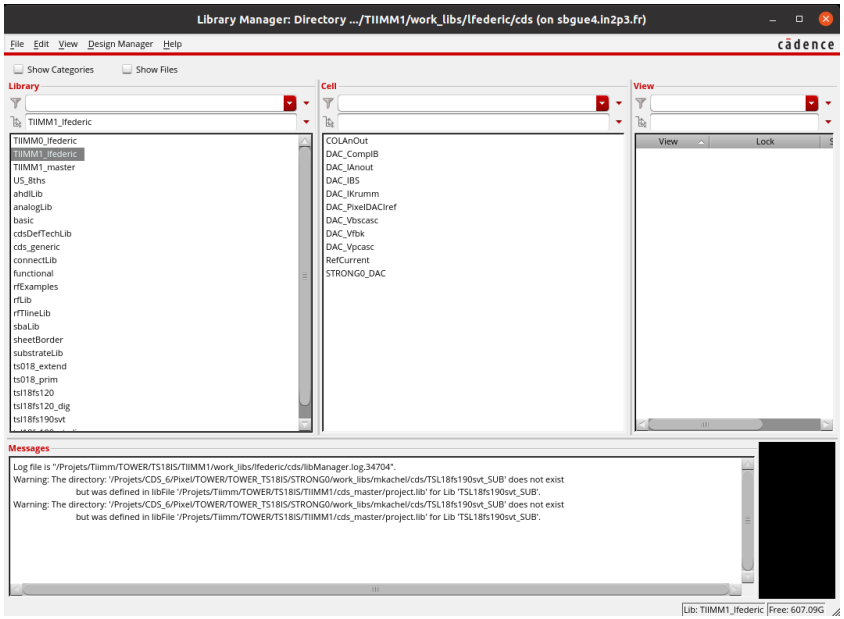
+ pixel digital part (column, “Strong0PixelReader”)(SystemVerilog);
+ row select logic (matrix, “RowSelect”)(Verilog);
+ command decoder (matrix, “CommandDecoder”)(Verilog);



TIIMM0 architecture on IN2P3 PC (TJ technology)

TIIMM0 analog:

+ copied my project on INFN PC to the IN2P3 PC and added to the cds.lib file (TIIMM0_lfederic);
+ components migrated to TowerJazz library (ts018_prim) and parameter from Weiping schematics (schematic);
+ access only to TIIMM1 library (TIIMM1_master, but TIIMM1 = TIIMM0 – TrimmDAC);
+ missing some cells link → in my own library (TIIMM1_lfederic) I created the missing cell using TIIMM1_master available cells (schematic).



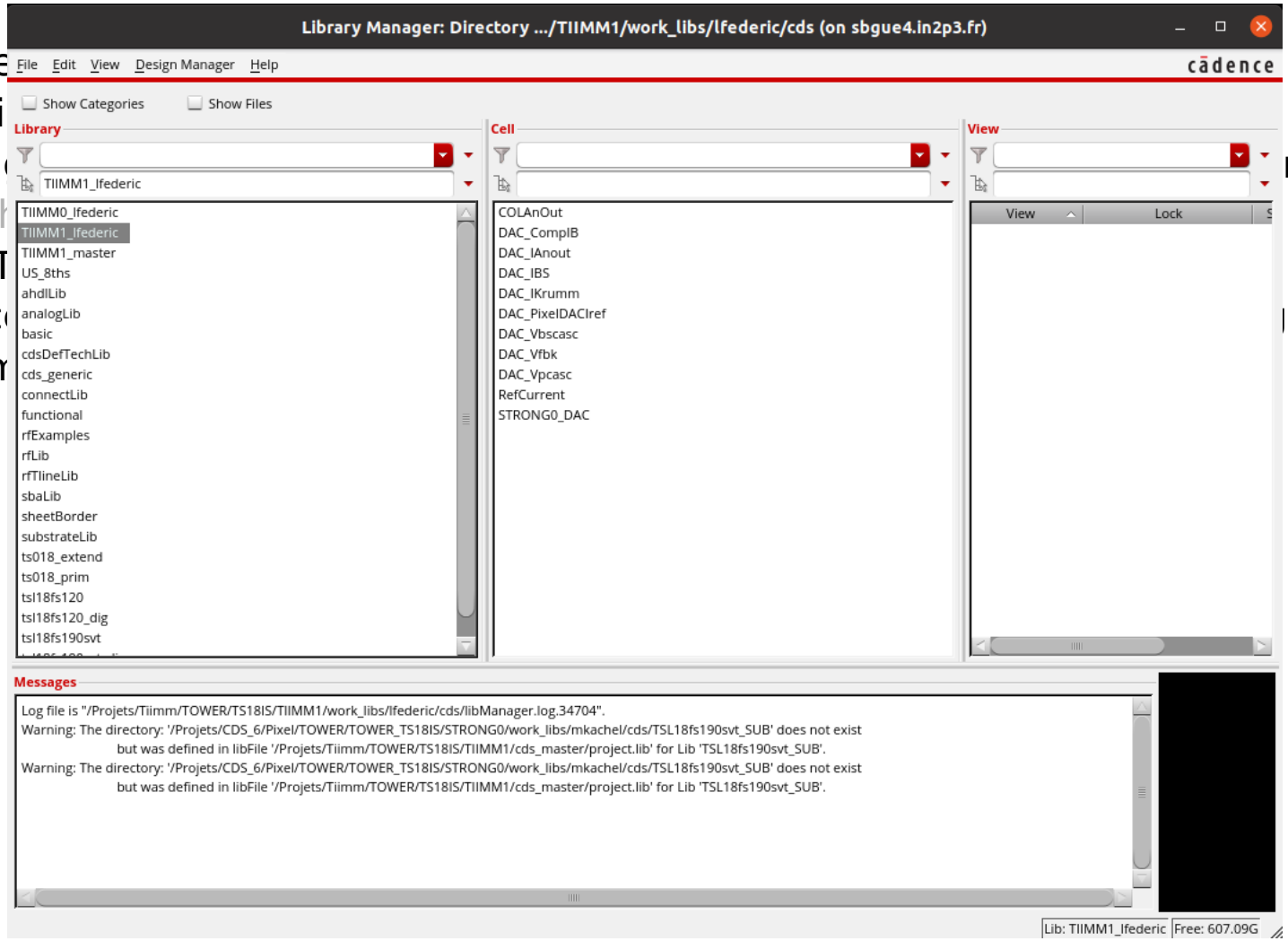
TIIMM0 digital:

* no changes

TIIMM0 architecture on IN2P3 PC (TJ technology)

TIIMM0 analog:

+ copied my proje
  (TIIMM0_lfederi
+ components mi ng
  schematics (sch
+ access only to T
+ missing some c cell
  using TIIMM1_m



TIIMM0 digital:

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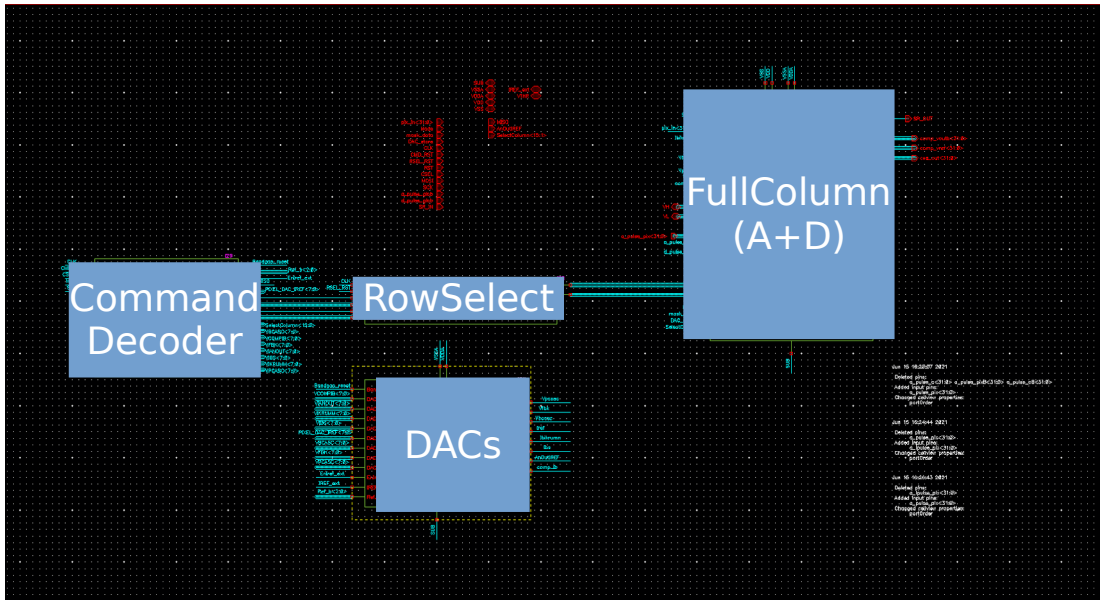

TIIMM0 digital:

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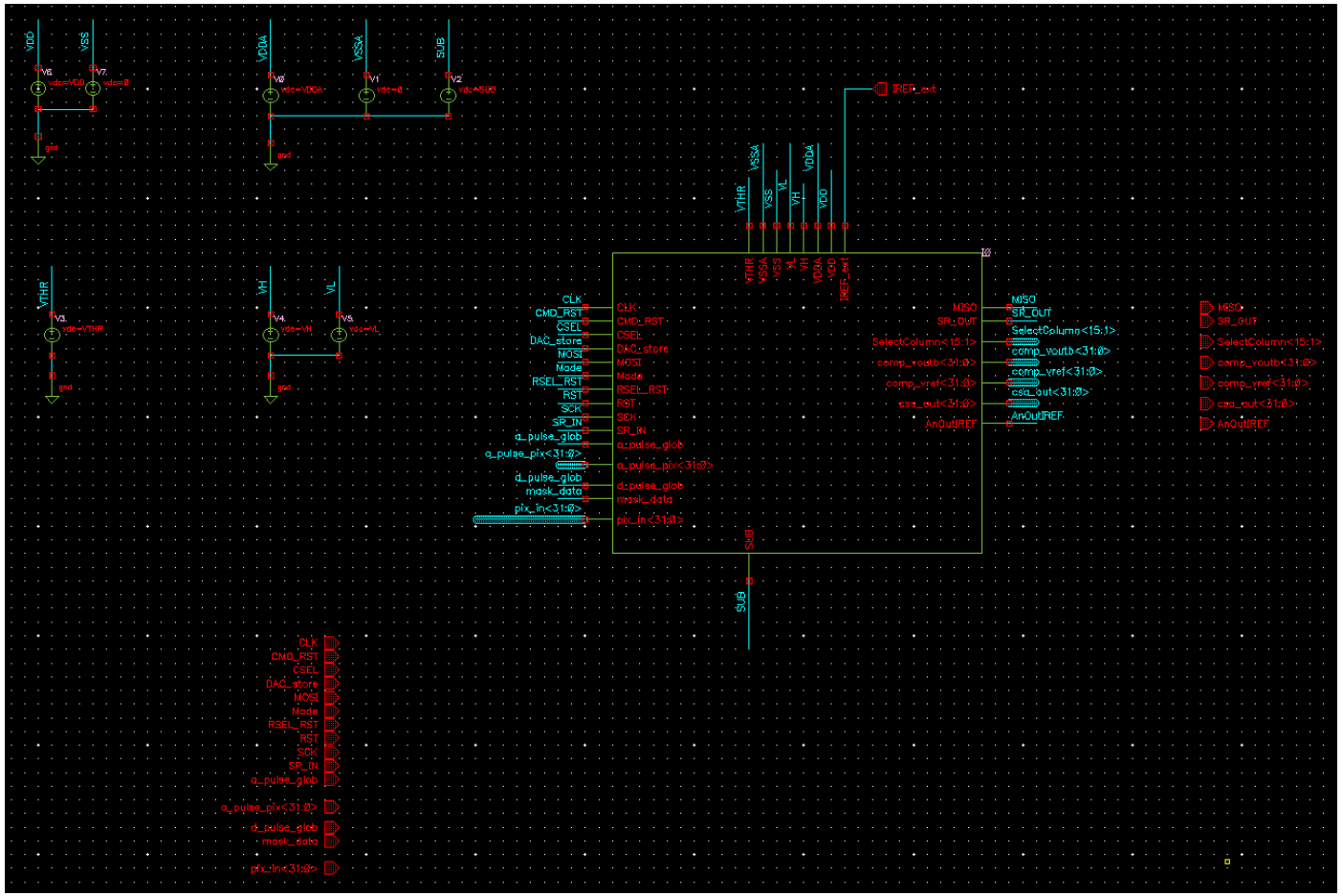
TIIMM0 architecture on IN2P3 PC (TJ technology)

TIIMM0:
+ Digital and Analog Column top



TIIMM0 architecture AMS

TIIMM0:
+ SystemVerilog testbench (trivial) to test the AMS simulation flow with A+D column
(SV testbench instantiating the FullColumn top (seen in previous slide)

Next steps

+ Complete the testbench for the full column mixed signals simulation/verification;
+ extend it to full matrix (?);