HiDRA2: High Dynamic Range Amplifier frontend ASIC

Specifications

Number of channels: 16

Supply voltage: 3.3 V

Analog functions: automatic double-gain pulse reset Charge Sensitive Amplifier (CSA), calibration circuitry (registers and capacitors), Correlated double sampling, Self-triggering circuitry, and output multiplexer

Power consumption: 3.75 mW/ch (common circuitry included), typical corner

Dynamin range:
- High gain: $\approx$ 2.7 pC (560 MIP on 380 μm Si sensors)
- Low gain: $\approx$ 52.6 pC (11000 MIP on 380 μm Si sensors)

Linearity
- High gain: $\pm$ 0.3 %
- Low gain: $\pm$ 0.6 %

Calibration capacitance: 1.6 pF

Equivalent noise charge: 2280 e^- + 7.5 e^-/pF RMS (CDS time constant of 10 us)

CSA minimum reset pulse duration: t_{CSA_reset} = 150 ns

CSA settling time (1 %): $t_{S\_CSA,1\%}$ = 400 ns @ C_D = 300 pF

CDS external pedestal reference: 900 mV

CDS reset duration: t_{CDS_reset} = t_{CSA_reset} + 400 ns @ C_D = 300 pF

Self-trigger gain: ×10

Self-trigger threshold: set by an external resistor, 2 adjustment bits ($\approx$ ×1, ×1.5, ×2, and ×2.5)

Self-trigger comparator hysteresis: 16 mV $\pm$ 2.3 mV r.m.s.

Self-trigger response time: $\leq$ 500 ns for signals 10 mV larger than the effective threshold (equal to the threshold voltage plus the comparator hysteresis)

Output buffer driving capability: 20 kΩ // 100 pF

Output settling time (1 %): $t_{S\_OUT,1\%}$ = 80 ns @ C_L = 100 pF

Package: CQFP100 (CQZ10001)

Pin function and description

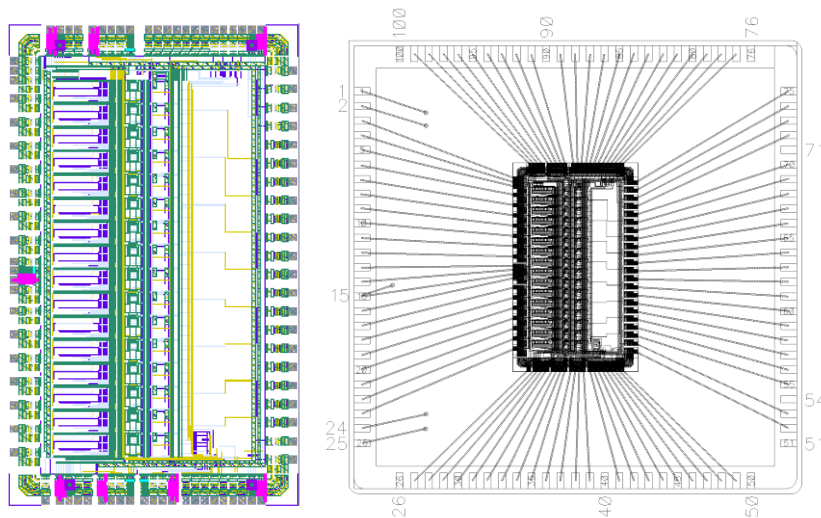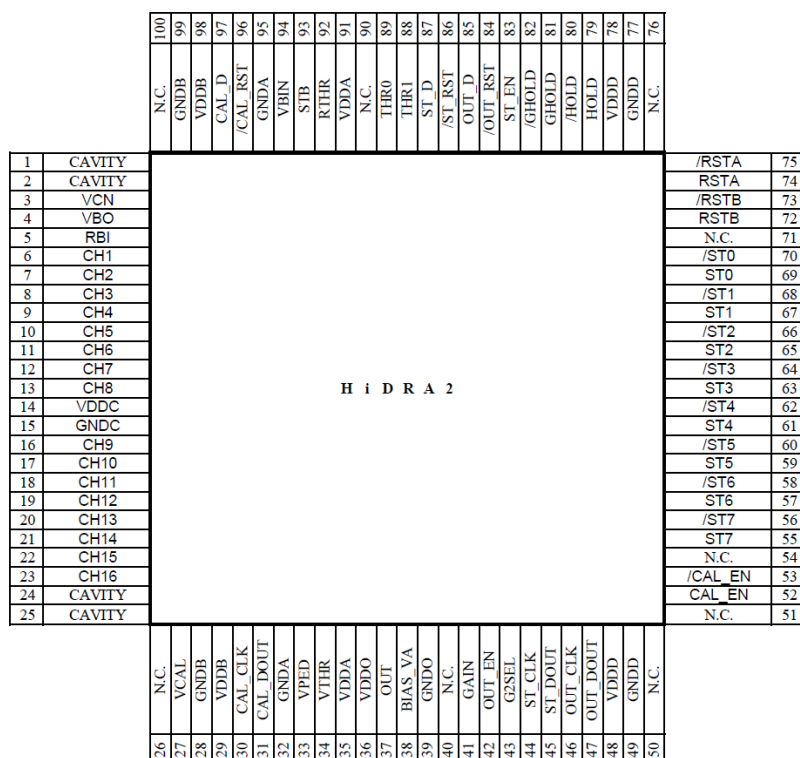**Figure 1**: HiDRA2 die and bonding diagram.

Figure 2: pin function diagram.

Table 1: pin function list.

Pin nr.	Name	Description	Notes
1	CAVITY	Connection to the package cavity	Connect to ground
2	CAVITY	Connection to the package cavity	Connect to ground
3	VCN	Bias of the CSA common gate	1.5 V, bypass capacitor to ground (pin 15)
4	VBO	Bias of the CSA output branch	150 kΩ connected between this pin and ground (pin 15), bypass capacitor to the power supply VDDC
5	RBI	Bias of the CSA input branch	2.2 kΩ connected between this pin and VDDC without bypass capacitor. To provide some filtering the resistor can be replaced by the series of two resistors with a grounded (pin 15) bypass capacitor connected to the common point of the series
6	CH1	Input channel 1	AC coupling mandatory
7	CH2	Input channel 2	AC coupling mandatory
8	CH3	Input channel 3	AC coupling mandatory
9	CH4	Input channel 4	AC coupling mandatory
10	CH5	Input channel 5	AC coupling mandatory
11	CH6	Input channel 6	AC coupling mandatory
12	CH7	Input channel 7	AC coupling mandatory
13	CH8	Input channel 8	AC coupling mandatory
14	VDDC	CSA power supply	3.3 V, bypass capacitor to ground (pin 15)
15	GNDC	CSA ground, connected to cavity	
16	CH9	Input channel 9	AC coupling mandatory
17	CH10	Input channel 10	AC coupling mandatory

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18	CH11	Input channel 11	AC coupling mandatory
19	CH12	Input channel 12	AC coupling mandatory
20	CH13	Input channel 13	AC coupling mandatory
21	CH14	Input channel 14	AC coupling mandatory
22	CH15	Input channel 15	AC coupling mandatory
23	CH16	Input channel 16	AC coupling mandatory
24	CAVITY	Connection to the package cavity	Connect to ground
25	CAVITY	Connection to the package cavity	Connect to ground
26	N.C.	Not connected	Connect to ground
27	VCAL	Calibration voltage input	0 – 3.3 V
28	GNDB	Digital circuitry ground	Connected to pin 99
29	VDDB	Digital circuitry power supply	3.3 V, connected to pin 98, bypass capacitor to ground (pin 28)
30	CAL_CLK	Calibration shift register clock	CMOS input (Schmitt trigger)
31	CAL_DOUT	Calibration shift register last channel output	CMOS output (I_{DRIVE} = 4 mA), can be used to daisy-chain several chips
32	GNDA	CDS and Self-trigger (ST) ground	Connected to pin 95
33	VPED	CDS (and output) pedestal voltage reference	0.9 V, bypass capacitor to ground (pin 32)
34	VTHR	ST threshold	10 nF bypass capacitor to VPED (pin 33)
35	VDDA	CDS and ST power supply	3.3 V, connected to pin 91, bypass capacitor to ground (pin 32)
36	VDDO	Output buffer power supply	3.3 V, bypass capacitor to ground (pin 39)
37	BIAS_VA	Output buffer bias	25 kΩ connected between this pin and VDDO, bypass capacitor to ground (pin 39)
38	OUT	Analog output	High impedance when OUT_EN is low
39	GNDO	Output buffer ground	
40	N.C.	Not connected	Connect to ground
41	GAIN	GAIN muxed output	CMOS output (I_{DRIVE} = 4 mA), high impedance when OUT_EN is low
42	OUT_EN	Analog output and GAIN enable signal	CMOS input (Schmitt trigger), active high. When low the outputs are in a high impedance state
43	G2SEL	Low gain selection	CMOS input (Schmitt trigger)
44	ST_CLK	Self-trigger shift register clock	CMOS input (Schmitt trigger)
45	ST_DOUT	Self-trigger shift register last channel output	CMOS output (I_{DRIVE} = 4 mA), can be used to daisy-chain several chips
46	OUT_CLK	Output shift register clock	CMOS input (Schmitt trigger)
47	OUT_DOUT	Output shift register last channel output	CMOS output (I_{DRIVE} = 4 mA), can be used to daisy-chain several chips
48	VDDD	Digital circuitry power supply	3.3 V, connected to pin 78, bypass capacitor to ground (pin 49)
49	GNDD	Digital circuitry ground	Connected to pin 77
50	N.C.	Not connected	Connect to ground
51	N.C.	Not connected	Connect to ground
52	CAL_EN	Calibration switches enable	LVDS input (pair with pin 53)
53	/CAL_EN	Calibration switches enable	LVDS input (pair with pin 52), with a fixed calibration voltage can be used to inject the charge at the CSA inputs
54	N.C.	Not connected	Connect to GND
55	ST7	Self-trigger output of CH15/CH16	CMOS output (I_{DRIVE} = 4 mA)
56	/ST7	Self-trigger complementary output	CMOS output (I_{DRIVE} = 4 mA)

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		of CH15/CH16	
57	ST6	Self-trigger output of CH13/CH14	CMOS output (I_{DRIVE} = 4 mA)
58	/ST6	Self-trigger complementary output of CH13/CH14	CMOS output (I_{DRIVE} = 4 mA)
59	ST5	Self-trigger output of CH11/CH12	CMOS output (I_{DRIVE} = 4 mA)
60	/ST5	Self-trigger complementary output of CH11/CH12	CMOS output (I_{DRIVE} = 4 mA)
61	ST4	Self-trigger output of CH9/CH10	CMOS output (I_{DRIVE} = 4 mA)
62	/ST4	Self-trigger complementary output of CH9/CH10	CMOS output (I_{DRIVE} = 4 mA)
63	ST3	Self-trigger output of CH7/CH8	CMOS output (I_{DRIVE} = 4 mA)
64	/ST3	Self-trigger complementary output of CH7/CH8	CMOS output (I_{DRIVE} = 4 mA)
65	ST2	Self-trigger output of CH5/CH6	CMOS output (I_{DRIVE} = 4 mA)
66	/ST2	Self-trigger complementary output of CH5/CH6	CMOS output (I_{DRIVE} = 4 mA)
67	ST1	Self-trigger output of CH3/CH4	CMOS output (I_{DRIVE} = 4 mA)
68	/ST1	Self-trigger complementary output of CH3/CH4	CMOS output (I_{DRIVE} = 4 mA)
69	ST0	Self-trigger output of CH1/CH2	CMOS output (I_{DRIVE} = 4 mA)
70	/ST0	Self-trigger complementary output of CH1/CH2	CMOS output (I_{DRIVE} = 4 mA)
71	N.C.	Not connected	Connect to ground
72	RSTB	Reset sequencing signal B	LVDS input (pair with pin 73)
73	/RSTB	Reset sequencing signal B	LVDS input (pair with pin 72)
74	RSTA	CSA "soft" reset	LVDS input (pair with pin 75)
75	/RSTA	Reset sequencing signal B	LVDS input (pair with pin 74)
76	N.C.	Not connected	Connect to ground
77	GNDD	Digital circuitry ground	Connected to pin 49
78	VDDD	Digital circuitry power supply	3.3 V, connected to pin 48, bypass capacitor to ground (pin 77)
79	HOLD	Hold signal	LVDS input (pair with pin 80)
80	/HOLD	Hold signal	LVDS input (pair with pin 79)
81	GHOLD	Gain hold signal	LVDS input (pair with pin 82)
82	/GHOLD	Gain hold signal	LVDS input (pair with pin 81)
83	ST_EN	Self-trigger enable	CMOS input (Schmitt trigger), active high. When low STx = 0 V and /STx = 3.3 V
84	/OUT_RST	Output shift register reset	CMOS input (Schmitt trigger), active low
85	OUT_D	Output shift register data in	CMOS input (Schmitt trigger)
86	/ST_RST	Self-trigger shift register reset	CMOS input (Schmitt trigger), active low
87	ST_D	Self-trigger shift register data in	CMOS input (Schmitt trigger)
88	THR1	Self-trigger threshold adjustment	CMOS input (Schmitt trigger)
89	THR0	Self-trigger threshold adjustment	CMOS input (Schmitt trigger)
90	N.C.	Not connected	Connect to ground
91	VDDA	Left bank CDS power supply	3.3 V, connected to pin 35, bypass capacitor to ground (pin 95)
92	RTHR	Bias for the generation of the self-trigger threshold	Resistor R_{THR} connected between this pin and VDDA, bypass capacitor to ground (pin 95)
93	STB	Bias for the self-trigger circuit	56 kΩ connected between this pin and VDDA, bypass capacitor to ground (pin 95)
94	VBIN	Bias of the CDS stage	100 kΩ connected between this pin and VDDA, bypass capacitor to ground (pin 95)

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95	GNDA	CDS ground	Connected to pin 32
96	/CAL_RST	Calibration shift register reset	CMOS input (Schmitt trigger), active low
97	CAL_D	Calibration shift register data in	CMOS input (Schmitt trigger)
98	VDDB	Digital circuitry power supply	3.3 V, connected to pin 29, bypass capacitor to ground (pin 99)
99	GNDB	Digital circuitry ground	Connected to pin 28
100	N.C.	Not connected	Connect to ground

NOTE 1: all numbers are for the typical corner with V_{DD} = 3.3 V and T = 27 °C.

NOTE 2: despite their different names, all GND pins must be connected to the same ground plane. VDD pins with the same name are internally connected together, hence they must be connected together externally minimizing the series resistance of the connection: power planes should be used.

NOTE 3: low voltage differential input signals can also be driven by differential CMOS signals. It is also possible to use single-ended signals connected to the positive polarity input provided that the negative polarity inputs are biased at VDD/2, but in this case charge will be injected at the CSA inputs by means of stray capacitive couplings between bonding wires. No termination resistor is integrated so that it is possible to control several devices with the same signal. External termination resistors are required to provide the differential voltage levels to the device.

NOTE 4: Five pins are connected to the metalized cavity of the ceramic package, one of which is also the ground pin for the CSAs. To reduce as much as possible digital noise interference with the analog section of the ASIC, it is best to connect all CAVITY pins to the ground plane.

HiDRA2 circuit operation

The ASIC includes 16 frontend channels, based on a pulsed reset Charge Sensitive Amplifier (CSA) with automatic double-gain selection, followed by a Correlated Double Sampling (CDS) filter, and a self-trigger circuitry that provides a differential CMOS output for each pair of channels (see Figure 3).

Frontend section

To correctly operate the frontend, it is necessary to provide to the chip a periodic reset sequence that discharges the CSA and CDS capacitors on a regular basis. The minimum CSA reset duration is 150 ns, while the CDS reset must account for the output settling time of the CSA after the reset (400 ns). The CSA is reset in two phases to reduce charge injection, and the reset sequence is repeated with a period that corresponds to the CDS time constant (interval between the acquisitions of the two samples). To be valid, an event must be triggered at least $t_{S\_CSA,1\%}$ before the second sample is to be acquired, maintaining in this way a fixed CDS time constant. After an event is detected, the read-out electronics controlling the ASIC is required to start the CSA settling time wait, and then to assert the GHOLD signals to avoid gain switching when the signal is very close to the low gain threshold. As soon as the CDS time constant expires the HOLD signal must be asserted, instead of the next reset sequence, to acquire the second sample and disconnect the CSA from the CDS filter. At this time the CDS filter becomes a Hold buffer for the subsequent signal acquisition. Upon completion of the read-out of all channels, the reset sequence must be started again.

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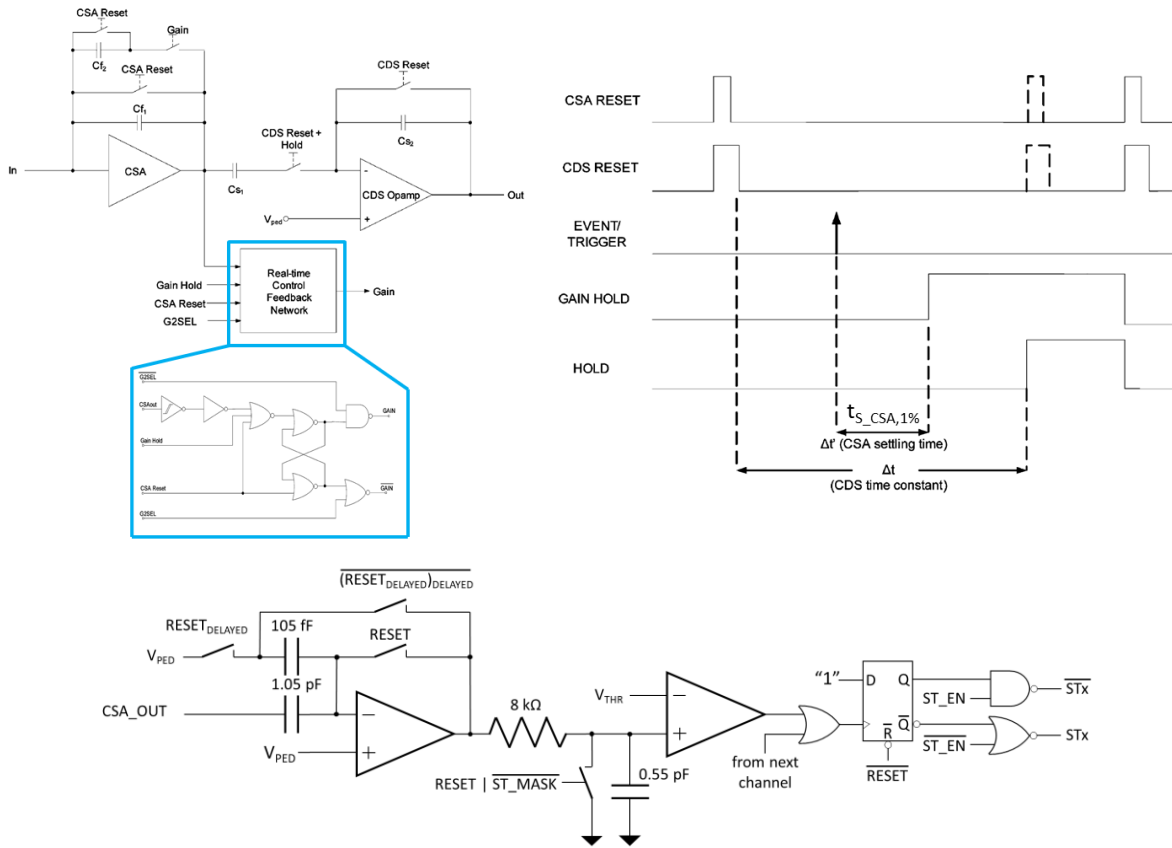
Figure 3: block scheme of a frontend channel and the self-trigger circuitry, and the diagram of the signal acquisition concept.

The signals controlling the reset sequence are RSTA-/RSTA and RSTB-/RSTB (LVDS inputs). They encode the two CSA reset phases, the CDS reset, and the signal acquisition configuration as shown by the following table and timing diagram:

RSTA	RSTB	Function
0	0	Signal acquisition
1	0	CSA reset phase 1 and CDS reset
1	1	CSA reset phase 2 and CDS reset
0	1	CDS reset
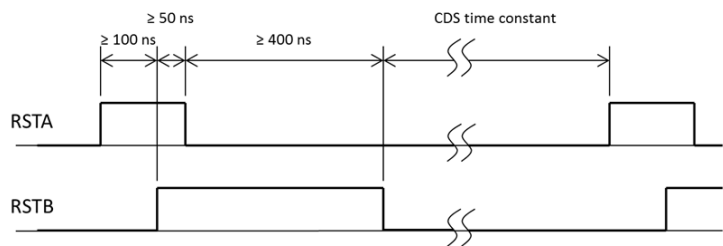
The reset sequence starts with the RSTA-RSTB state "10" that must be asserted for at least 100 ns, then the state is switched to "11" for at least 50 ns, followed by the state "01" for at least 400 ns ($t_{S\_CSA,1\%}$). At this point signal acquisition starts with the RSTA-RSTB state "00" that lasts for a time equal to the CDS time constant.

The signal from all the channels is read out by means of a multiplexer that connects the output of a channel to the OUT pin when the relative bit of a dedicated shift register is active and the OUT_EN signal is asserted. Only one bit of the shift register must be active at any given time, otherwise a short-circuit results between the outputs of the simultaneously active channels. Also the digital GAIN signal of each channel, indicating the CSA gain configuration for the event, is multiplexed to a single output pin, and both outputs are in a high impedance state when OUT_EN is low.

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The frontend comprises a calibration circuitry consisting of a capacitor, a D-type flip-flop, and a two positions switch. In normal operation the switch connects the calibration capacitor to ground in parallel to the detector and stray capacitance. The D-type flip-flop is part of a shift register that can be used to daisy-chain several chips together to set the calibration mask for all the channels. If the flip-flop holds a "1" then the switch can connect the calibration capacitor to the VCAL pin injecting at the CSA input a charge $C_{CAL} \times V_{CAL}$. The actual connection is possible only when the CAL_EN-/CAL_EN LVDS signals are active. Hence, CAL_EN is effectively used to inject the charge, but it is also possible (but not preferred) to keep this signal active and to pulse instead the VCAL pin.

For calibration purposes, the gain of the CSA can be set to its low value by means of the G2SEL signal, which overrides the automatic-gain control circuit.

The data inputs of both calibration and output shift registers are connected to the respective flip-flops of CH1, hence it is possible to perform a sequential calibration of the channels by operating the calibration shift register in the same way as the output register. It is also possible to set up a calibration mask to inject charge in more than one channel at the same time, in this case the mask must be shifted in starting from the bit corresponding to CH16.

Self-trigger section

The self-trigger section comprises the threshold generator circuit (not shown in Figure 3) and, for each channel, an amplification stage and a comparator. The threshold generator is based on three current mirrors, biased by an external resistor connected to +3.3 V, whose output currents are summed together and then redirected to a resistor connected to V_{PED}. Two of the current mirrors can be switched off/on by means of the input signals TH0 and TH1, providing a minimal threshold regulation capability. The base value of the threshold is ≈ 0.7 MIPs for $R_{THR} = 680$ kΩ, and ≈ 1.6 MIPs for $R_{THR} = 330$ kΩ; the TH0-TH1 configuration allows to multiply the base threshold for a coefficient which is approximately ×1.5 (code 01), ×2 (code 10) and ×2.5 (code 11).

The threshold is applied to the negative input of a comparator connected to a ×10 amplification stage. This amplification stage allows to minimize the impact of the comparator offset and to simplify the generation of the threshold. The gain stage also acts as the CDS to filter the output of the CSA, and its circuit configuration allows to cancel the input offset. It is reset by the same signal that resets the CDS. The output of the gain stage is connected to the comparator by means of a low pass RC filter, which is shorted to ground during the reset phase, or if the self-trigger is disabled for the channel. This feature provides the required immunity to the transient occurring when the reset signal is switched off. Since the comparator provides hysteresis to reduce switching due to noise, the actual threshold is the sum of the output of the threshold generator and the hysteresis itself.
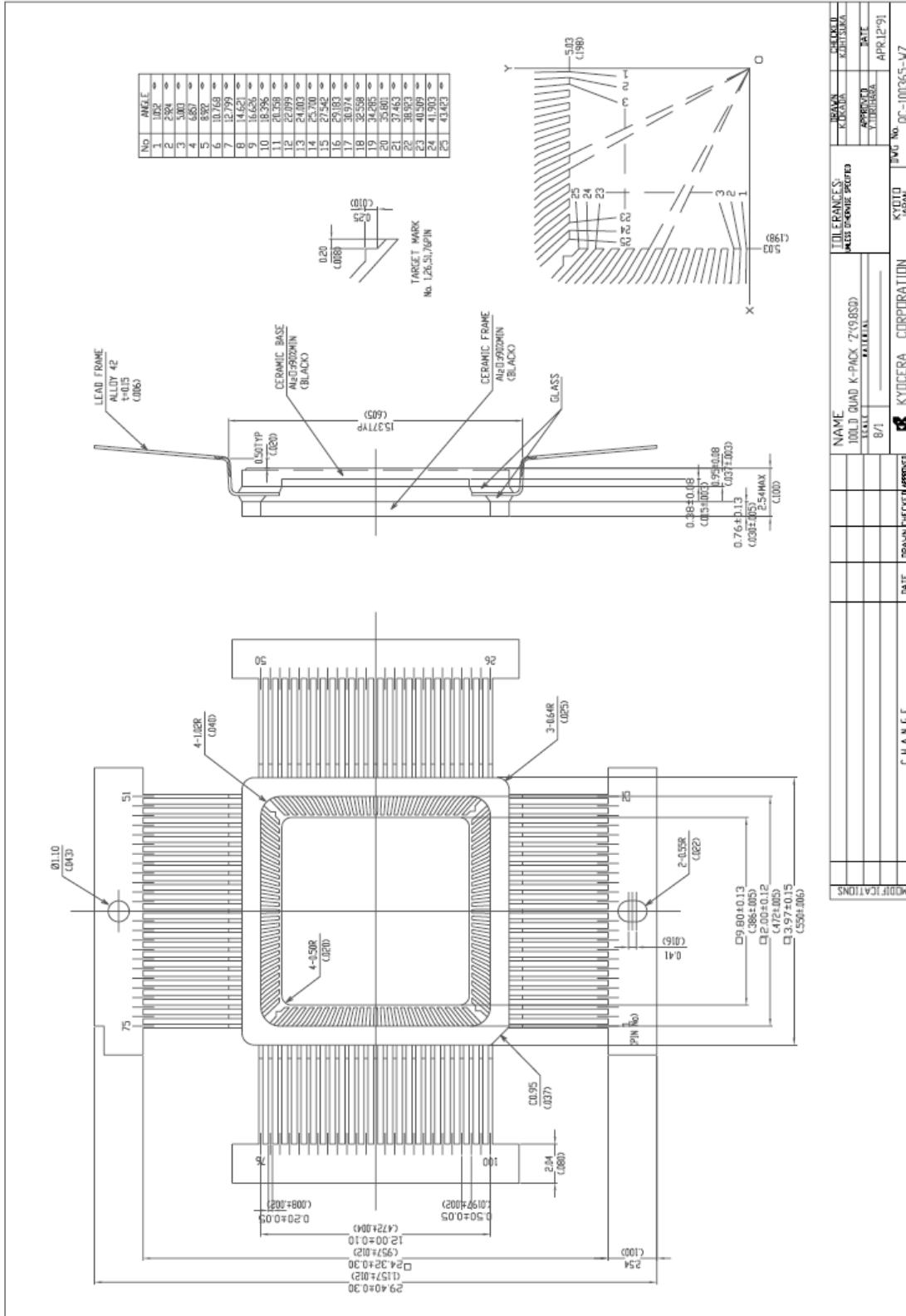
The ORed comparator outputs of two consecutive channels clock a D flip-flop whose outputs, masked by the ST_EN signal, drive the STx and /STx outputs of the chip.

The self-trigger circuit is continuously operating when not in the reset state, hence the self-trigger output must be sampled as soon as a good trigger is detected and the GHOLD signal is sent to the frontend section. The ST_EN signal could be disabled during event acquisition to avoid switching caused by signal injection due to capacitive coupling between the output shift register signals and the ASIC analog inputs.

A shift register is provided to mask the self-trigger on a channel-by-channel basis. The input of the shift register is connected to the flip-flop of CH1, and the output of the last flip-flop is provided to allow for daisy-chain connections. The self-trigger mask must be shifted-in in reverse order, i.e. starting with the value of the mask for CH16.

Package information