PSD Trigger

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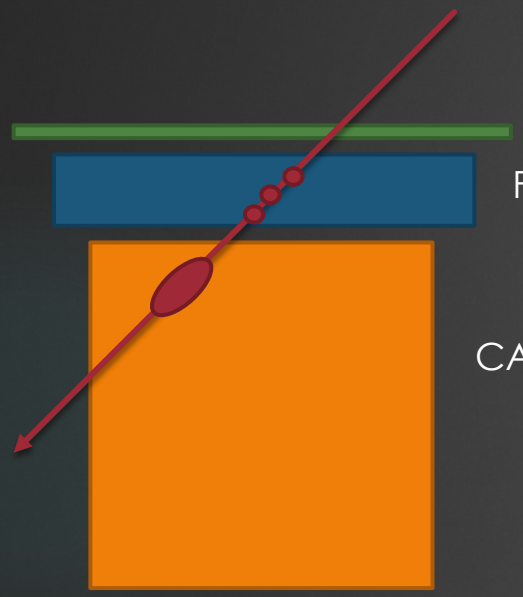
Trigger Logic

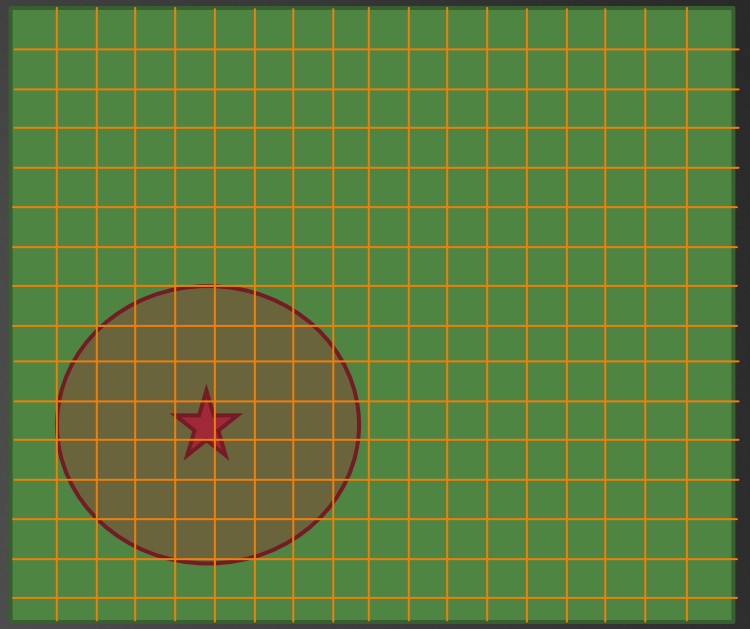
The PSD Veto signal should be provided after a FIT or a LE-CALO Trigger do accept or reject the "gamma-event"



PSD - VETO

FIT – 3-in-a-row trigger (< 1-5 GeV)

CALO – Low Energy trigger (> 0.5 GeV)



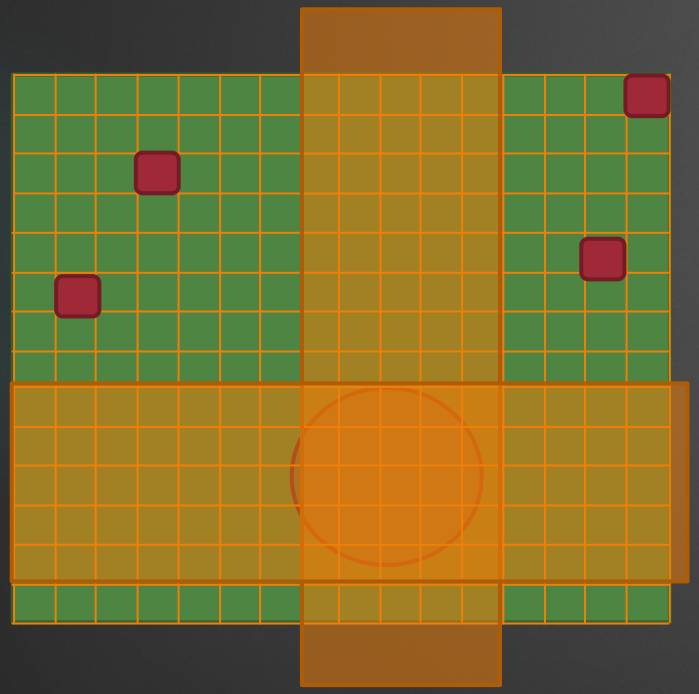
We need to define a Region of Interest (ROI) in order to look at a small number of active elements (tiles or bars) and reduce the probability of "false" veto signal due to noise and nearby charged particles (protons)

The ROI should be defined by the FIT with only the trigger infos without any tracking to be real-time

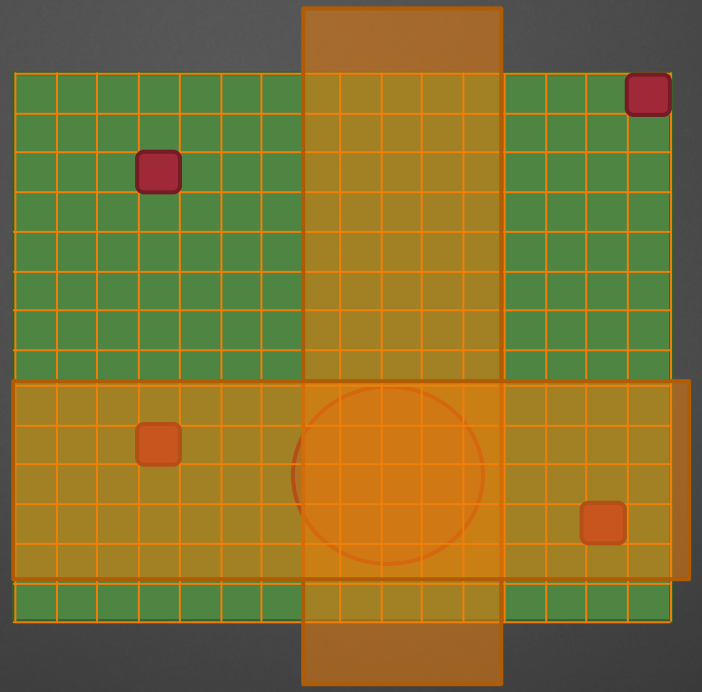
Trigger Logic

After each trigger we should provide a “map” for each of the 5 sides with the fired active elements (bar/tile) in few tens of ns

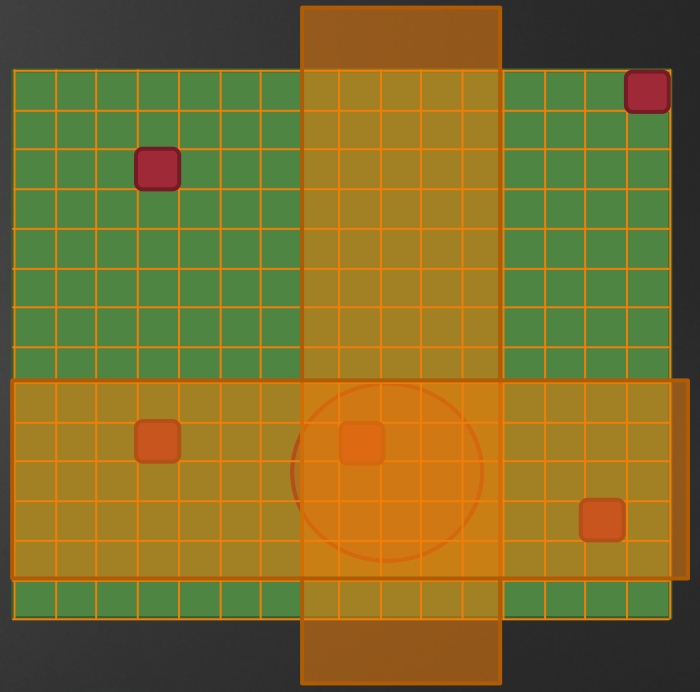
Each map should be checked against the ROI (defined from the FIT trigger infos)



Good gamma event



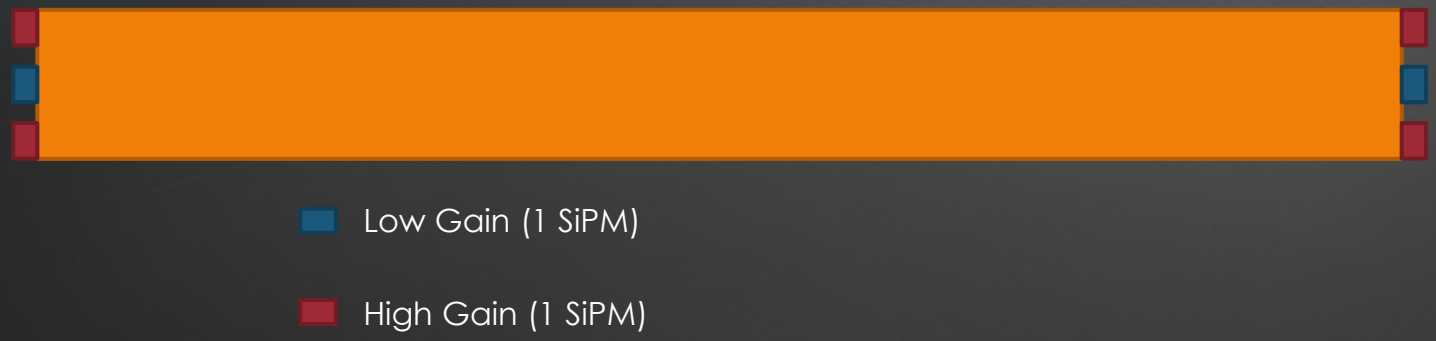
Good gamma event for tiles
Rejected gamma event fro bars



Rejected gamma event

Readout Channel

- High Gain: 3x3 mm2 SiPM(s) with High Gain Amplification for high efficiency trigger at 1/3 MIP and for light ions identification - HG
- Low Gain: 1x1 mm2 SiPM(s) with Low Gain Amplification for heavy ions identification - LG

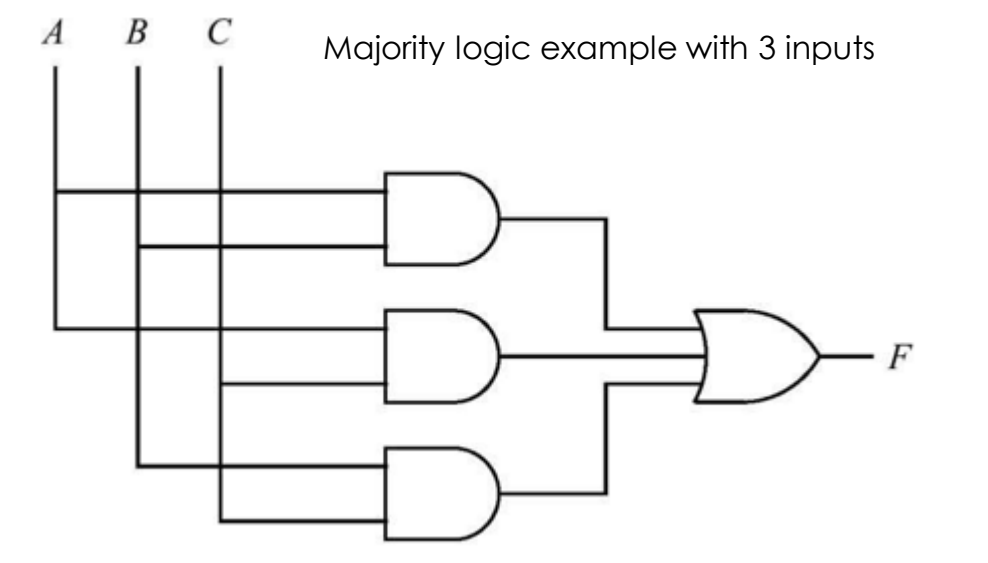


For the tiles we have enough space on the sides or on the top face to connect more than 1 SiPM to each Readout Ch.

For the bars the space on the two opposite sides is small and only 1 SiPM for Readout Ch. could be accommodated

Majority logic for each active element (tile or bar)

A Majority logic trigger could provide all the needed features for the PSD trigger



Majority logic example with 3 inputs

The Majority logic trigger have the following advantages:

1. Rejection of spurious triggers due to dark counts (AND gate of few tens of ns – SiPM dependent)
2. Redundancy: even if we lost one readout channel the Veto signal could be asserted from the other channels
3. For bars: if we put two readout channel on each side of the bar we should not lose events that cross the bar near one end and that produce a low signal in the opposite end

The majority logic should be implemented at FPGA level and should provide a signal in hundred of ns after the main trigger.