EIC silicon technology choice

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on behalf of the EIC Silicon Consortium

ATHENA Tracking WG meeting

Tuesday 1 June 2021

Tracking requirements from physics

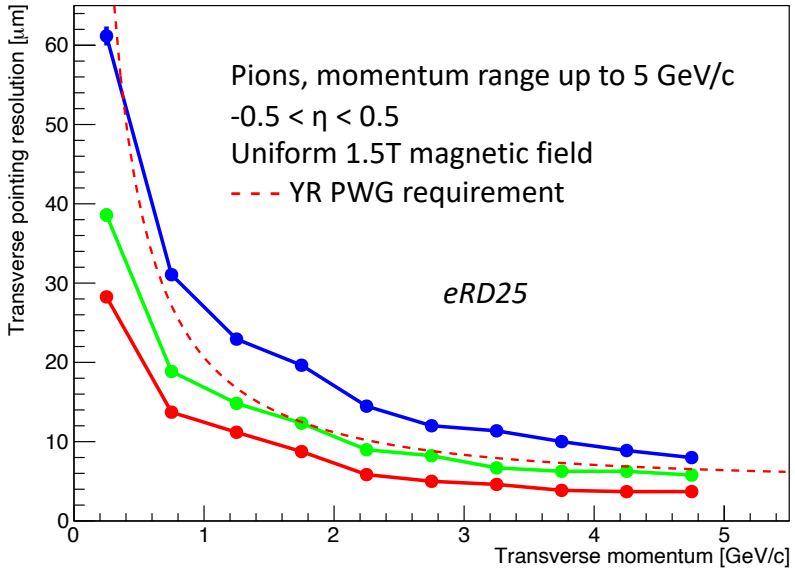
Tracking requirements from PWGs						
			Momentum res.	Material budget	Minimum pT	Transverse pointing res.
η						
-3.5 to -3.0	Central Detector	Backward Detector	σp/p ~ 0.1%×p ⊕ 0.5%	~5% X0 or less	100-150 MeV/c	
-3.0 to -2.5					100-150 MeV/c	dca(xy) ~ 30/pT μm ⊕ 40 μm
-2.5 to -2.0			σp/p ~ 0.05%×p ⊕ 0.5%		100-150 MeV/c	dca(xy) ~ 30/pT μm ⊕ 20 μm
-2.0 to -1.5					100-150 MeV/c	
-1.5 to -1.0					100-150 MeV/c	
-1.0 to -0.5		Barrel	σp/p ~ 0.05%×p ⊕ 0.5%		100-150 MeV/c	dca(xy) ~ 20/pT μm ⊕ 5 μm
-0.5 to 0						
0 to 0.5						
0.5 to 1.0						
1.0 to 1.5		Forward Detector	σp/p ~ 0.05%×p ⊕ 1%		100-150 MeV/c	dca(xy) ~ 30/pT μm ⊕ 20 μm
1.5 to 2.0					100-150 MeV/c	
2.0 to 2.5					100-150 MeV/c	
2.5 to 3.0			σp/p ~ 0.1%×p ⊕ 2%		100-150 MeV/c	dca(xy) ~ 30/pT μm ⊕ 40 μm
3.0 to 3.5					100-150 MeV/c	dca(xy) ~ 30/pT μm ⊕ 60 μm

From YR 11.2.2 at arXiv:2103.05419

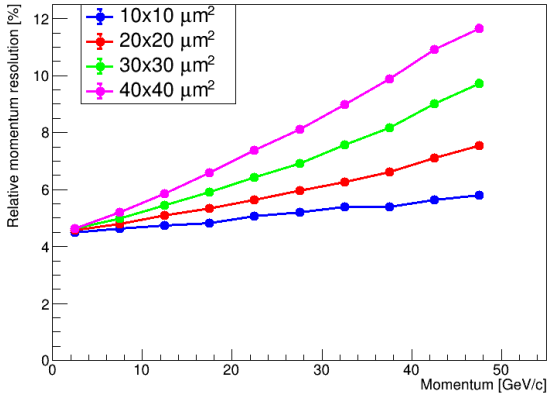
- Silicon requirements:
  - Spatial resolution:
    - ~5 μm in tracking layers and disks (~20 μm pixel pitch)
    - ~3 μm in the vertex layers (~10 μm pixel pitch)
  - Material budget:
    - <0.8/0.3% X/X0 per layer/disk,
    - < 0.1% X/X0 per vertex layer
  - Power consumption 20 - 40 mW/cm^2
  - Integration time ~2 μs

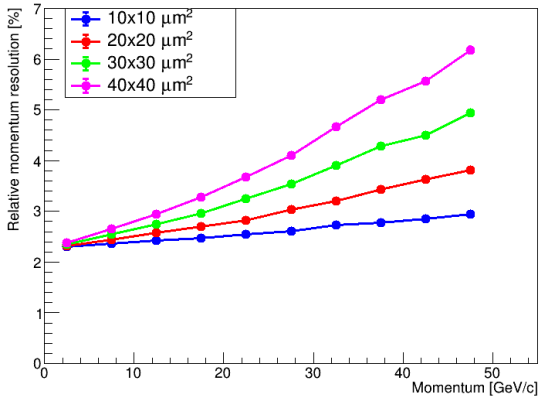
Simulation driven technology choice

- Pre-YR simulations showed the need for high granularity and low material budget



	Green	Blue	**Red (ITS3 derived EIC SVT)**
Beam pipe radius [mm]	18	**31**	**31**
x/X0 vertex	0.3%	0.3%	**0.05%**
x/X0 tracking layers	0.8%	0.8%	0.8%
Pixel pitch [um]	20	20	**10**





Forward region studied; η = 3
Single electrons fired from centre
Magnetic field: uniform 1.5 T and 3 T
Vertex layers and disks: 0.3% x/X0
Tracking layers: 0.8% x/X0
Beam pipe radius: 18 mm
See H. Wennlöf at http://cern.ch/go/xKk6

YR baseline concepts performance

- Transverse pointing resolution: requirements satisfied at both 1.5T and 3T at all pseudo-rapidity
- Relative momentum resolution: requirements better satisfied for the higher field value and in the central pseudo-rapidity region

Hybrid, H. Wennlöf, Birmingham

Layer	Length	Radial position
Layer 1	420 mm	36.4 mm
Layer 2	420 mm	44.5 mm
Layer 3	420 mm	52.6 mm
Layer 4	840 mm	133.8 mm
Layer 5	840 mm	180.0 mm
TPC start	2110 mm	200.0 mm
TPC end	2110 mm	780.0 mm

(a) Barrel region

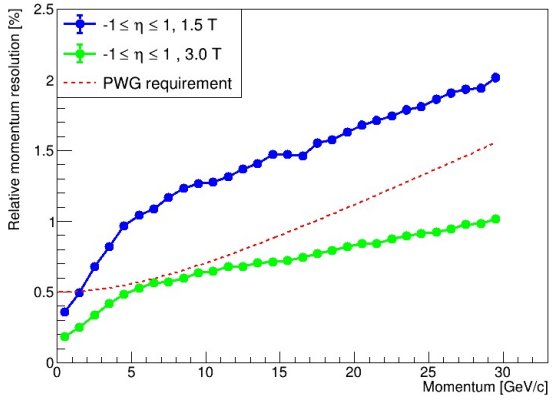
Disk	z position	Inner radius	Outer radius
Disk 1	220 mm	36.4 mm	71.3 mm
Disk 2	430 mm	36.4 mm	139.4 mm
Disk 3	586 mm	36.4 mm	190.0 mm
Disk 4	742 mm	49.9 mm	190.0 mm
Disk 5	898 mm	66.7 mm	190.0 mm
Disk 6	1054 mm	83.5 mm	190.0 mm
Disk 7	1210 mm	99.3 mm	190.0 mm

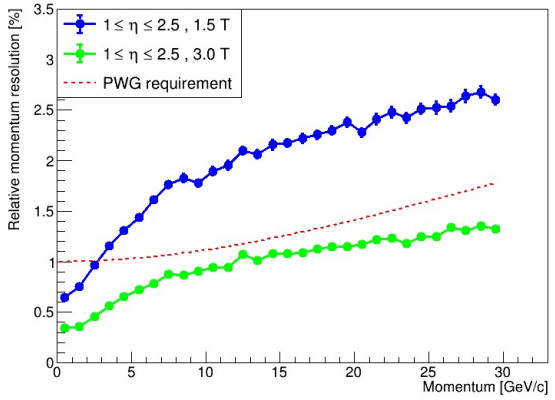
(b) Disk region

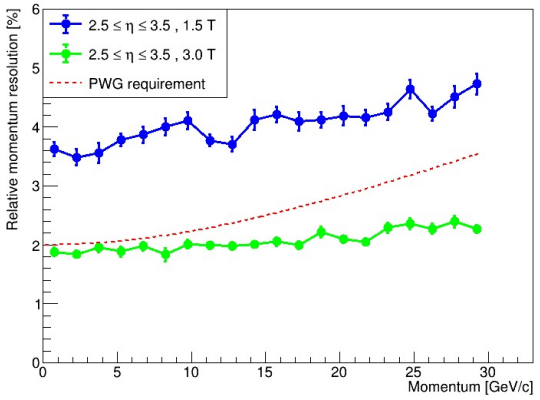
10μm pixel pitch

$x/X_0 = 0.05\%$ per vertexing layer (1 – 3)
$x/X_0 = 0.55\%$ per tracking layer (4 and 5)
$x/X_0 = 0.24\%$ per disk (1 – 7)

The material budget figures from







Physics requirements present a challenge in the forward regions, despite the low traversed mass and 10μm pixel pitch

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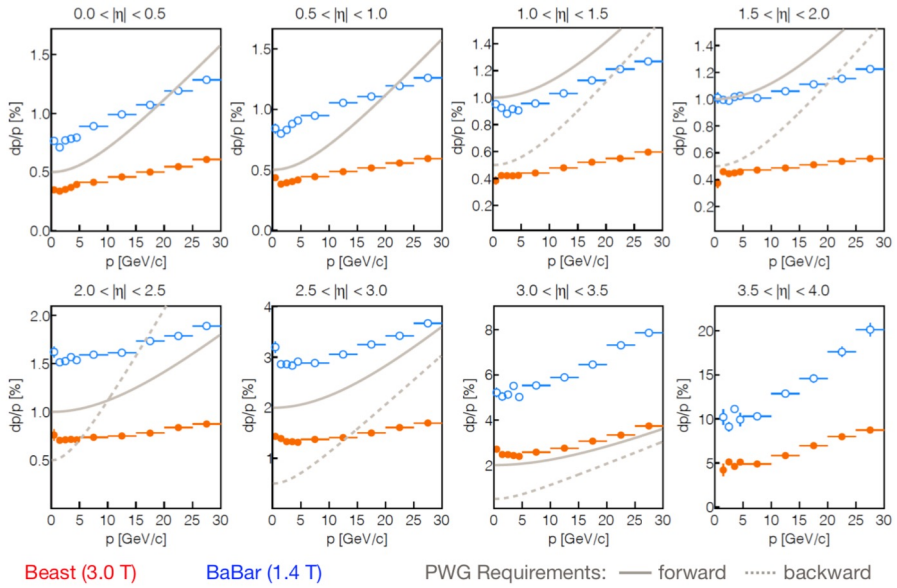
All-silicon, R. Cruz-Torres, LBNL

Barrel layer	radius [cm]	length along z [cm]
1	3.30	30
2	5.70	30
3	21.00	54
4	22.68	60
5	39.30	105
6	43.23	114

Disk number	z position [cm]	outer radius [cm]	inner radius [cm]
-5	-121	43.23	4.41
-4	-97	43.23	3.70
-3	-73	43.23	3.18
-2	-49	36.26	3.18
-1	-25	18.50	3.18
1	25	18.50	3.18
2	49	36.26	3.18
3	73	43.23	3.50
4	97	43.23	4.70
5	121	43.23	5.91

10 μm pixel pitch, x/X0 = 0.3% per layer, disk



Physics requirements present a challenge in the forward regions, despite the low traversed mass and 10μm pixel pitch

ALICE ITS3 sensor

- The ALICE ITS3 project aims at developing a new generation MAPS sensor at the 65 nm node with extremely low mass for the LHC Run4 (HL-LHC)

ITS3 sensor

- Specifications meet or even exceed the EIC requirements
- Higher granularity (10 μm pixel pitch) and lower power consumption (<20mW/cm^2) with respect to pre-CD0 simulation baseline (that was ITS2/ALPIDE derived)
- Also, integration time, fake hit rate and time resolution better than required at the EIC
- Sensor design optimized for high yield, stitched sensor to reach wafer-scale size (up to 28 x 10 cm^2)

ALICE

Specifications

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 μm	20-40 μm
Pixel size	27 x 29 μm	O(10 x 10 μm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 μs	~ 200 ns
Time resolution	~ 1 μs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager | ITS3 kickoff | 04.12.2019 |

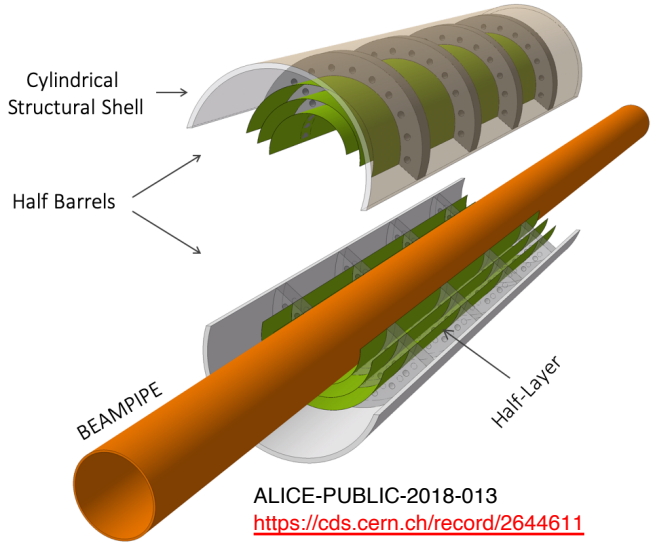
- ITS3 fallback solution: new MAPS sensor in 180 nm CMOS imaging technology
  - Decision expected this year

ALICE ITS3 detector concept

- In addition to the sensor, the ITS3 detector concept is very attractive for the vertex layers of an EIC SVT detector

ITS3 detector concept

- Three layers vertex detector, 0.12 m^2
- Truly cylindrical layers
- Design and post-processing techniques to reach an extremely low material budget of 0.05% X/X0 per layer
- Low power, wafer-scale sensor, thinned to 20-40 μm, bent around the beam pipe = air-cooling, support and services outside active area



ALICE-PUBLIC-2018-013
https://cds.cern.ch/record/2644611

Path to an EIC detector based on 65 nm MAPS

- Despite the large overlap, the EIC and ITS3 detector have some significant differences, most notably the size
  - The ITS3 is a 0.12 m^2, three layers, vertex detector
  - The proposed EIC concepts have vertex and tracking layers, disks in forward/backward direction, covering an area >10 m^2

- Projected cost and yield of stitched wafer-scale sensors not compatible with use in the EIC detector outside the vertex layers

- Tracking layers and disks will need a more conventional support structures (staves, disks) and sensor size
  - The design of a wafer-scale sensor is different from the design of a reticle-size sensor, for the same specifications → EIC sensor development needs to fork-off
    - Exploring possibility to collaborate with CERN/ALICE on this too, common interest in sensor for large area detector

The path to an EIC detector based on 65 nm MAPS thus requires to develop

1. ITS3-like vertexing layers

2. EIC variant for the staves and disks

Fallback solutions

- Development of 65 nm MAPS is at a very early stage of technology evaluation and sensor development
- Fallback solutions need to be considered in case the technology or sensor development encounter issues that would compromise the timeline and cost of the project

- Fallback option 1
  - New MAPS sensor in 180 nm developed by the ALICE ITS3 collaboration in case of problems with the 65 nm MAPS development
  - Decision expected later this year after evaluation of first 65 nm submission

- Fallback option 2
  - The only experiment ready MAPS that could deployed as a plug-and-play solution is the ALPIDE
  - This solution would not meet the requirements and impact on physics performance would need to be evaluated
  - This option would need to be replaced with an upgrade once the main development path in 65 nm is ready to allow the EIC to meet its physics goals

EIC SC consortium

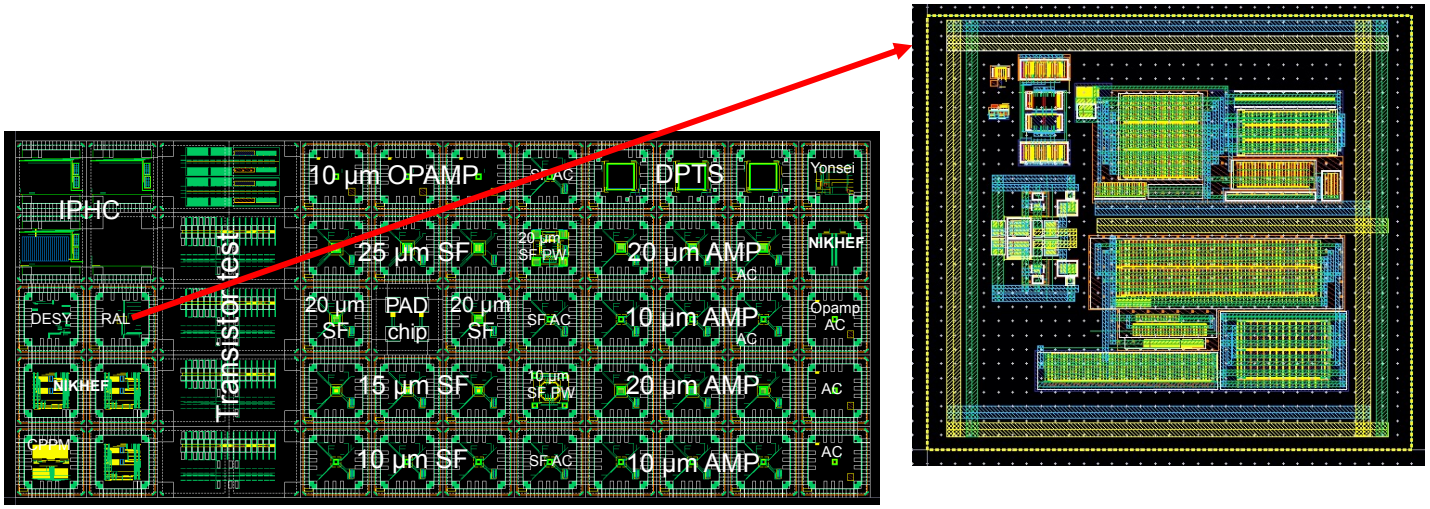
- The development of an ITS3 derived EIC vertex and tracking detector is carried out by the EIC Silicon Consortium
  - EOI: https://indico.bnl.gov/event/8552/contributions/43219/
  - LBNL, Uni Birmingham, RAL, BNL, INFN leadership
  - To join: https://lists.bnl.gov/mailman/listinfo/eic-rd-silicon-l
  - Indico: https://indico.bnl.gov/category/354/

- The EIC SC is open to institutes from different emerging collaborations interested to work on the proposed sensor solution for their specific EIC detector implementation
  - Similar concept to the CERN RD groups (such as RD50, RD53)
  - This will maximise the successful delivery of the technology with the lowest cost to the project

- Work packaged defined; work ongoing with ITS3 on sensor design, and thinning and bending
- Silicon strategy document, estimate of R&D costs, timeline of development up to CD4 drafted and shared with to the EIC project detector systems coordinators

Status of sensor development

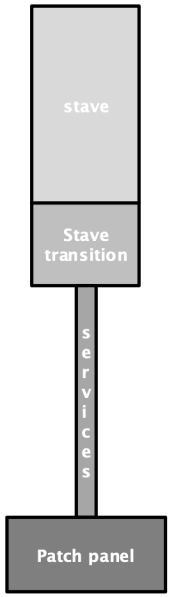
- RAL already involved in first 65 nm submission with ITS3 Work Package 2 (first EIC institute involved in EIC MAPS design at this stage!)
  - Funded via the EIC Generic Detector R&D programme, project eRD25 Silicon Tracking and Vertexing Consortium, Birmingham/LBNL/RAL



- ITS3 ER1 submission planning ongoing, including stitched matrix, submission end of 2021/beginning of 2022
  - Combination of previously planned MLR2 & ER1
- RAL+Brunel, LBNL and BNL defining contribution in discussion with ITS3 sensor design group (Walter Snoeys, Gianluca Aglieri Rinella)

Ongoing work on services and supports

- Material estimates for services and supports available (extrapolation based on ALICE ITS2 with ITS3 sensor power consumption)



	Stave X/X0	Stave transition (per 100 cm^2 of Si surface)	Services (per 100 cm^2 of Si surface)	Patch panel (per 100 cm^2 of Si surface)
ITS3 like vertexing	~0.1%	6.66 cm^3 of material with X/X0 of 0.0684 per traversed cm	2.96 cm^2 cross section with X/X0 of 0.022 per traversed cm	4.32 cm x 1cm x 1 cm with 0.102 X/X0 per traversed cm
ITS3 like barrel (up to 1.5m length)	0.55 %	4.286 cm^3 of material with X/X0 of 0.0684 per traversed cm	1.905 cm^2 cross section with X/X0 of 0.022 per traversed cm	2.778cm x 1cm x 1 cm with 0.102 X/X0 per traversed cm
ITS3 like disc (up to 60 cm diameter)	0.24%	6.66 cm^3 of material with X/X0 of 0.0684 per traversed cm	2.96 cm^2 cross section with X/X0 of 0.022 per traversed cm	4.321 cm x 1cm x 1 cm with 0.102 X/X0 per traversed cm

https://indico.bnl.gov/event/8231/contributions/37955/
https://indico.bnl.gov/event/9080/contributions/40920/

- Detailed review of powering options including possible configurations with DC-DC converter or serial powering, estimate of material budget and timescale for development carried out and summarised in a document
  - https://www.eicug.org/web/sites/default/files/Powering-options-for-an-EIC-silicon-tracker.pdf

Elements of the EIC Silicon Acquisition Strategy (1/2)

"Strategy Document for Silicon Tracking and Vertexing for the EIC",
Proponents: G. Contin, G. Deptuch, L. Greiner, L. Gonella, P. Jones, I. Sedgwick, E. Sichtermann,
23 April 2021
Document circulated to Elke and Rolf

- The specified ALICE ITS3 65 nm MAPS sensor has performance that meets or even exceeds the EIC tracking and vertexing requirements as demonstrated in simulations presented in the Yellow Report and in the eRD25 proposal and report.

- The development of the EIC tracking and vertexing system can leverage on a well-funded, large effort at CERN, open to non-ALICE members to contribute to the R&D to develop and use the technology for other applications.

- The ALICE ITS3 approach to develop an ultra-low mass vertex detector is particularly attractive for the EIC vertex layers that could be easily designed with the same technologies developed for the ITS3 detector.

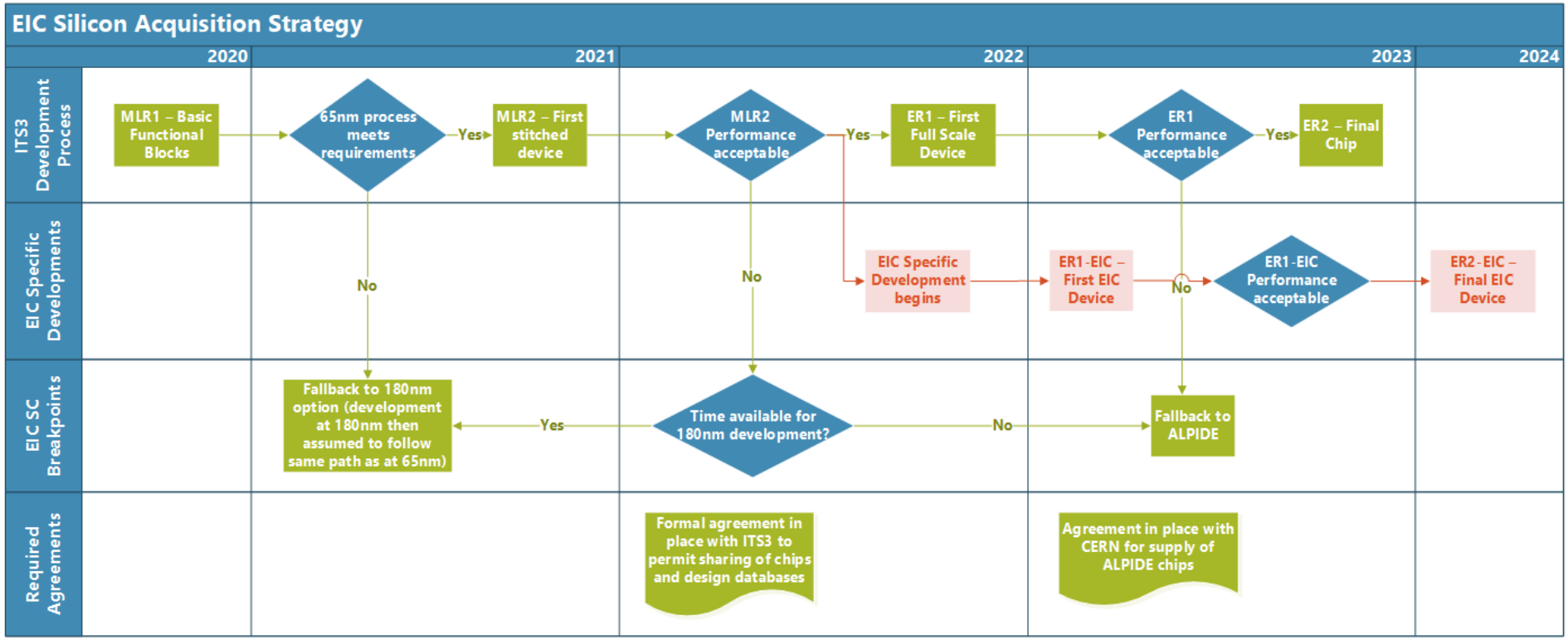
Elements of the EIC Silicon Acquisition Strategy (2/2)

- The schedule of the ITS3 and EIC projects are well aligned.
  - Up to TDR, construction and installation are on a different time scale.

- The ITS3 project has a 180 nm MAPS sensor fallback solution in case the main 65 nm development would not prove feasible on the required me scale. The decision will be taken later this year after results from the first submission in 65 nm.

- A large group of EIC institutes have expressed interest in this proposed development and joined to form the EIC Silicon Consortium, providing the required broad base of expertise for the full detector implementation. Some of these institutes are already working with ITS3 on sensor development.

EIC Silicon Acquisition Strategy flowchart



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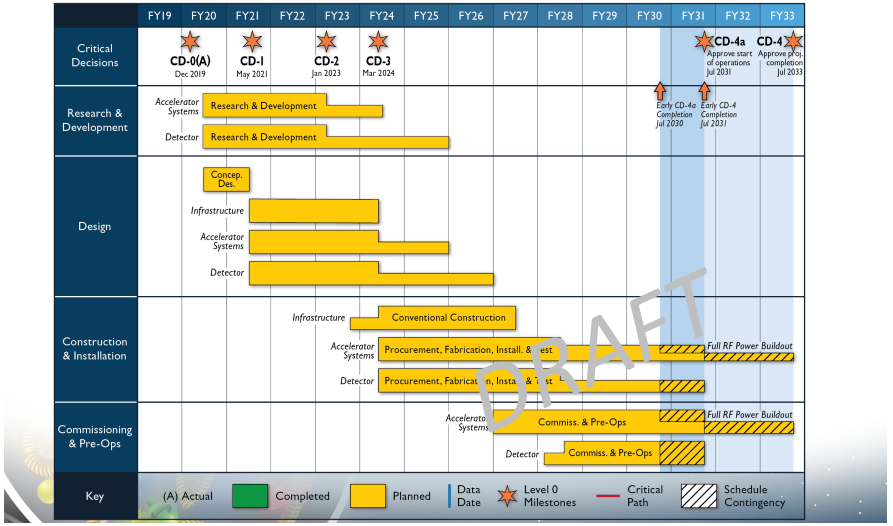
Timeline

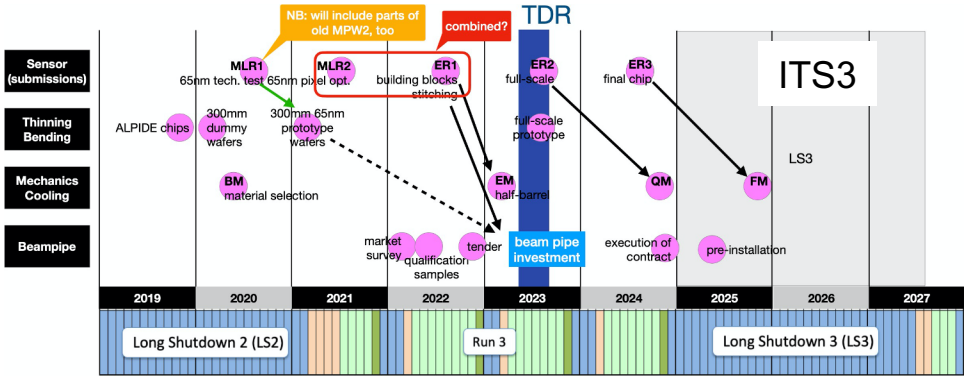
- The timeline for the development is tied to the sensor development

Year	Main tasks
2021	Submission of the first MLR.
2022	Submission of the first engineering run (ITS).
2023	Submission of the first engineering run (EIC variant), second engineering run (ITS3).
2024	Submission of the second engineering run (EIC variant).
2025	Integration of prototype sensors into disc and stave. Possible contingency submission of EIC variant.

Proposed Schedule – New!



See J. Yeck,
https://indico.bnl.gov/event/10825/contributions/46080/
Kick-off meeting for an EIC detector at IP6, March 2021



Timeline - detailed

- The timeline for the development is tied to the sensor development

Year	Detailed tasks
2021	• MLR1 submission • Testing and characterization of MLR1 • Sensor design for ITS3 ER1 • R&D into powering, stave/disc construction, cooling, overall infrastructure
2022	• Sensor design for ITS3 ER1 • ITS3 ER1 submission • Testing and characterization of ITS3 ER1 • R&D + prototyping into powering, stave/disc construction, cooling, overall infrastructure
2023	• Testing and characterization of ITS3 ER1 and assessment of yield • Assessment and planning for EIC sensor fork of ITS3 design • Fork off sensor design and work on EIC variant for staves and discs (may move to next year depending on results) • ER submission for EIC variant sensor (EIC ER1) for staves and discs • Detailed prototyping into powering, stave/disc construction, cooling, overall infrastructure • Investigation of adaptation of ITS3 design for use in EIC vertex layers (different radii, # layers, services from both ends to meet length requirements, etc.) with ITS ER1
2024	• Testing and characterization of EIC ER1 and assessment of yield • Si design for EIC ER2 • EIC ER2 submission for EIC variant sensor for staves and discs • Detailed prototyping into powering, stave/disc construction, cooling, overall infrastructure using EIC ER1 prototypes • Adaptation of ITS3 design for use in EIC inner layers with ITS2 ER2 (or integration of design into EIC ER2 if necessary).
2025	• Testing and characterization of EIC ER2 and assessment of yield • Complete stave and disks prototypes with EIC ER2 • Vertex layers prototypes with ITS2 ER3

Backup slides

ITS3-derived EIC SVT

- 65 nm MAPS sensor, 10 µm pixel pitch, <20mW/cm^2
- Adopt ITS3 concept for the EIC vertex layers
  - Wafer scale sensor, thin and bent around beam pipe, <0.1% X/X0
- EIC variant for the staves and discs
  - Sensor size vs yield optimisation (stitched but not wafer scale), conventional stave and disk structures, work on cooling, structure and services to meet X/X0 (estimated 0.55% X/X0 in barrel layers, 0.24% X/X0 in disks)

ALICE

Specifications

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
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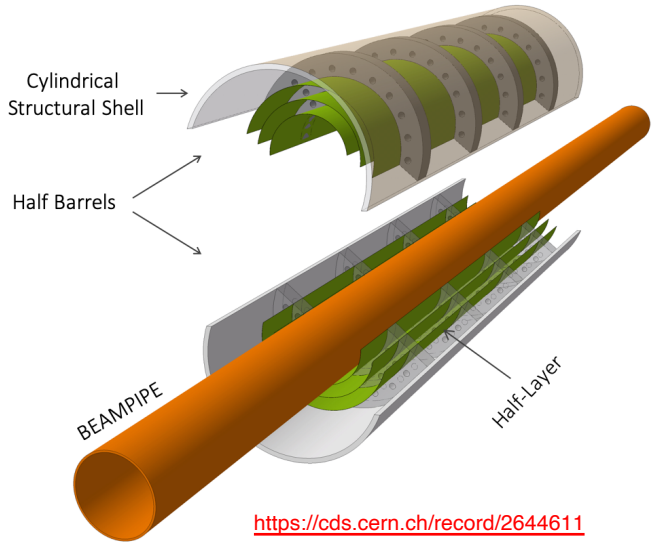
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

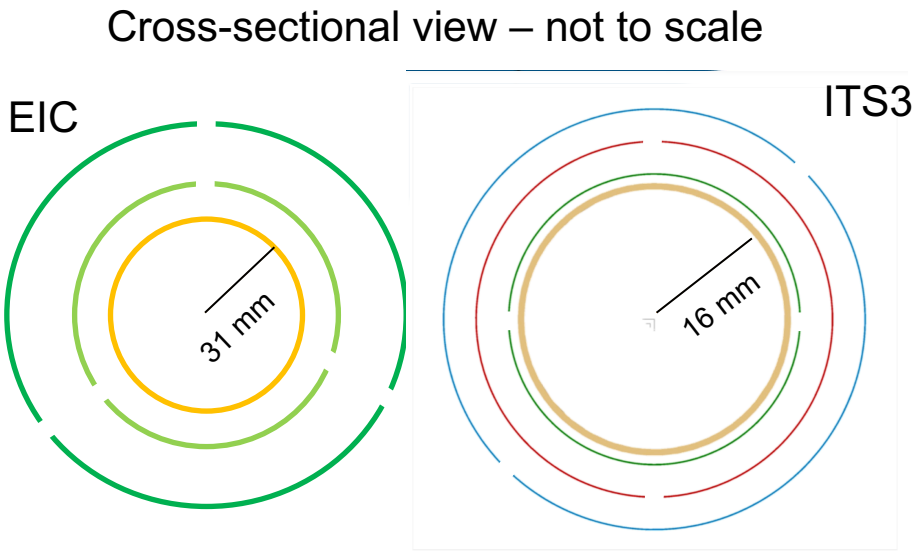
M. Mager | ITS3 kickoff | 04.12.2019 |

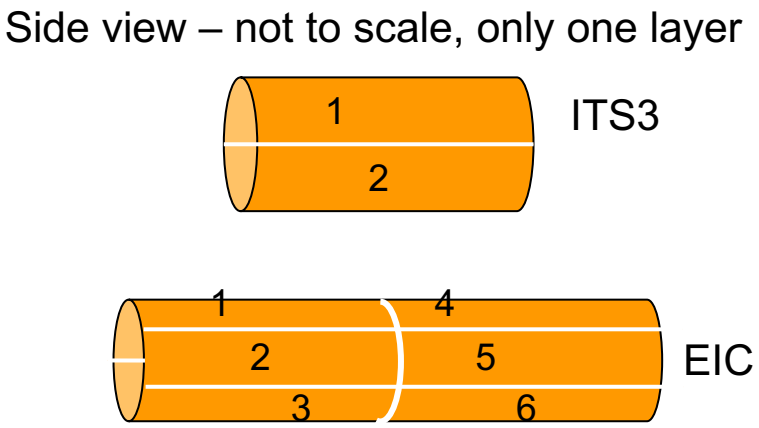


https://cds.cern.ch/record/2644611

EIC SVT strawman design – Vertex layers

- Use ITS3 detector sensor and detector layout, adapted to larger radii and length of the EIC vertex layers
  - Three bent sensors needed to cover the larger radii
  - Along the length, two sensors may be needed to cover the length depending on detector configuration/further optimisations
  - In total, three to six sensors per layer (instead of two in ITS3)
- Deploy wafer-scale sensor as in ITS3 (with different length if needed)
- Material budget X/X0 ~0.05% per layer as in ITS3
- Services may come out on both sides of EIC vertex layers





EIC SVT strawman design – Tracking layers and disks

- Staves and discs will be based on a forked EIC specific sensor design based on the ITS3 sensor
  - Same functionality and interfaces as ITS3 sensor, stitched but not wafer-scale
  - Stitched sensor layout/size will need to be optimized to provide the coverage needed for each stave and disk
  - Optimization will consider yield estimates from first engineering run
- Staves derived from ITS2 structures; discs composed of overlapping staves or low mass CFC support discs
- Material budget estimate
  - Tracking layer X/X0 ~0.55%
  - Disks X/X0 ~0.24 %