Silicon Trackers (part2)

RD_FCC Referee meeting
3 June 2021

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Università di Milano and INFN

For the Silicon Tracker community

(MILANO + PISA)

Sezione di Milano

UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

Silicon Trackers

- Requirements critical for the VTX part:
  - high granularity
  - low material
  - low power consumption
- Large area tracker can be a bit less challenging
- Currently pursuing the same concept:
  - Depleted Monolithic Active Pixels
    - reduce material avoiding double strip layers
    - large scale production at various CMOS foundries
  - Exploring different technology nodes

CEPC Detector R&D Project

1.2 ARCADIA CMOS MAPS

Document Responsible:	Manuel Rolo
	29/04/2020 5:00:00 PM

Manuel's presentation

CEPC Detector R&D Project

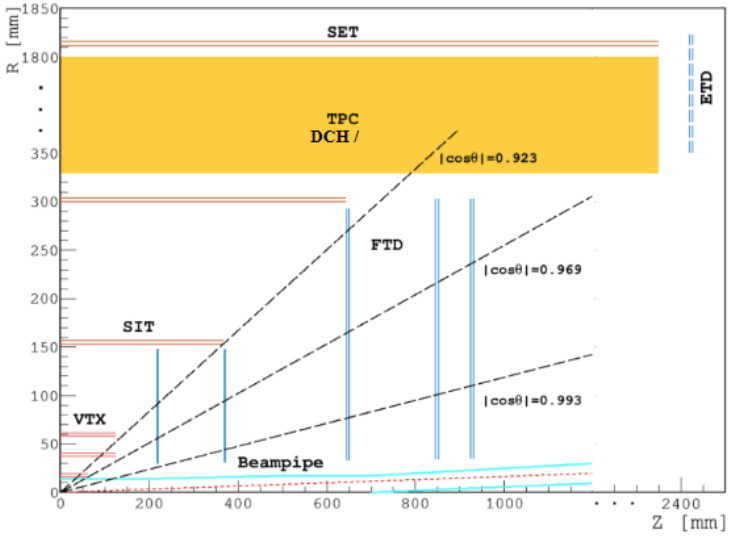
2.2 Silicon Tracker Prototype

Document Responsible:	Harald Fox, Meng Wang
Last saved by on	1/22/2021 5:40:00 AM
Revision number:	3

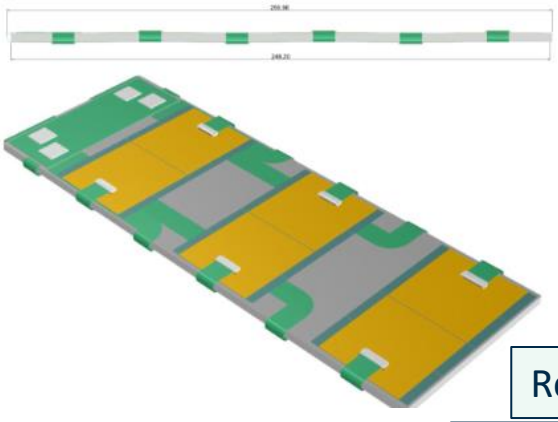
This talk

Silicon Tracker

- An effort is being started to provide a realistic mechanical layout for the tracker

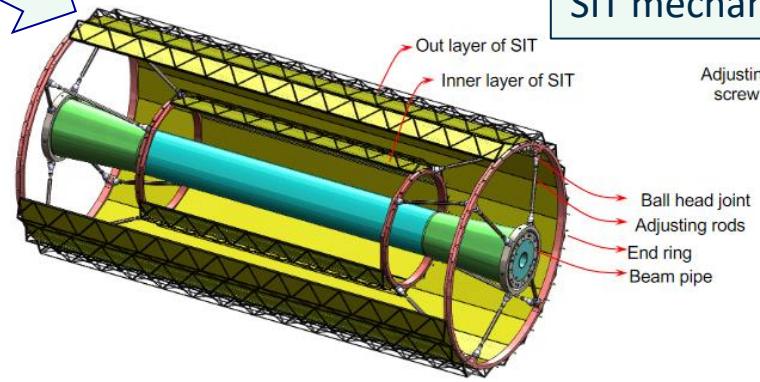


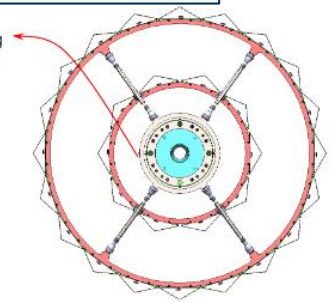
CDR conceptual layout



Realistic SET local support

SIT mechanical model

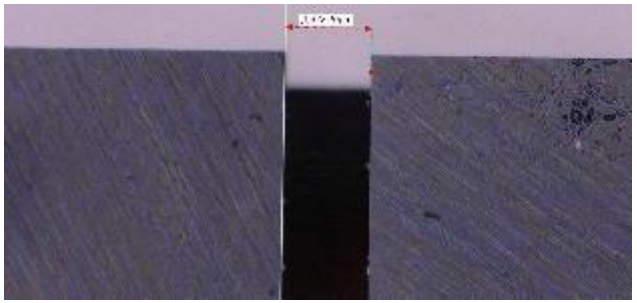


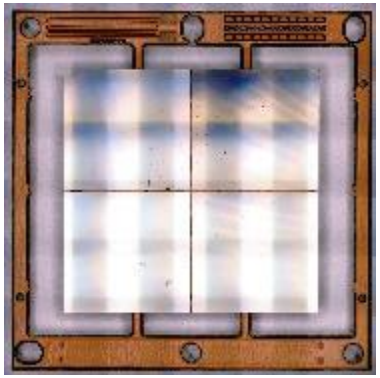


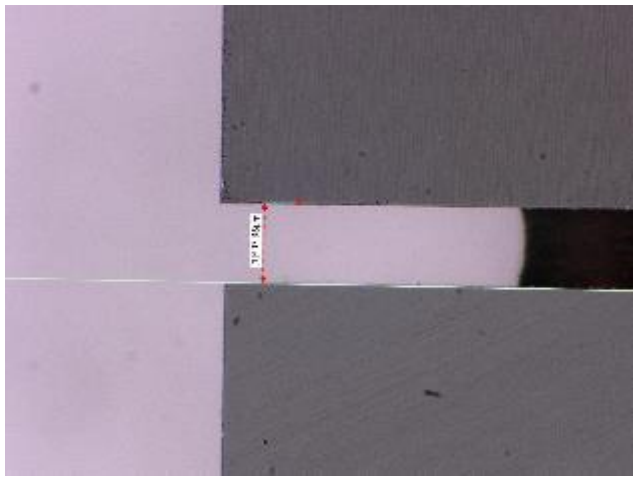
- Different layout options still open:
  - Full Si, TPC, DCH (IDEA),
    small DCH (so called 4th layout from IHEP)
- Kickoff engineering meeting on 18 March , follow-ups on 1 April and today
- Interest by the Pisa group already involved in CMS and Belle2
  - design of a lightweight stave structure

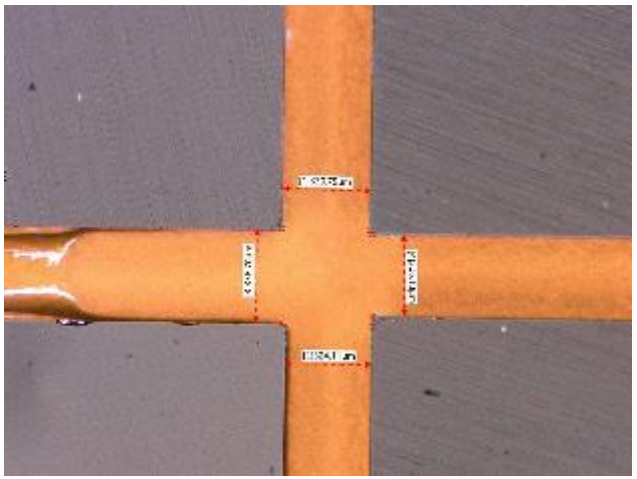
Sensor prototyping with ATLASPIX3

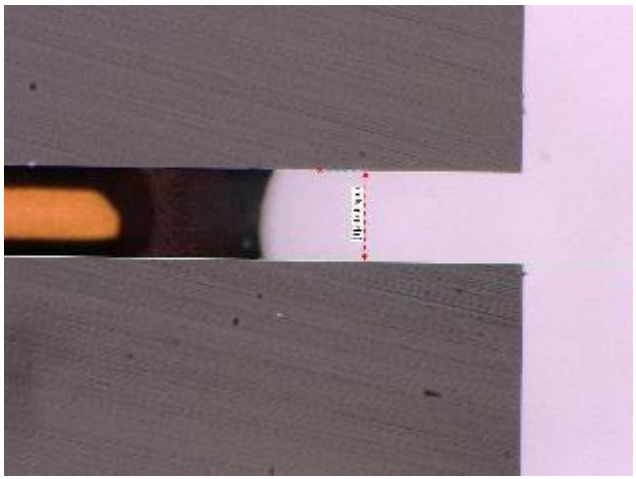
- First module assembled using the 2020 Hybrid
- Kept some safe margin to avoid clashes
  (300 um instead of nominal 200 um)

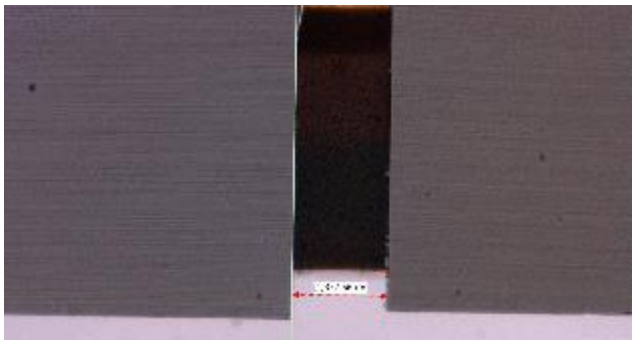








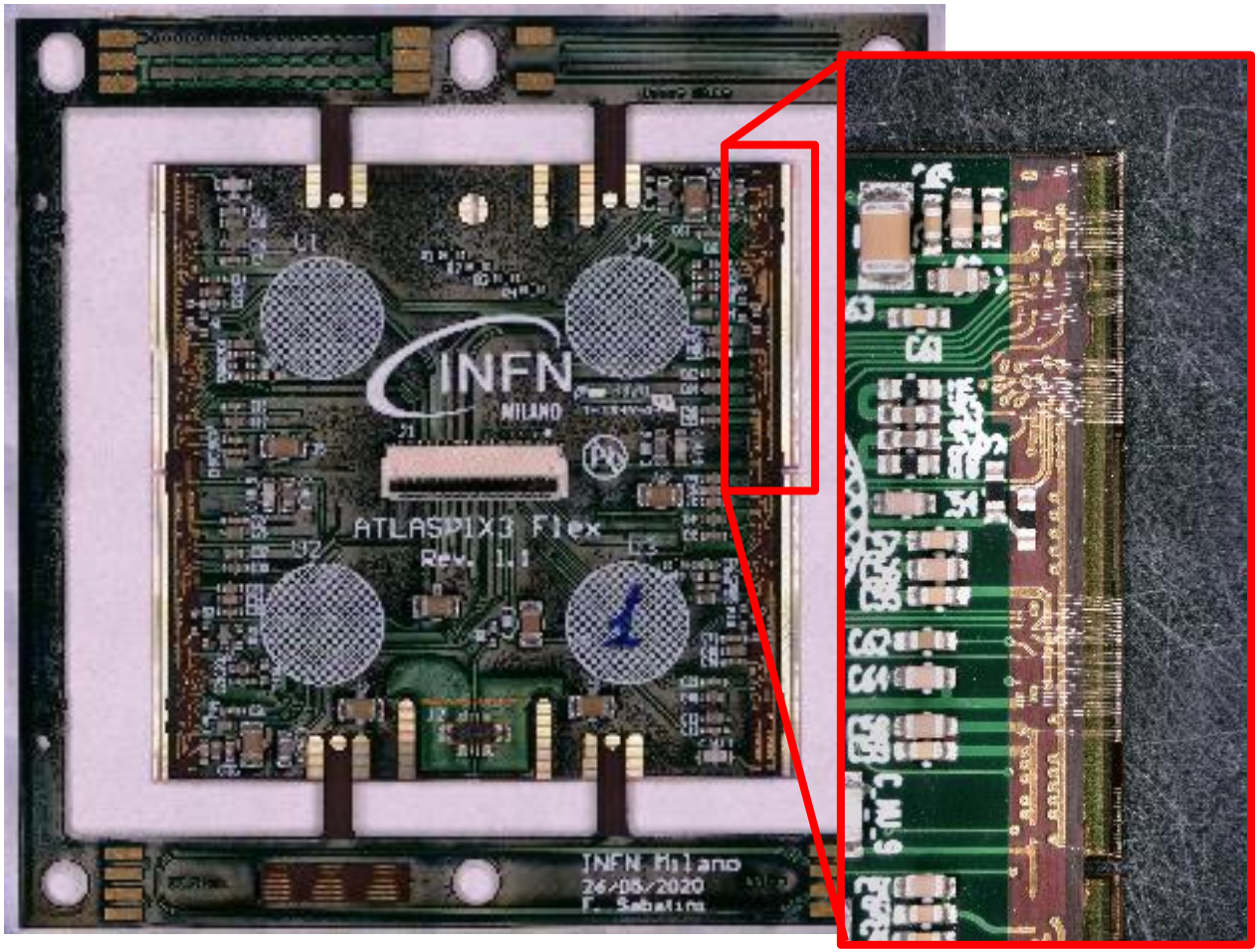




- parallelism acceptable:
  max 50 um variation between the two chip sides

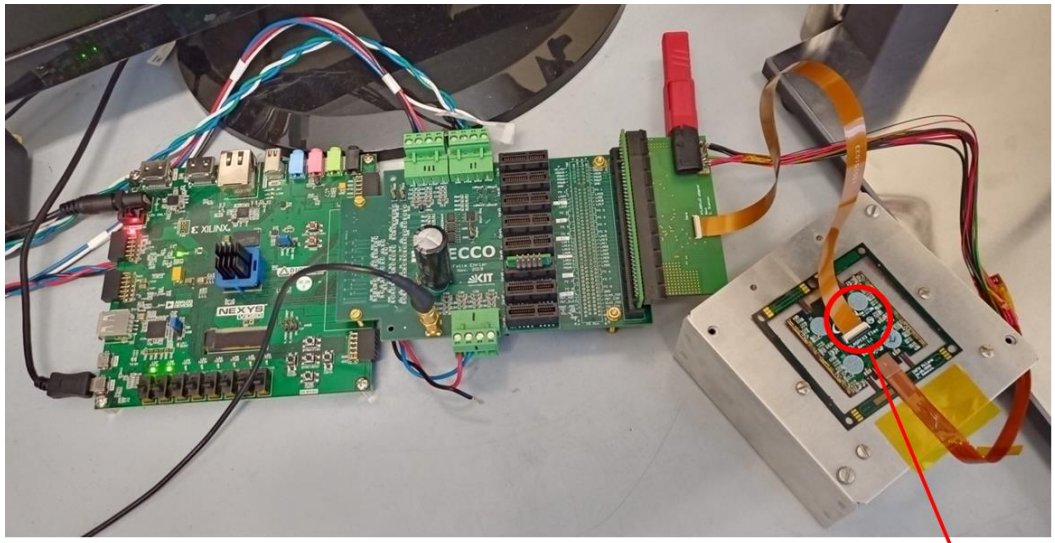
Sensor prototyping with ATLASPIX3

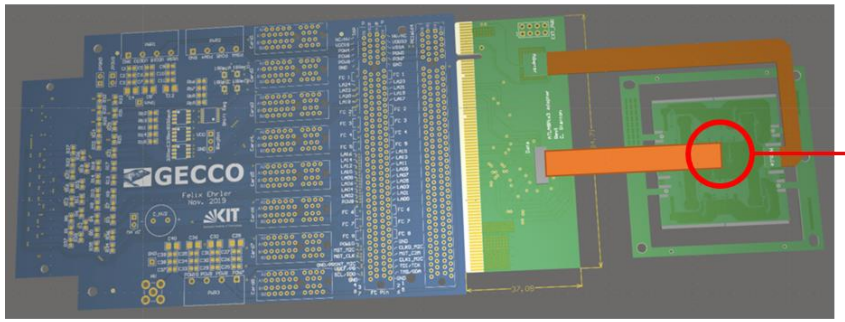
- Probing of the supply voltages has been performed on the flex without CMOS modules:
  - HV, GNDA, VDDD, VLVDS and VGATE
- Probing of the continuity for all signals from the FMC connector to the flex circuit:
- Matched impedance and continuity for all signals
- The following signals could be probed and matched the expected results:
  - CkRef_N/P, Cmd_N/P, ExtTrigger_N/P
  - EnCDR, useSPI, CmdClockInvert, TakeFast, untriggeredROen, EnPLL, SelExt

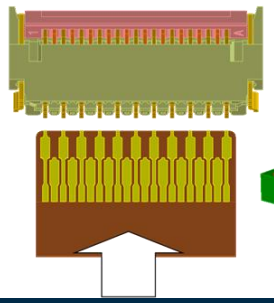


Preparing for module tests

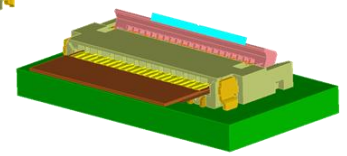
- At the moment we are merging the firmware for the triggered readout (single chip) and the firmware for the telescope's "hit driven" readout to be able to configure 4 chips individually.
  - The location of some signals on the adapter card's pins wasn't matching the one from the GECCO board:
    - Signals have been re-assigned to the correct pins location
    - Unused signals in the flex circuit have been deleted
  - The last changes have been completed to obtain a working bitstream from the telescope's "hit driven" firmware







Molex cable



Next steps (on 2021 budget)

- An updated version ATLASPIX3.1 is available
  - fixes on the main VDDA/VDDD regulators
  - on-chip command-clock-recovery being debugged
  - preliminary steps to start new flex design to prototype more realistic modules:
    - Only one LV supply (currently 3 are needed) + HV
    - Single command and control line (now using 4 to distribute also clock, trigger and reset signals)
- To simplify procurement logistics:
  - the required wafers for the prototyping program were purchased by UK groups
  - RD_FCC will instead pay the thinning and dicing
- Develop the stave design:
  - provide the design of a section of the stave to test multi module operation
  - design of full stave structure and FEA study the mechanical stability