ARCADIA

Status Report

RD_FCC Meeting with Referees
June 3rd, 2021

Istituto Nazionale di Fisica Nucleare

Manuel Da Rocha Rolo (INFN)
on behalf of the ARCADIA Collaboration

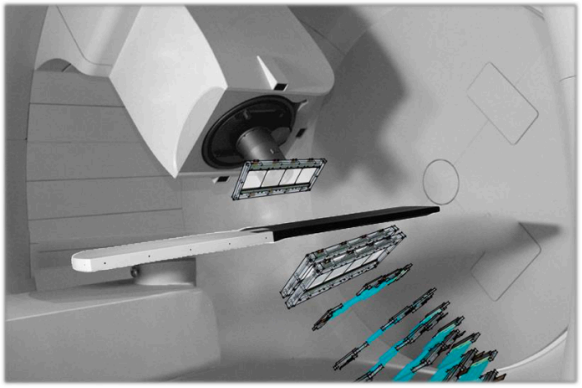
F. Alfonsi, G. Ambrosi, A. Andreazza, E. Bianco, G. Balbi, S. Beolè, M. Caccia, A. Candelori, D. Chiappara, T. Corradino, T. Croci, M. Da Rocha Rolo, G. F. Dalla Betta, A. De Angelis, G. Dellacasa, N. Demaria, L. De Cilladi, B. Di Ruzza, A. Di Salvo, D. Falchieri, M. Favaro, A. Gabrielli, L. Gaioni, S. Garbolino, G. Gebbia, R. Giampaolo, N. Giangiacomi , P. Giubilato, R. Iuppa, M. Mandurrino, M. Manghisoni, S. Mattiazzo, M. Mignone, C. Neubüser, F. Nozzoli, J. Olave, L. Pancheri, D. Passeri, A. Paternò, M. Pezzoli, P. Placidi, L. Ratti, E. Ricci, S. B. Ricciarini, A. Rivetti, R. Santoro, A. Scorzoni, L. Servoli, F. Tosello, G. Traversi, C. Vacchi, R. Wheadon, J. Wyss, P. Zuccon

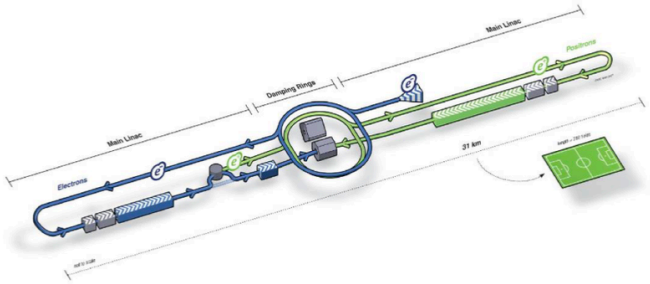
ARCADIA: CMOS DMAPS platform at INFN

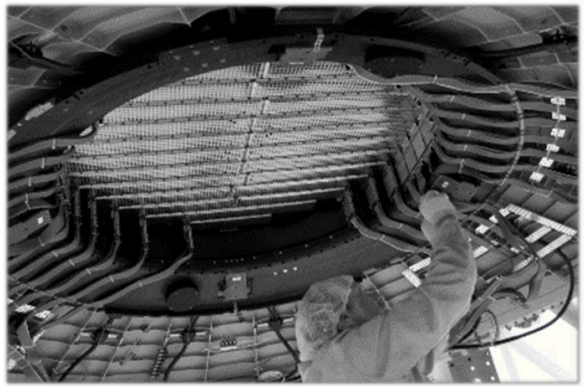
What do we want: to develop a design and fabrication platform for large-area fully-depleted CMOS sensors, at the moment targeting space, medical and future HEP infrastructures (thin sensors) and X-ray detectors (thicker sensors)

What do we need from the silicon foundry:

- access to an engineered CMOS process (already done with SEED, patented) and custom starting substrates
- access to future SPW runs for dedicated reticle size (next 3 years) and larger-than-reticle (from 2023) designs





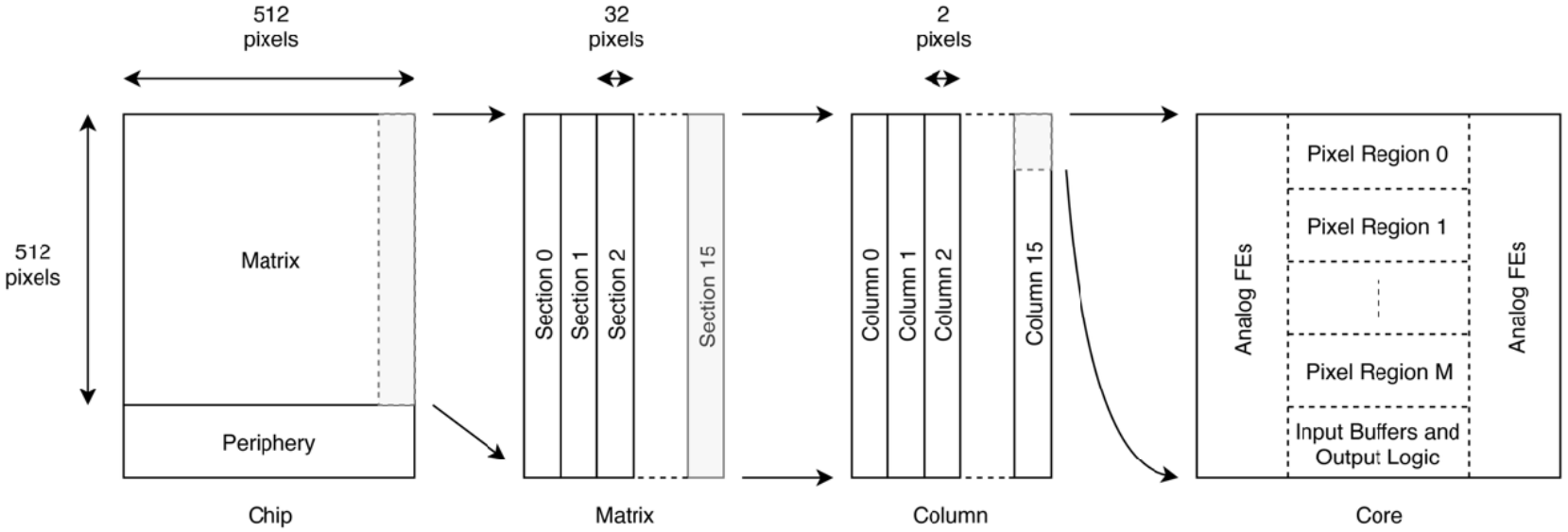


Medical
- Low power (≤ 40 mW/cm²)
- Medium rate ≈ 10 MHz – 100 MHz/cm²
- Ultra low material budget (low energy)
- Very large area (≥ 16 cm²)
- 3-side buttable design
- Low to medium rad-tolerance ≈ 10 kGy

e⁺e⁻
- Low power (≤ 40 mW/cm²)
- Medium rate ≈ 10 MHz – 100 MHz / cm²
- Very low material budget
- Large area (≥ 6 cm²)
- 3-side buttable design
- Low to medium rad-tolerance ≈ 10 kGy

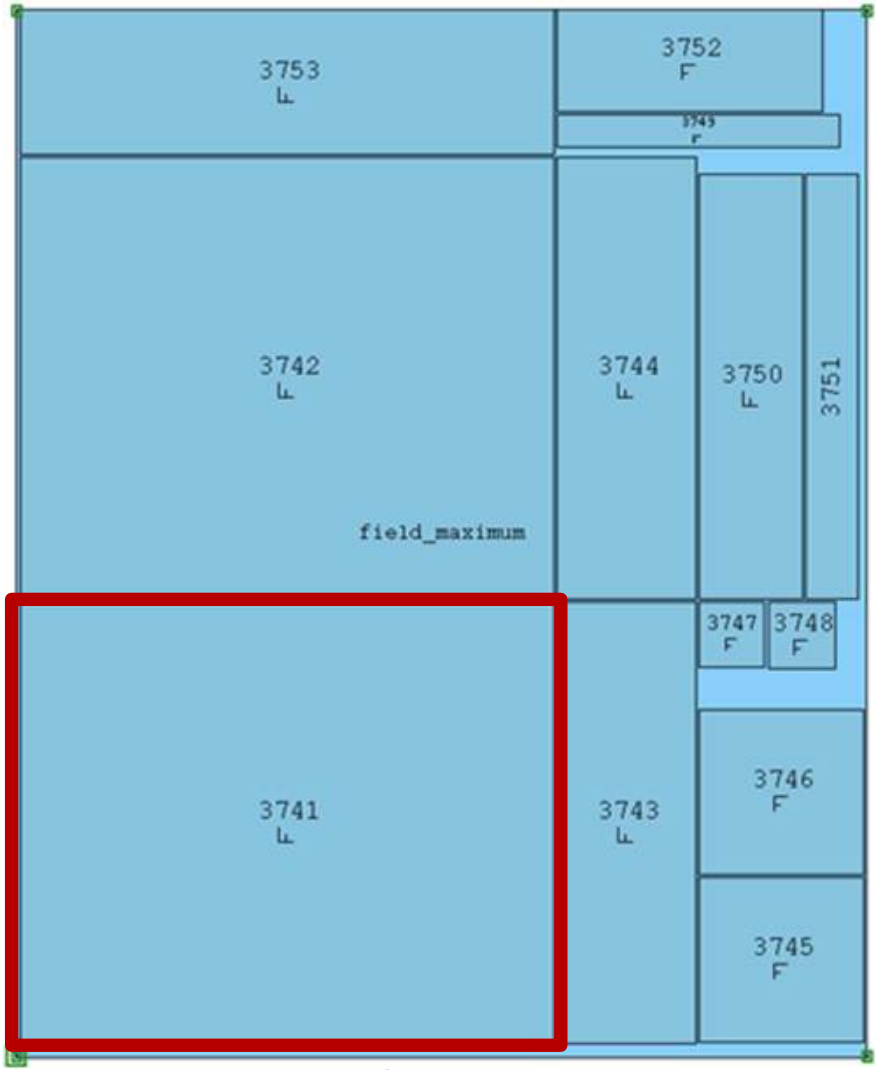
Space
- Ultra low power (≤ 10 mW/cm²)
- Very low rate ≈ kHz/cm²
- Low material budget
- Large area (≥ 6 cm²)
- 3-side buttable
- Low rad-tolerance ≈ 1 kGy

ARCADIA-MD1: Main Demonstrator Chip



- Pixel size 25 µm x 25 µm: process, back-side pattern and geometry validated in silicon (both MATISSE and pseudo-matrices, electrical, laser, radioactive source and microbeam).
- Matrix core 512 x 512, "side-abuttable" to accomodate a 1024 x 512 silicon active area (2.56 x 1.28 cm^2). Matrix and EoC architecture, data links and payload ID: scalable to 2048 x 2048*
- Triggerless binary data readout, event rate up to 100 MHz/cm^2
- First Engineering Run (SPW) with ARCADIA-MD1 by 11/2020, 2nd full CMOS maskset mid-2021 (higher data throughput, SEU protection, on-chip data compression), 3rd SPW mid-2022 with design fixes, explorative sensor and CMOS designs

ARCADIA - reticle for 1st Engineering Run



- BN3741/2: **ARCADIA-MD1a**/b
- BN3743: ARCADIA-miniD (debug)
- BN3744: ARCADIA-miniD with on-chip LDOs for large-scale yield management
- BN3745/6: MAPS and test structures for PSI
- BN3747/8: MATISSE2020 and MATISSE Low Power (front-end for space instruments)
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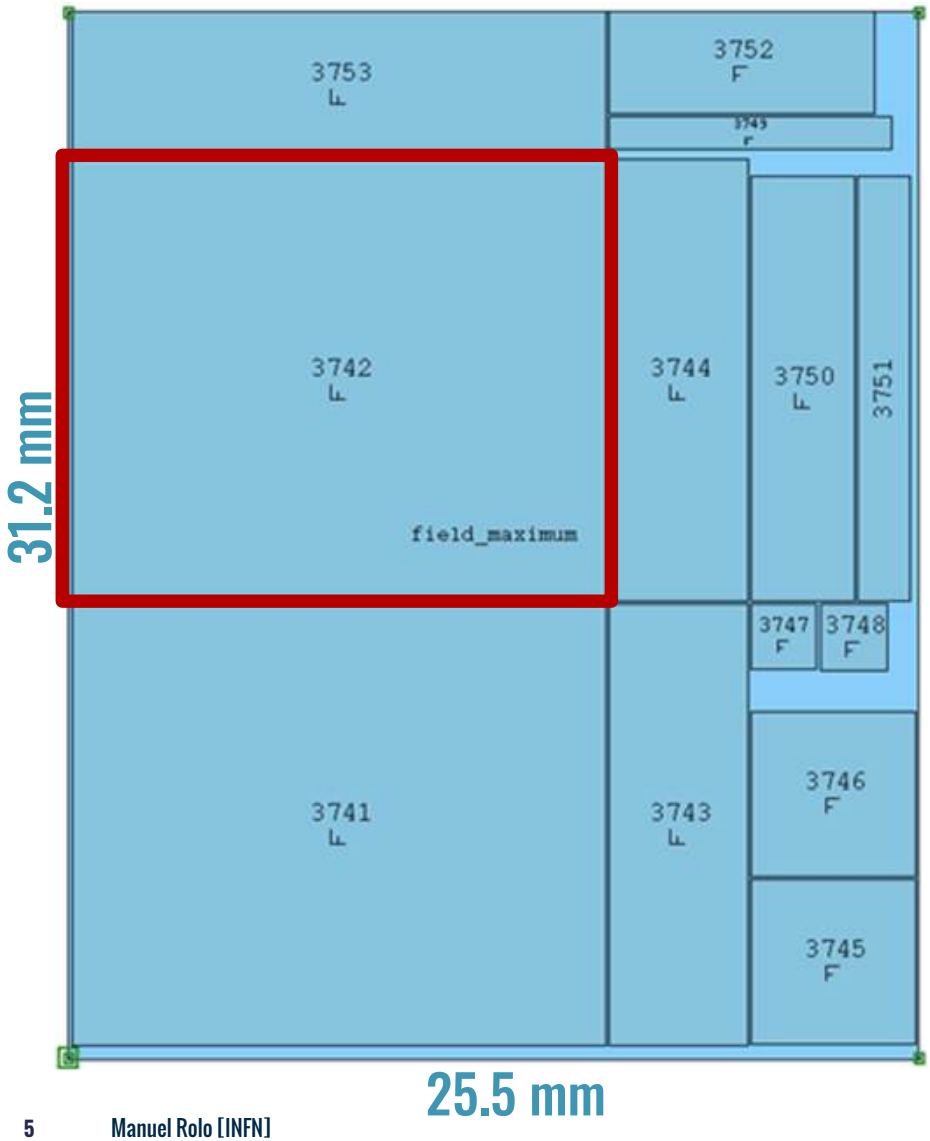

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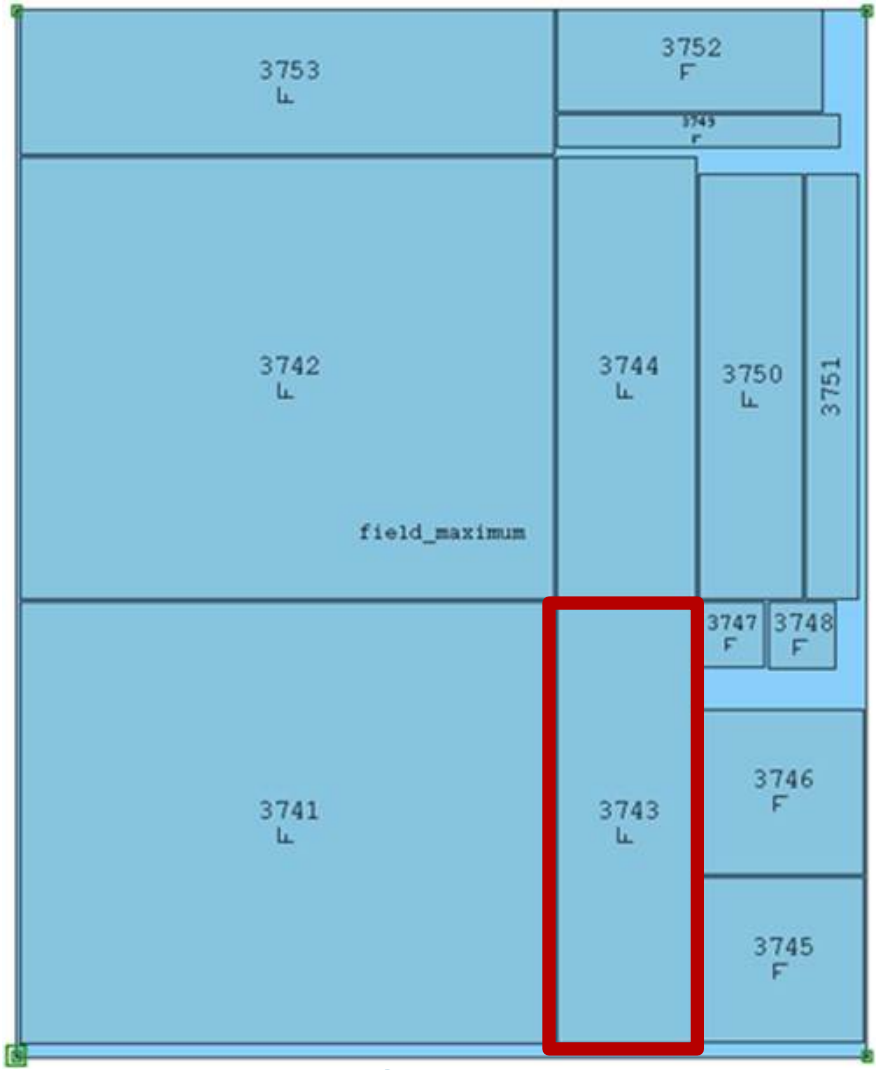

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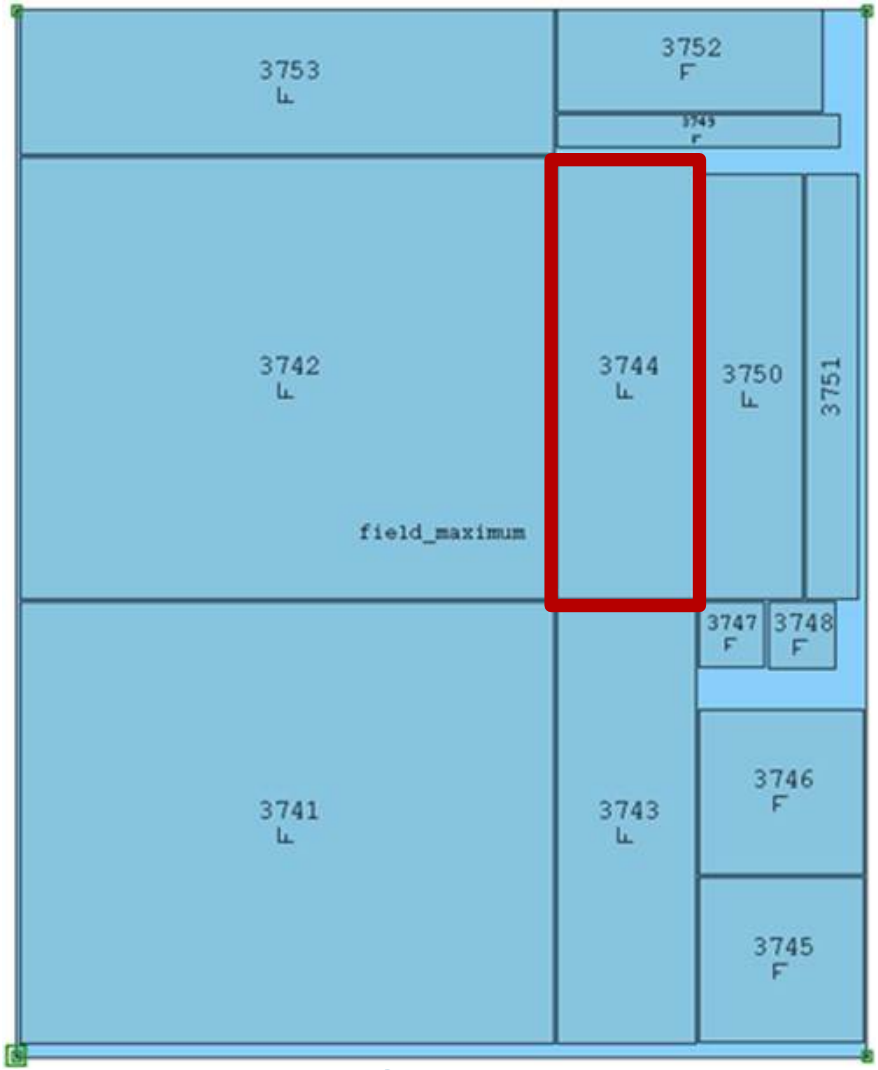

- BN3741/2: ARCADIA-MD1a/b
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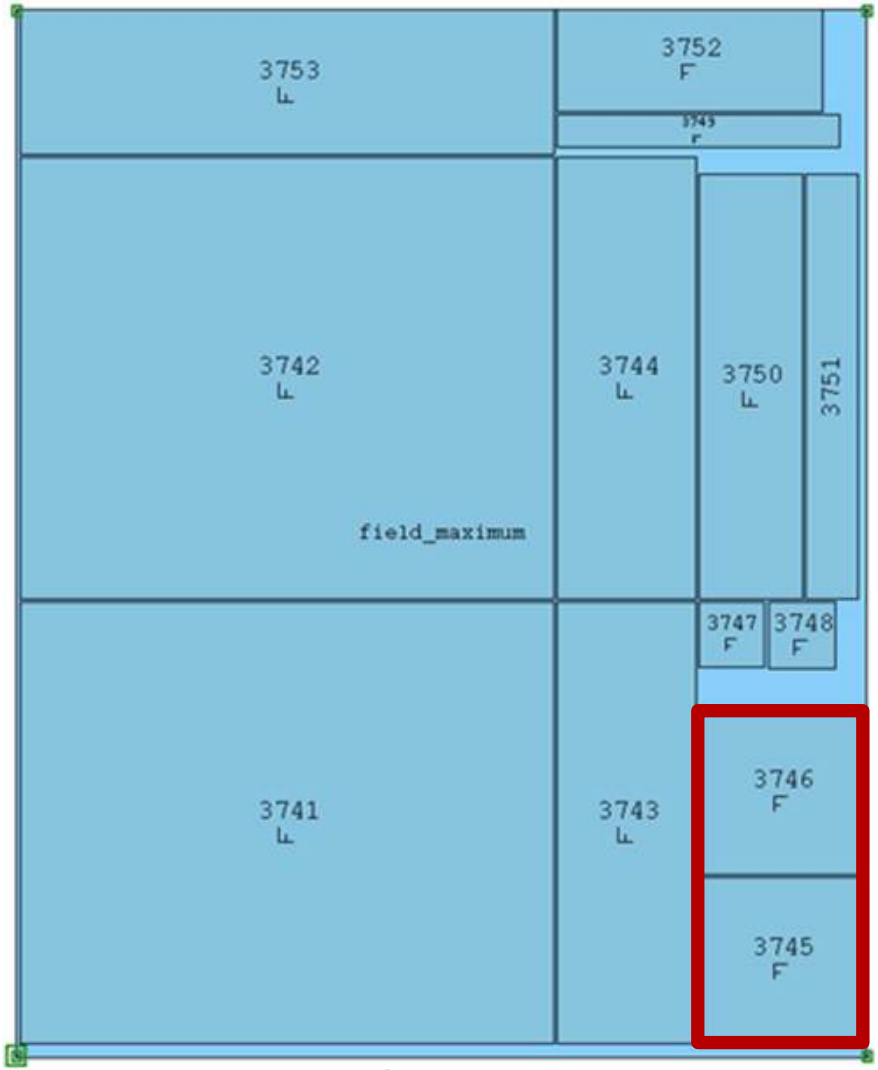

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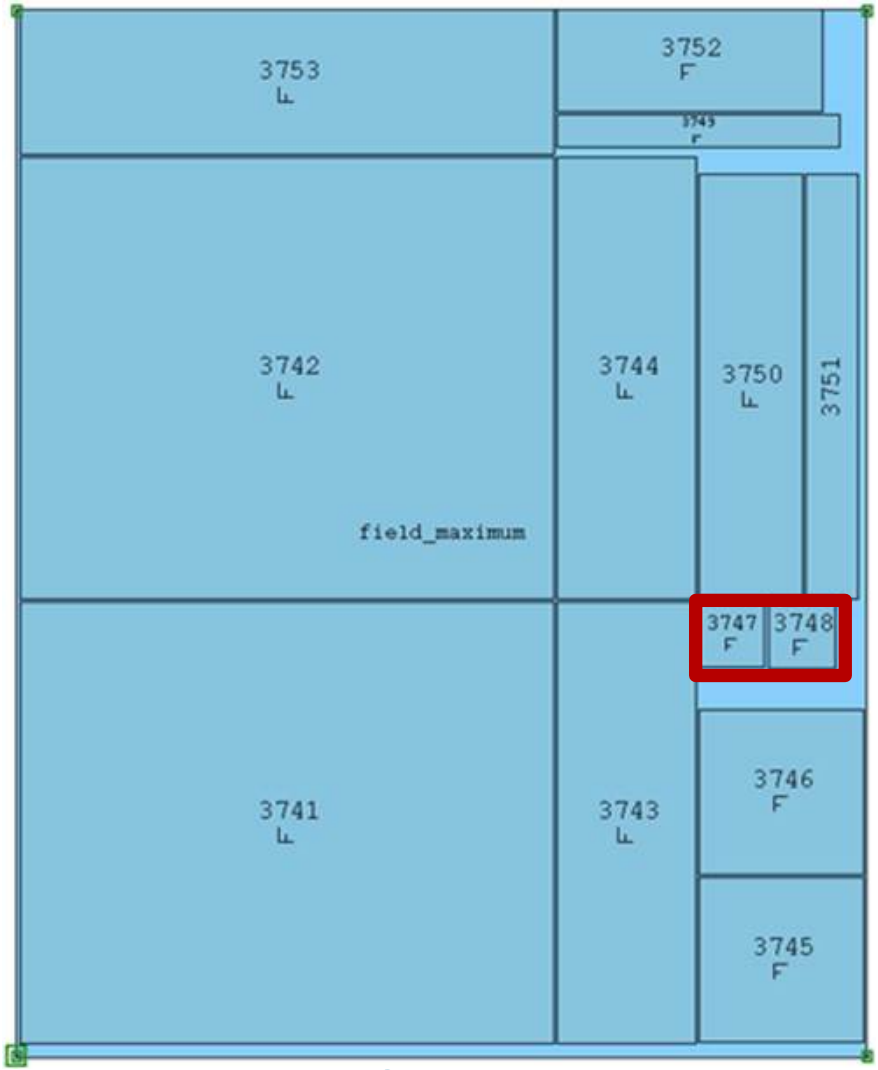

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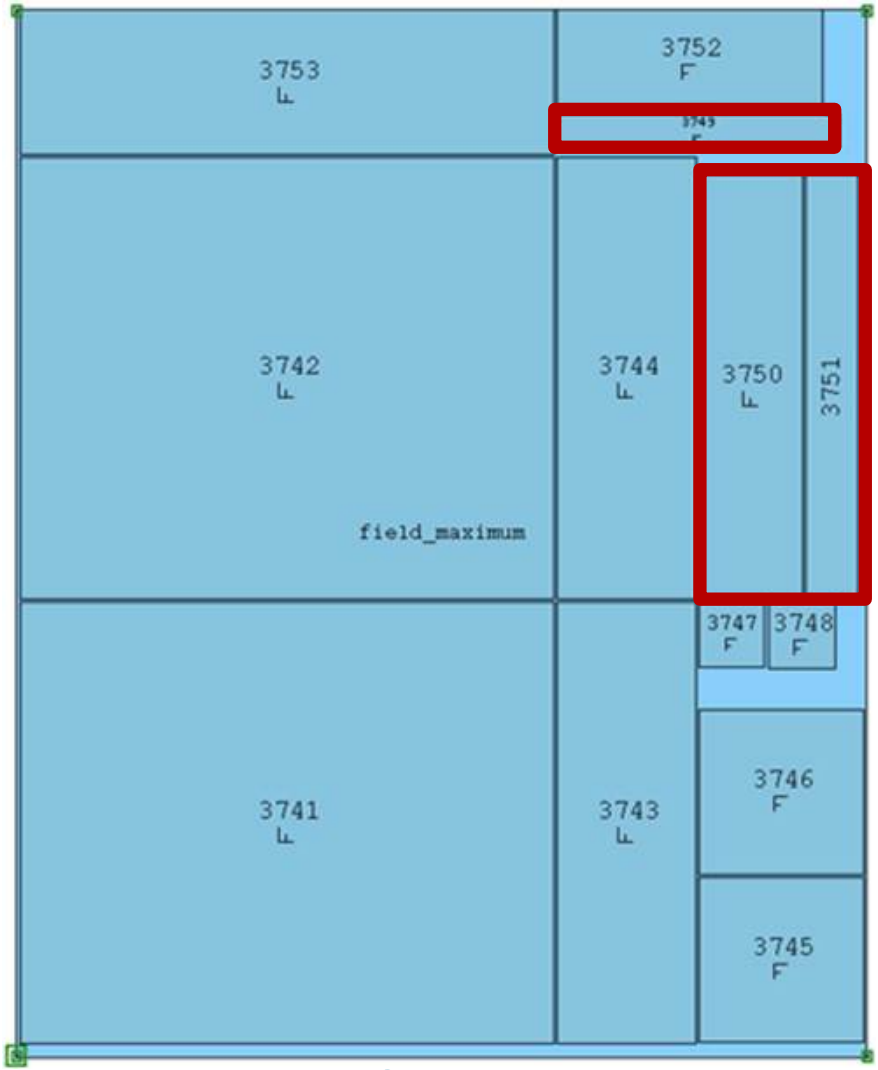

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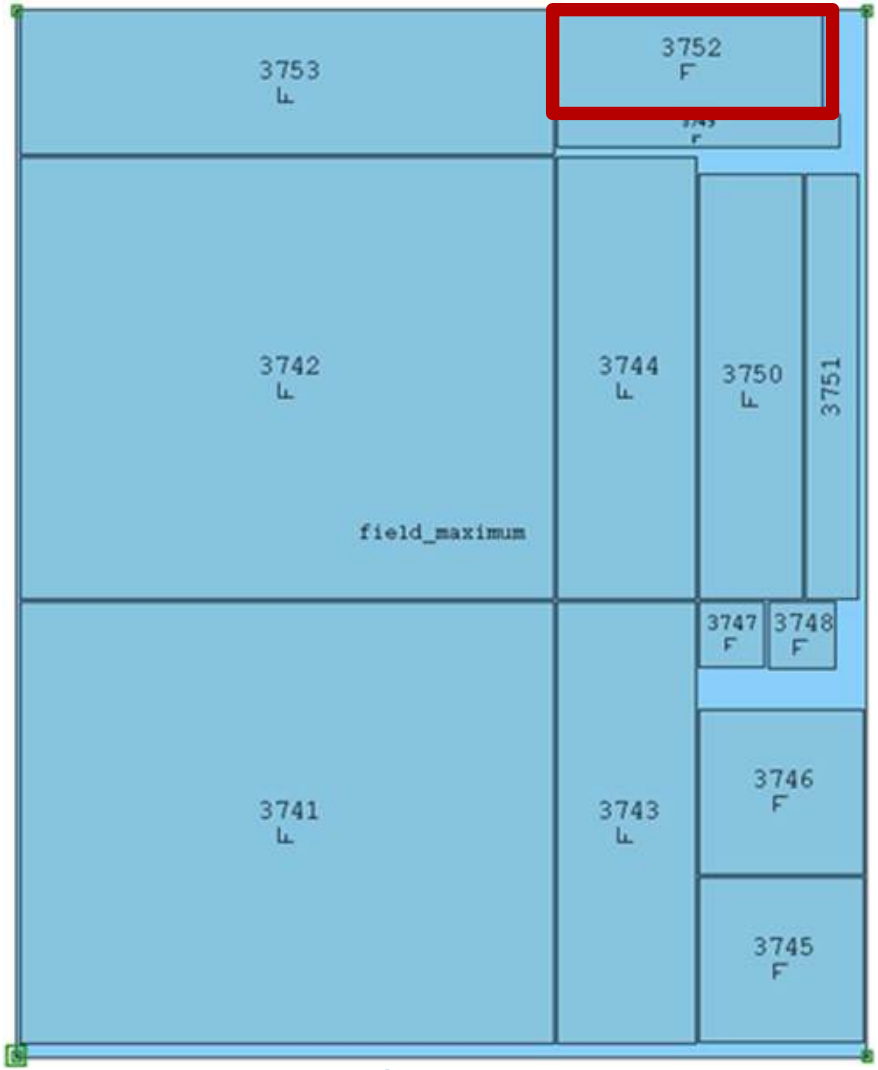

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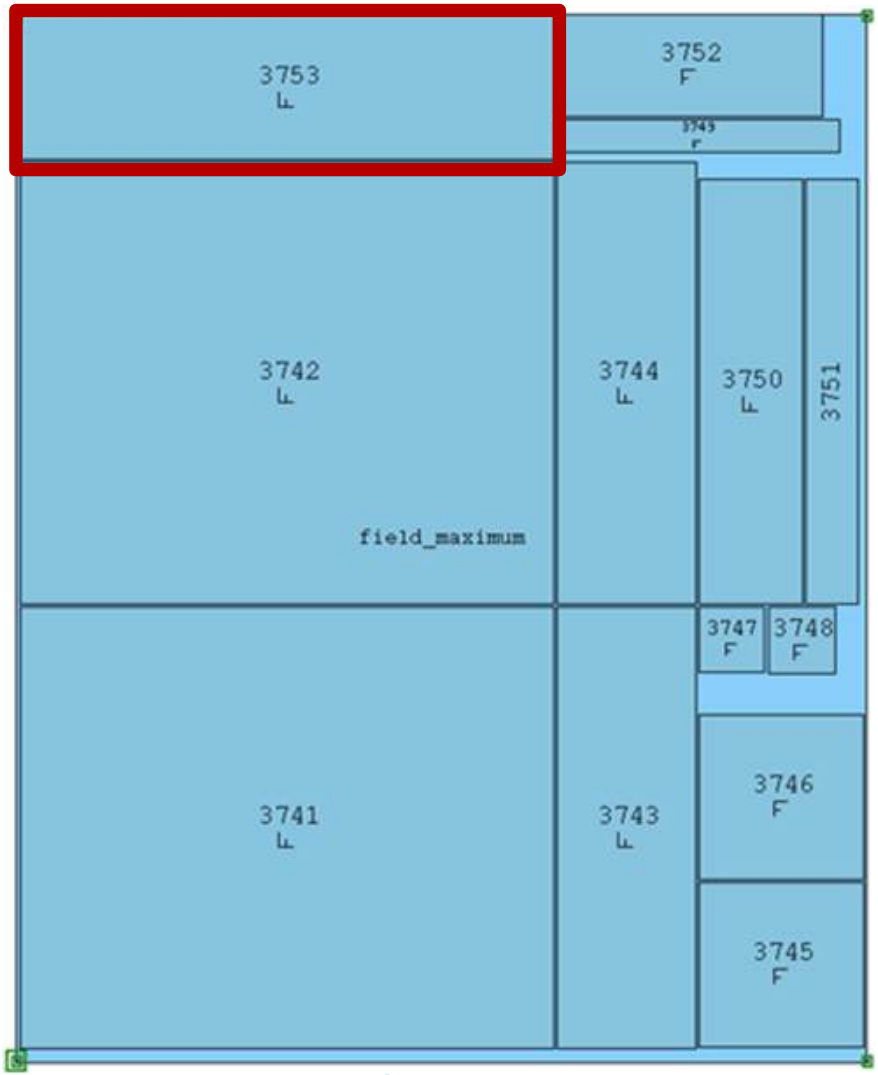

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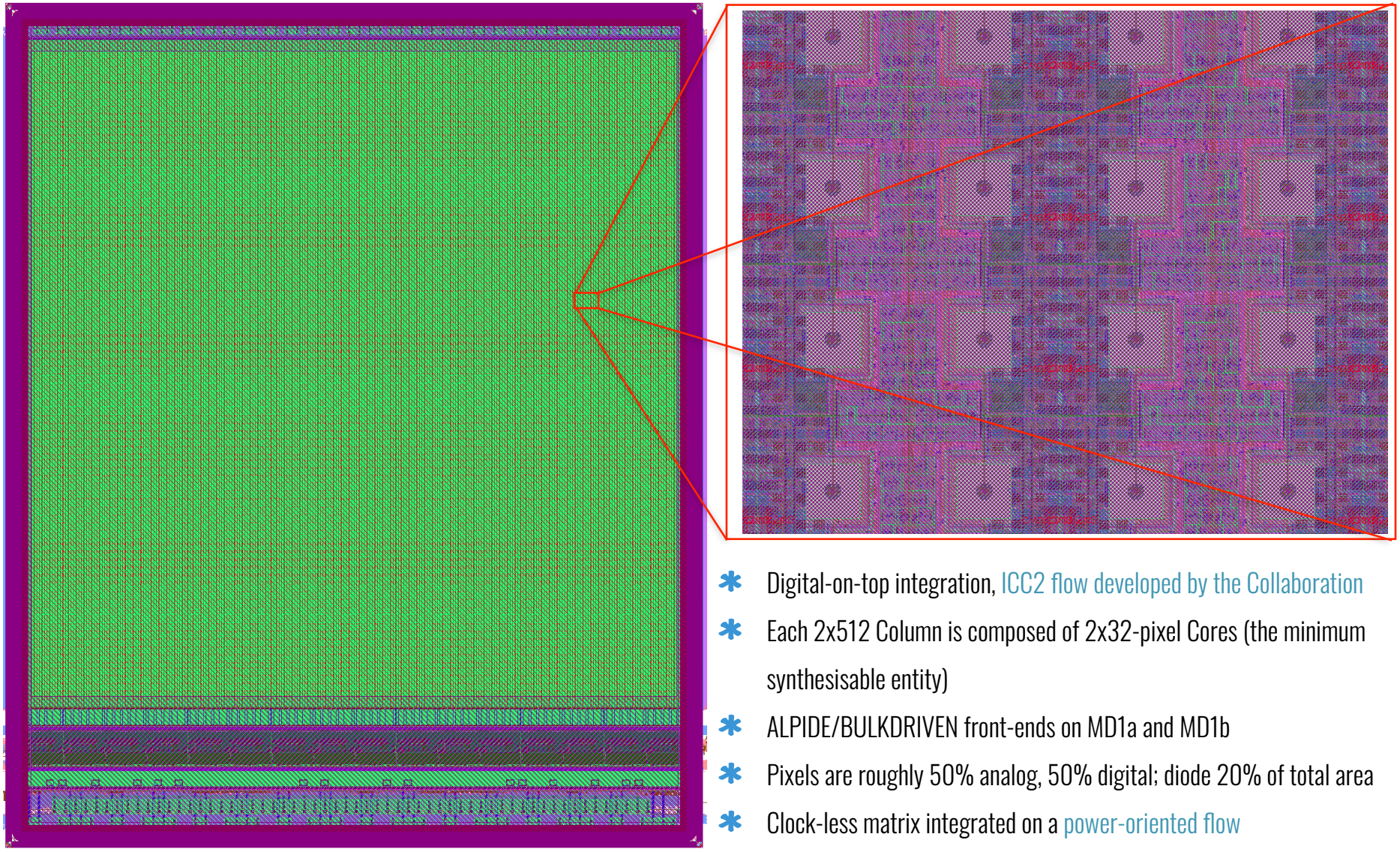
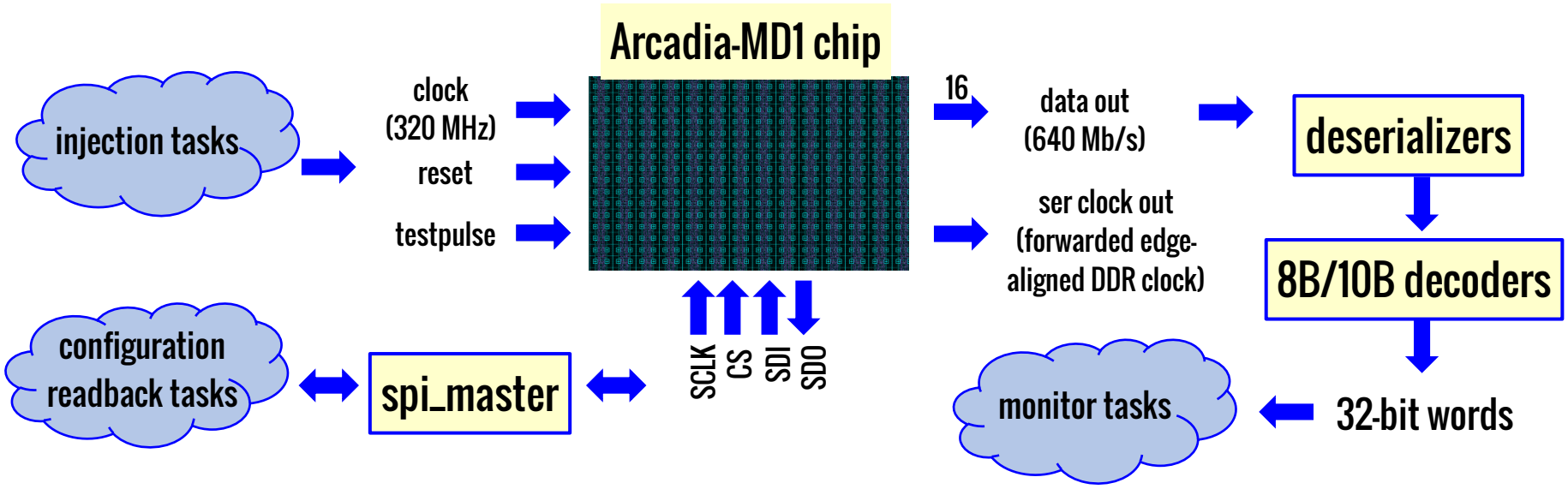
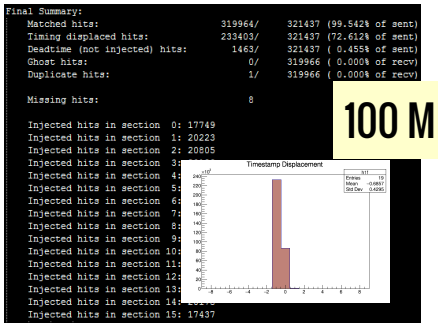
ARCADIA - Main Demonstrator Chip



- Digital-on-top integration, ICC2 flow developed by the Collaboration
- Each 2x512 Column is composed of 2x32-pixel Cores (the minimum synthesisable entity)
- ALPIDE/BULKDRIVEN front-ends on MD1a and MD1b
- Pixels are roughly 50% analog, 50% digital; diode 20% of total area
- Clock-less matrix integrated on a power-oriented flow

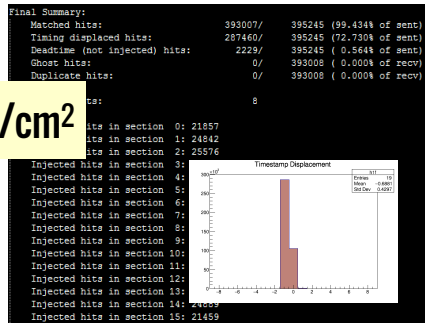
ARCADIA-MD1 Verification Framework



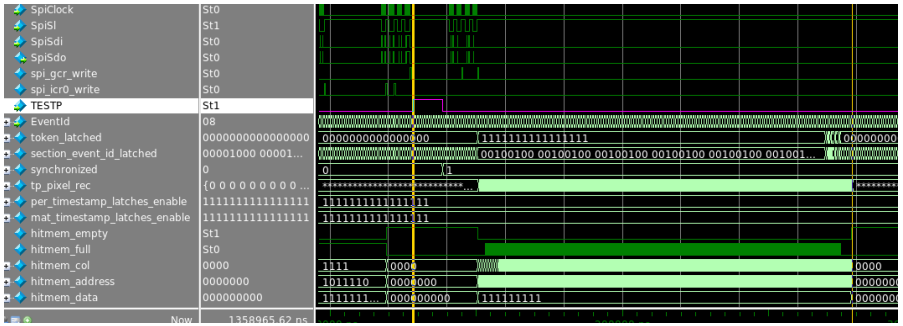


100 MHz/cm²

dEdx9.2_thetamax0_thickness100_posMED_100MHz_50mmColl_uniform



dEdx23_thetamax4_thickness100_posMED_100MHz_50mmColl_uniform

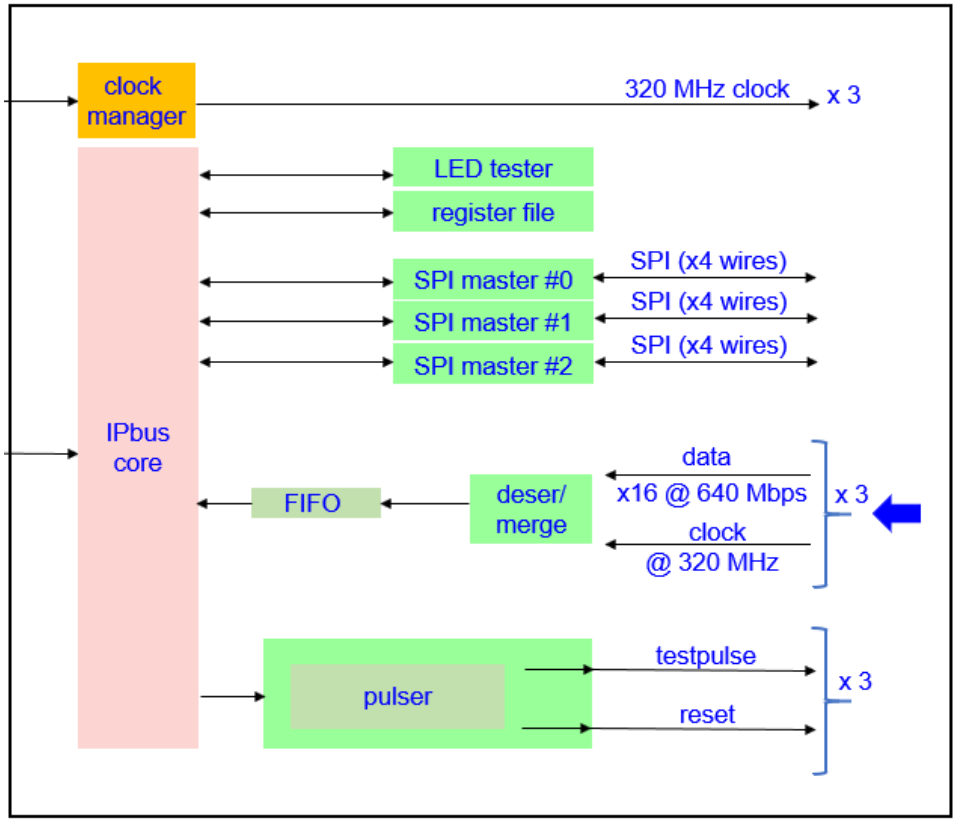


ARCADIA DAQ Firmware

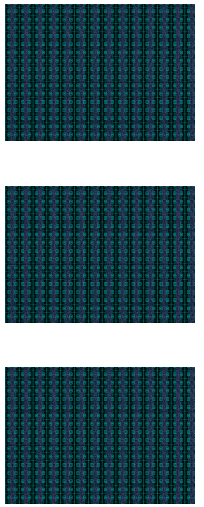
- The DAQ firmware blocks have also been inserted into the same simulation framework used for the ARCADIA-MD1 chip verification;
- We currently have a **universal simulation framework** in which the **ARCADIA-MD1 chip is configured and readout** via IPbus atomic operations **through the DAQ blocks**. This list of atomic operations is also being translated into the software running on the PC, which is being designed.

IPbus tasks:

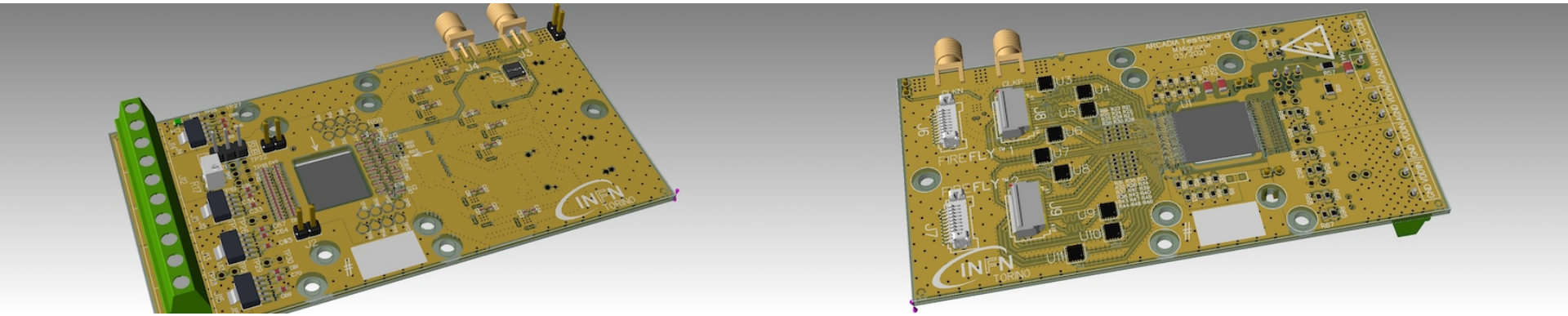
IPbus write
IPbus read
IPbus read_block



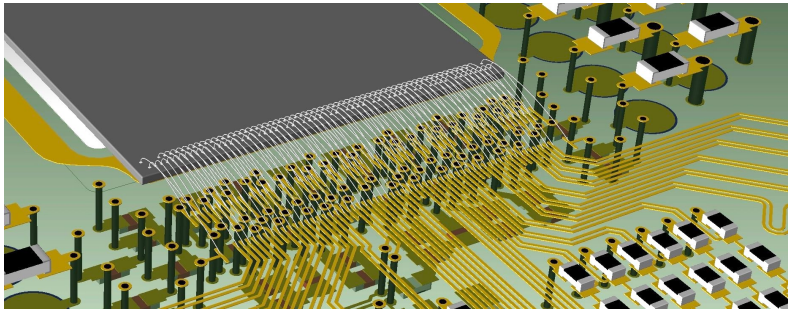
ARCADIA- MD1
(3 chips)



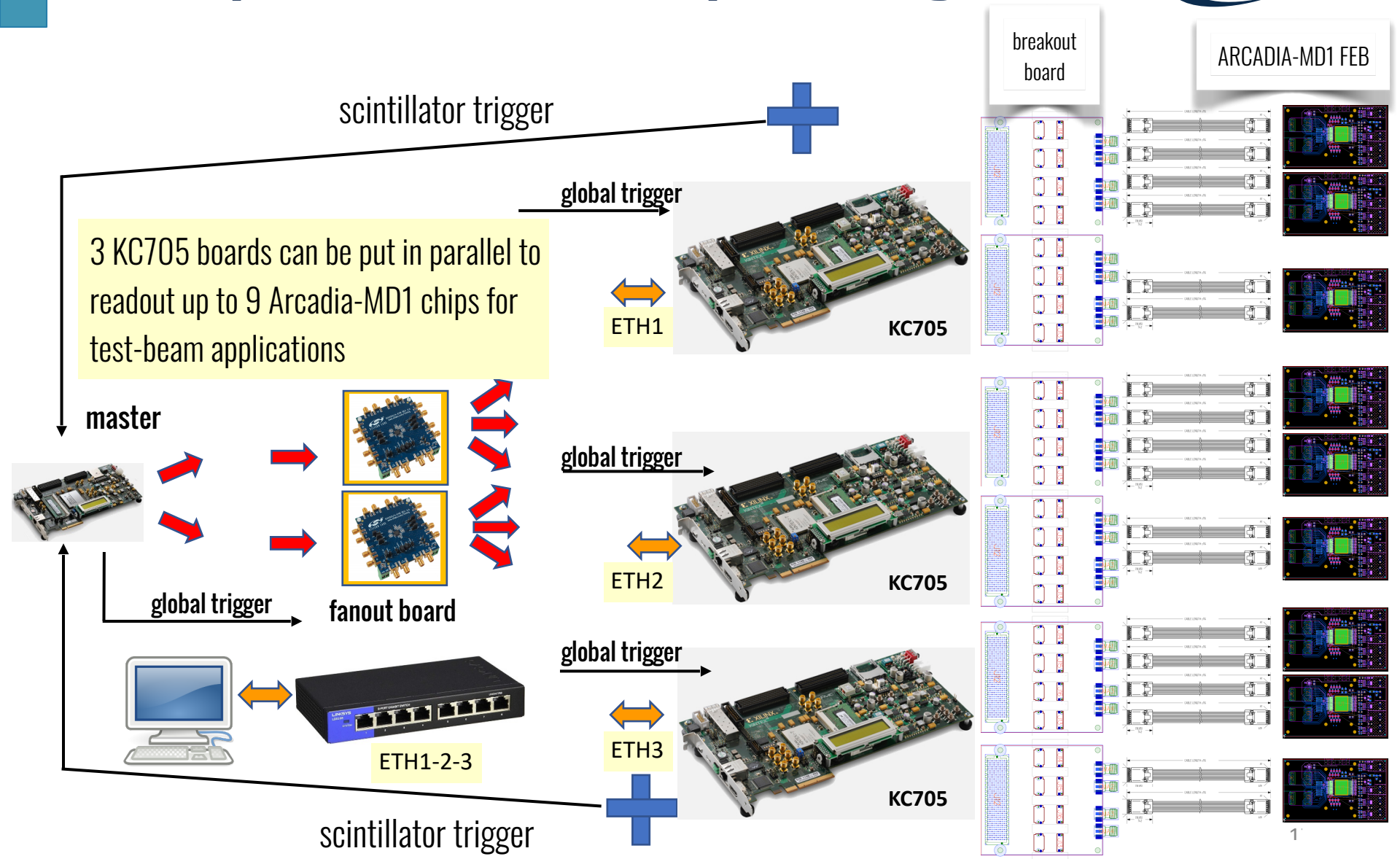
ARCADIA-MD1/miniD Front-End Board



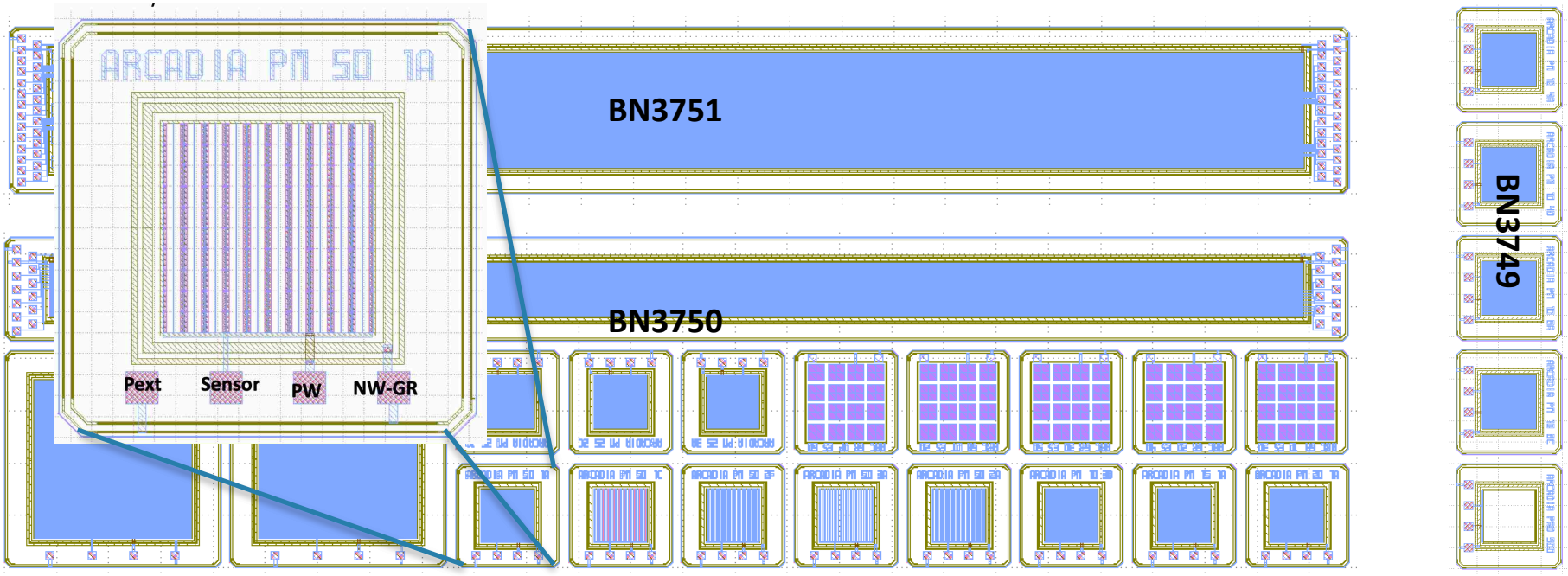
- 2 Samtec FireFly connectors for ASIC signals (Clock, SPI, Data)
- Possibility to use both an external low jitter Clock (via SMA connectors) or the clock provided by the FPGA
- Possibility to connect the high voltage on the DMAPS substrate or via the (wire bonded) pads on top
- Independent voltage regulators for the regional domains on-chip (IO Buffers, Analog Core, Digital Core)
- Extensive lab tests for the C-LVDS links
- PCB through-hole for matrix BSI
- production finished, in transit



Multi-plane MD1 Telescope Configuration



Pixel/Strip Test Structures



- **strips come in different flavours:**
  - 25 μm pitch pixelated + 25 μm continuous (10+10) [2 variants]
  - 10 μm pixelated (4 groups of 12 strips connected to pads) [4 variants]

- **and pixels as well:**
  - Pseudo-Matrices of 1x1 and 2x2 mm^2
  - 50 μm (5 variants)
  - 25 μm (3 variants)
  - 10 μm (6 variants)

Getting ready for silicon: priorities

- **Measurements on bonded test structures (first non-irradiated and then irradiated with x-rays and neutrons), front-side and back side**
  - IV curves with temperature, extraction of depletion, punch-through voltages, dark current and capacitance
  - Charge collection with focused pulsed laser (back-side). On pixels: only signal evolution with time and position of the laser spot. On strips: charge sharing is also possible.
  - Lab. sources. (top-side and back-side)

- **Characterisation of the ARCADIA-MD1**
  - functional and electrical characterisation (basic functionalities with on-chip test pulse and hit injection, s-curves, threshold calibration, rate assessment)
  - laser scans with red and IR light (CCE vs bias voltage, uniformity, clustering and resolution)
  - tests with x-ray and radioactive sources (55Fe, 241Am, 90Sr)
  - cosmic ray stand (sync and event building, efficiency, resolution) and beam tests with MD1 telescopes

ARCADIA@AIDAinnova

Advanced European infrastructure for Detectors at Accelerators

INFN

AIDAinnova Kick-off meeting

13-16 April 2021
Zoom
Europe/Zurich timezone

Search...

- Overview
- Agenda
- Registration
- Participant List
- Videoconference Rooms
- Coffee breaks

Contact
AIDAinnova-admin@cer...

The **AIDAinnova** (Advancement and Innovation for Detectors at Accelerators) project begins **1 April 2021 and will run for 4 years**. The kick-off meeting marks the official start of collaboration, when the **45 beneficiaries** and numerous associate partners will connect together within the AIDAinnova framework. The Kick-off will consist of parallels meetings of Work Packages, plenary sessions, a Steering Committee and a Governing Board meeting.

All the Zoom links are in the "videoconference rooms" section.

Have a chat with the AIDAinnova members during the coffee breaks by using Wonder me at the following link: https://www.wonder.me/r?id=c17eb000-5900-4487-80f4-3ec4bfdf305a

For questions or further information on the AIDAinnova Kick-off meeting please contact the Local Organizing Committee.

13:00 - 14:00

MAPS: Introduction
Ian Grinstein

nm Monopix: Status and Plans
I. Barbero

nm RD50-MPW3 and beyond
Illa Figueras

nm MALTA: Status and Plans
Solans Sa

Stream 3: WP2 - Communication, Outreach and Knowledge Transfer
Aurelie Pezous, Ms Daniela Antonio

Coffee/Tea Break
Zoom 15:25 - 15:35

Task 8.3.2: Large area scintillator det...
Frank Simon

16:00

Task 8.4.1: Innovative SiPMs and fut...
Rok Pestotnik et al.

Task 8.4.2: Development of highly-gr...
Romualdo Santoro

Coffe
Zoom

TJ 18
Konst

LF 11
Manuel Dionisio D...

TJ 65 nm Developments and Plans
Jerome Baudot

Zoom 14:00 - 17:00

17:00 **Coffee break**

LF 110 nm ARCADIA: Status and Plans
16:05 - 16:30
(Zoom)
Presenter Manuel Dionisio Da Rocha Rolo

- EC contribution **10.0 M€**
- Activities:
  - Joint Research & Networks

ARCADIA at AIDAinnova
WP5 - Depleted Monolithic Active Pixel Sensors

Development of next generation monolithic CMOS devices.

- Develop a demonstrator system that can be used in future experiments and upgrades
- Improvements in many directions: timing, thickness, speed, power, area, bendability,..
- Arcadia++ more focused on future colliders: ALICE LS3, Higgs factories (FCC, CEPC)
- Project start April 2021, 4 Years.

Expression of Interest for participating in the H2020 Innovation Pilot on detector technologies at accelerators

Title: **ARCADIA++** : Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Participants (max. 6): *list the participating institutes, laboratories and industrial partners*

Name of the legal entity	Type (university, institute, laboratory, company)	Country
INFN – BO, MI, PD, PV, PG, TIFPA, TO	Institute	Italy
Univ. Oxford	University	England
PSI	Institute	Switzerland
ETH	Institute	Switzerland
Univ. Zurich	University	Switzerland
IHEP	Institute	China

Contacts: *One name + e-mail per participant*

Participating institute/company	Main contact person	E-mail
INFN	Manuel Da Rocha Rolo	darochar@to.infn.it
Univ. Oxford	Daniela Bortoletto	daniela.bortoletto@physics.ox.ac.uk
PSI	Hans-Christian Kästli	hans-christian.kaestli@psi.ch
ETH	Malte Backhaus	backhaus@cern.ch
Univ. Zurich	Florencia Canelli	canelli@physik.uzh.ch
IHEP	Joao G Da Costa	guimaraes@ihep.ac.cn

ARCADIA@CEPC

Detector R&D Project Identification and Tasks Arrangement

The **Circular Electron Positron Collider (CEPC)** is a large international scientific facility proposed by the Chinese particle physics community.

- The **ARCADIA/LFoundry technology** is one of the two (the first being directly supported by MOST) proposals for the Vertex detector.

1. Vertex
   - 1.1. Pixel Vertex Prototype
   - 1.2. ARCADIA/LFoundry CMOS

CEPC Detector R&D Project

1.2 ARCADIA CMOS MAPS

Document Responsible:	Manuel Rolo
Last saved by on	11/01/2021 5:00:00 PM
Revision number:	2

CEPC Physics and Detector Plenary Meeting

Wednesday, January 6, 2021 from **15:00** to **17:00** (Asia/Shanghai)
at **IHEP Multi-subject Building (228)**

Description Zoom Connection:
https://weidijia.zoom.com.cn/j/69326273597?pwd=T0hCTW9zWlFZbDd3Nng4bzl1THIwQT09

ID: 693 2627 3597
pwd: 378821

The former version of the R&D documents were last discussed in detail at a meeting on April 29, 2020 which agenda is linked below. Those late Word files can be found in the "Document" tab below. Updates should be posted into today's indico agenda.

Material: Minutes | agenda | document

Wednesday, January 6, 2021

15:00 - 15:20 Short introduction *20'*
Speaker: Joao Guimaraes Costa

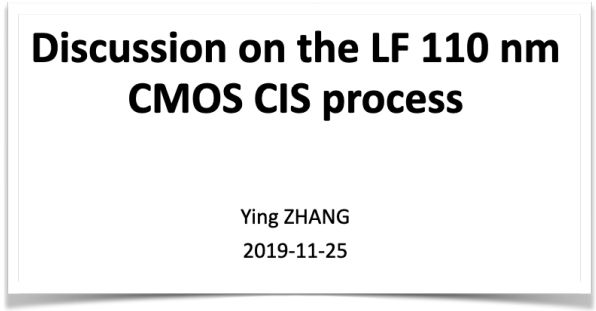
15:20 - 16:20 Discussion of Detector Project R&D Tasks *1h0'*
Speakers: Roberto Ferrari (INFN), Paolo Giacomelli (INFN-Bo), Francesco Grancagnolo (INFN-Lecce), Suen Hou (IPAS), LI Gang (EPC.IHEP), Prof. Zhen An LIU Zhenan (IHEP), Dr. Weidong Li (高能所), Prof. Zhijun Liang (IHEP), Dr. Jianbei Liu (University of Science and Technology of China), Dr. Yong Liu (Institute of High Energy Physics), Prof. Qun OUYANG (IHEP), Dr. Huirong Qi (Institute of High Energy Physics, CAS), RUAN Manqi, Prof. Meng Wang (Shandong University), Haijun Yang (Shanghai Jiao Tong University), Dr. Hongbo ZHU (IHEP), Mr. Zian ZHU Zian (高能所), Prof. Liang Li (Shanghai Jiao Tong University), Manuel Dionisio Da Rocha Rolo (INFN Torino), Dr. Xiaolong Wang (Institute of Modern Physics, Fudan University), Dr. Sheng-Sen Sun (Institute of High Energy Physics)

1.1 Vertex *15'*
Speakers: Prof. LIANG Zhijun, Prof. Qun OUYANG (IHEP), Joao Guimaraes Costa

1.2 ARCADIA CMOS MAPS *15'*
Speaker: Manuel Dionisio Da Rocha Rolo (INFN Torino)
Material: Slides

Platform for sensor design and fabrication

- Discussion on the use of SEED/ARCADIA for the R&D towards CEPC started in 2019.



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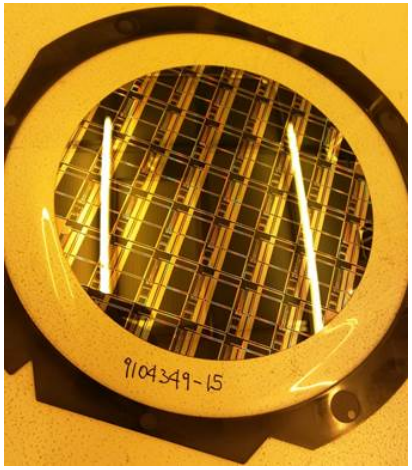
Institute of High Energy Physics Chinese Academy of Sciences

- **The access to LFoundry Process Design Kit (PDK) and Synopsys PyCells for CMOS LF11is is active at IHEP since January 2020.**
  - ☑ INFN and IHEP can share CMOS design databases and program shared tapeouts to foundry
- **Discussion started on design and fabrication flow towards a Joint IHEP-INFN MAPS:**
  - INFN provides IHEP with a signal sample database and a simplified sensor geometry
  - IHEP designs (in-house or in cooperation with INFN) a CMOS MAPS using LFoundry LF11is
  - INFN cares the final DRC on IHEP's gds2, validation of the design and production

ARCADIA: status and plans in a nutshell

- ARCADIA has now secured a total budget of 1.4 M€ with several groups working on:
  - Sensor R&D and Technology
  - CMOS IP Design and Chip Integration
  - Data Acquisition for electrical characterisation and beam tests with multi-chip telescopes
  - Radiation Hardness qualification
  - System-level characterisation for Medical (pCT), Future Leptonic Colliders and Space Instruments

- **Schedule for 2021-2022**
  - all hardware and firmware ready for testing, first silicon just delivered
  - 1st SPW run included 800 mm2 of innovative DMAPS, sensor and CMOS technology (first tests on sensors are ok, wafers currently being diced)
  - 2nd run mid-2021: in preparation, 3rd run planned for mid-2022;



Thank you for listening!