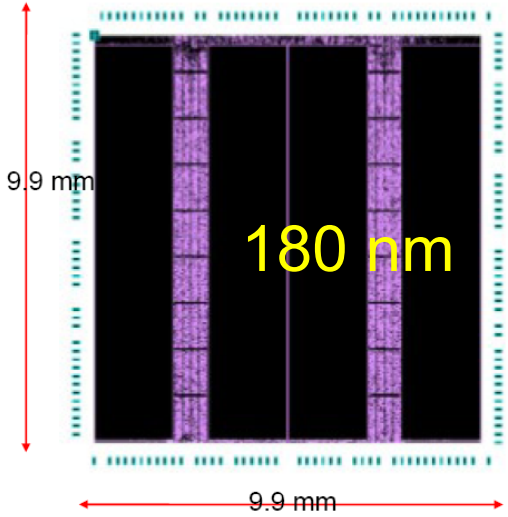
FTK Update

Paola for the FTK Italian collaboration

(Bologna-Frascati-Milano-Pavia-Pisa)

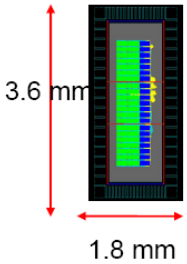
- Approved by **TDAQ** in april – next: approval by **ATLAS**
- Ongoing activity: **AMchip, AMboard, TSP, Simulation**
- Next future: mezzanine for **2-D clustering**, **Vertical Slice**, **Services**
- **July 7, 10 am room 250** – presentation to the electronic group

Amchip03



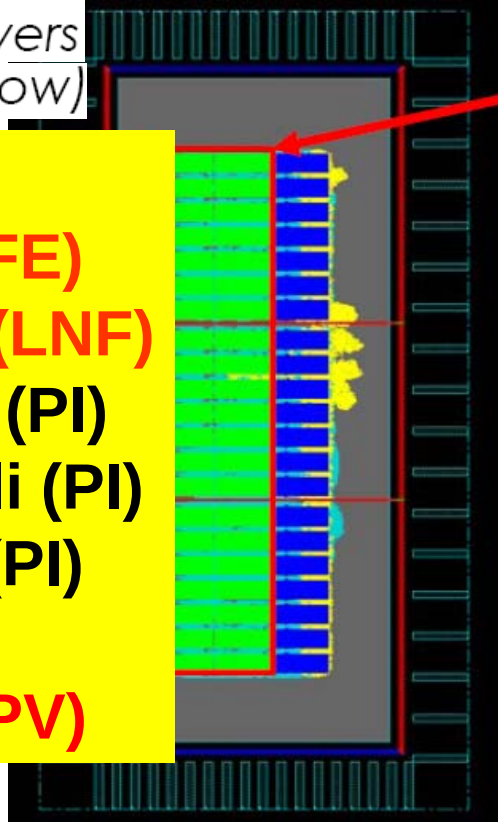
AmchiP04

90 nm



- 1 smaller pattern bank.
- Same logic (address decoding, JTAG interface..).
- External pinout compatibility with the amchip03 test setup (both software and hardware).
- Same majority logic (std cell)7
- ***New layer: Full Custom.***

8 full-custom layers per pattern(row)



TODAY

L.Sartori (FE)

M.Beretta (LNF)

E. Bossini (PI)

F. Crescioli (PI)

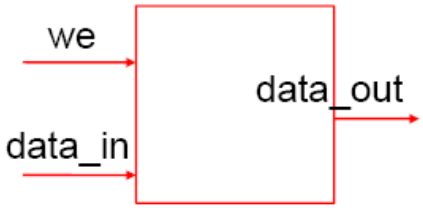
I. Sacco (PI)

TEST

A. Lanza (PV)

..Full-Custom vs standard-cell in 30 sec...

A memory cell (latch) in the standard cell tech:



It's a black box for the designer:

- timing and geometrical characterization are provided by the foundry;
- a library provides a set of standard digital cells (memory and logical cells);
- They are general purpose, no user optimization.

A memory cell in the full-custom tech:

Poly, Metals drawing "by hand".
Maximum level of optimization.

Each full-custom layer is a new standard cell:

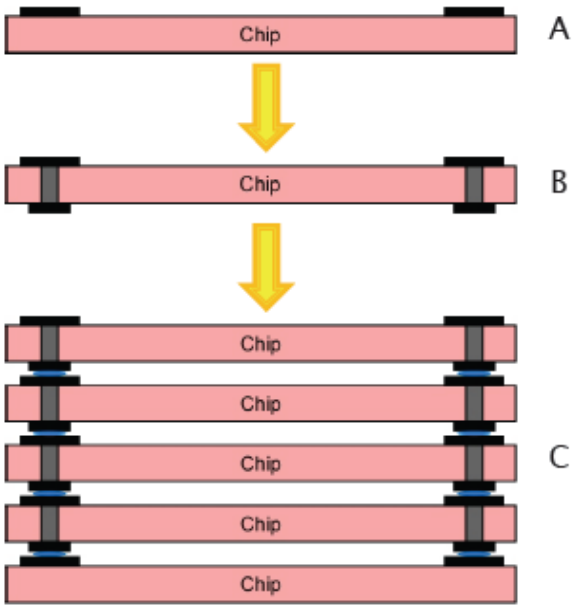
1) std cell constraints/rules;
2) model for behavioral simulation;
3) model for timing simulation.

The layer is composed by 15 Content Address Memory (CAM) cells.

All the rest is still in standard cell

Germany: collaborate on 65 nm or even 45 nm?

2.5D??? What is that?



jimhoff@fnal.gov (x2398)

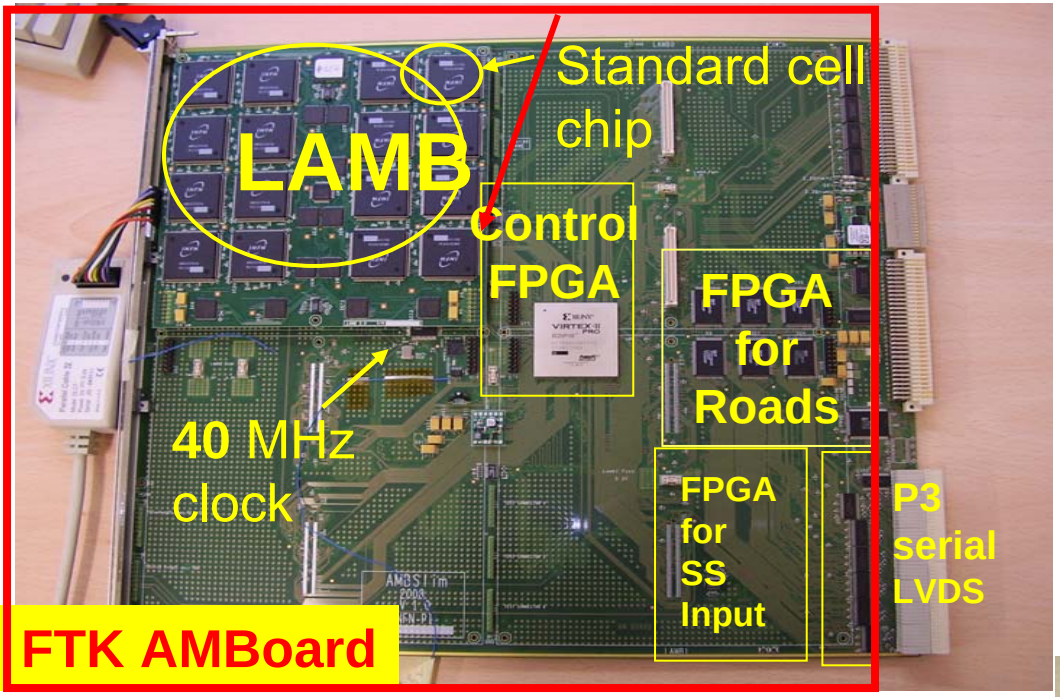
- Generally speaking, 3D is used to describe any "monolithic" design with multiple active tiers.
- Unfortunately, 3D also refers to the density of interconnect between tiers. "True 3D" or "full 3D" or sometimes simply "3D" refers to dense interconnects between tiers located throughout the tiers (not just in a few specific locations).
- So what is 2.5D? 2.5D is a stacking of multiple active tiers, so it is still "3D". However, the interconnect density is comparatively low, often just at the pads.
- To the right is shown a 2.5D stacking. We start at the top with a single chip (A). Through silicon vias are cut at or near the pads and back-side metal is placed on the chip (B). Multiple chips are placed in a stack by one of a variety of methods (bump bonding, DBI, etc.). The result is shown in (C).

- Less expensive.
- Simpler technology.
- (Possibly?) Greater reuse of existing technology because you are not specifically designing a new 3D chip (maybe).

FERMILAB - tomorrow

We are defining a collaboration Italy-USA for DOE application to Generic R&D funds (ATLAS FTK - Fermilab CMS, both interested)

AMboard: Pisa-Milano



Board Power consumption:

230 W @ 1,8 V today
@ 1V Phase 1
→ 128 A today
→ 230 A Phase 1

cooling

Fast and dense connectors

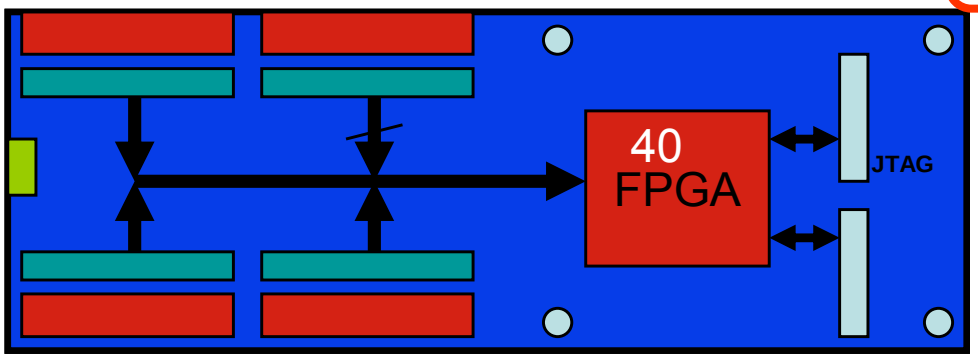
Thin powerful - FPGAs

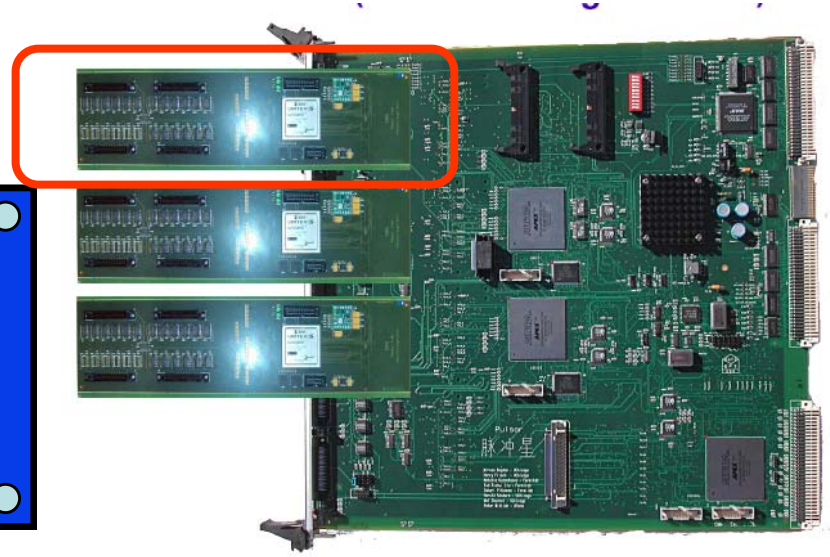
16 AMBoards per “core” crate
→ 8 core crates in the system
Discussion with CERN started on **POWER** and **COOLING**

Whatever is the power of the AM we can build, we can do better complementing the AM with a TSP

Milano: starting from an existing mezzanine will build a TSP Prototype to test its performances and extrapolate its costs

Clone the GF Mezzanina.
Use it on Pulsar





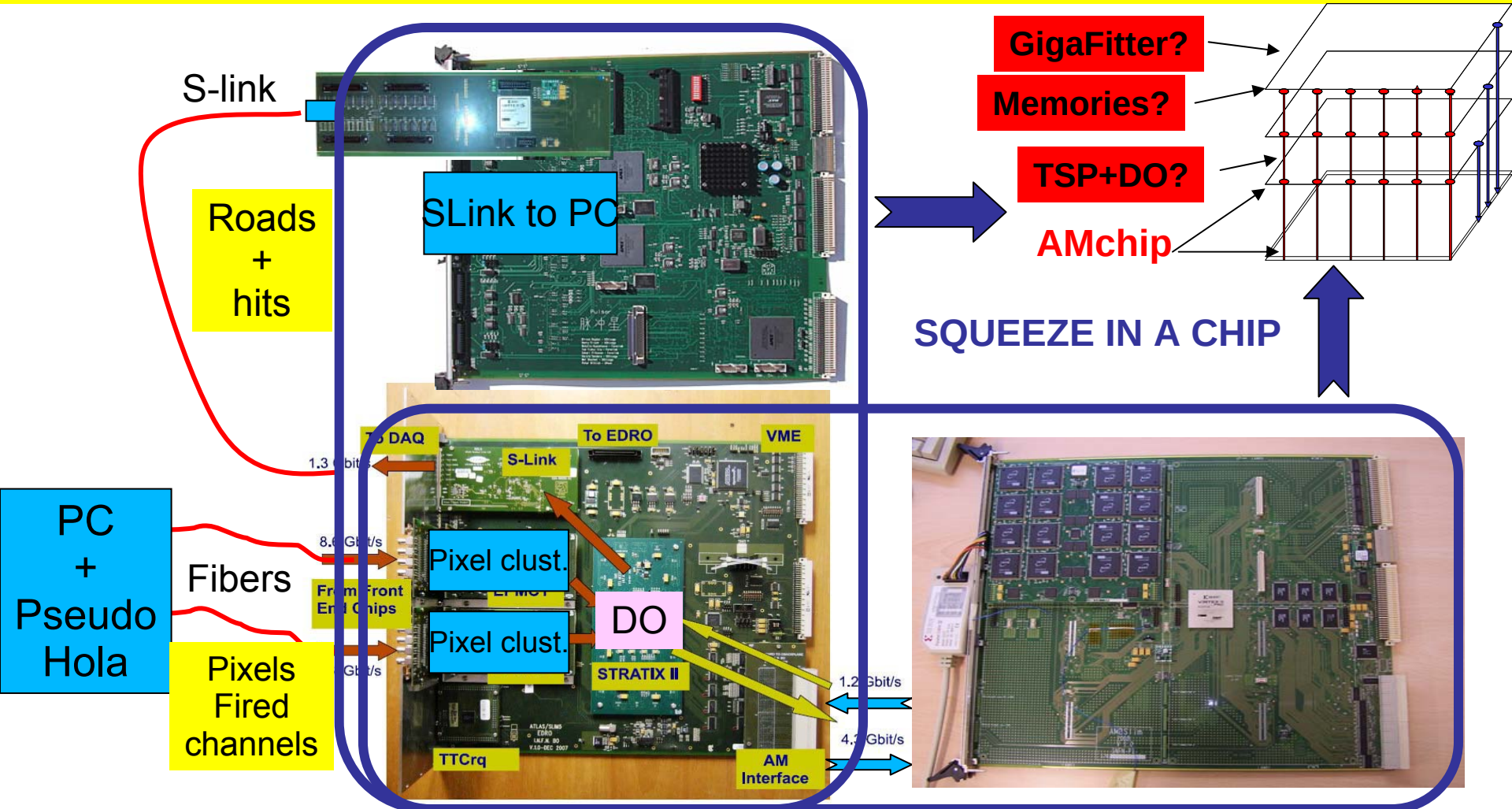
SERVICES FOR 2012: Holas on the detector

Chicago – Pavia - Frascati

Tests: the Vertical Slice starting next June:

Bologna (EDRO)-Pisa (AMBoard)

when ready Frascati (pixel clustering) – Milano (TSP) - Pavia (AMboard and software)



Simulation activity Pisa-Frascati a lot of space for new people

- Efficiency-tracking improvements and studies
- Efforts to reduce the # of matched roads, optimize banks
- Algorithm Improvements Studies
- Comparison of 11L, Option B and Option A - Select baseline design
- Description and study of the evolution of the system from 10^{33} up to 5×10^{34} and above.
- Trigger strategy developments
- Integrate FTKSim into ATHENA
- Compare simulation with real data

The following is a technically limited schedule:

SHOWN @GR1 March 30 2010

Vertical slice and software	beginning in late 2010, continuing into 2012
Design & prototype of each board	June, 2012
Exception: New AM chip and AM board with full TSP implementation come after completion of R&D and study of ATLAS collision data.	
Install dual-output HOLAs	2012 shutdown
Install system needed for 3×10^{33}	late 2012 – early 2013
Expand system for 1×10^{34}	late 2014 – early 2015
Full system for 3×10^{34}	decided after AM chip R&D and study of real data

Global Costs based on TP (6-10 y):

~1150 K€ Italy
~1150 K€ USA
~200 K€ Waseda
~300+ extra K€ new institutions

Assuming we can have material from CDF

Costs for 2013 run

~400 K€ Italy
~500 K€ USA
~200 K€ Waseda
~0 new institutions

Breakdown of 410 k€ for 2013 (using CDF crates & Lambs)

2011: R&D + prototypes + Services (Hola2, fibers....)

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TSP R&D	20 k€	http://www.pi.infn.it/~paola/FTK/ForReferees.xls
AM prototype	30 k€	
Services	60 k€	

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TOT 2011 110 k€ + (50 k€ for LAMBs S.J. CDF run 2013)

2012: production for barrel

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AMchip prototype	40 k€
AMBoards	40 k€
DF pixel mezzanines	100 k€

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TOT 2012 180 k€

We will need also 5 crates (9U VME)
Not included into these costs
Trying to find them inside CDF

2013: production for forward/backward

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DF pixel mezzanines	90 k€
AMboard	30 k€

+ extra depending on schedule

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TOT 120 k€ + ?

Breakdown 2011 between collaborators

TSP R&D	20 k€	MILANO
AM test for P3 connect.	5 k€	MILANO
AM prototype	15 k€	PISA
Vertical Slice	10 k€	BOLOGNA
Services	30 k€	PAVIA
(Hola2, fibers..)	30 k€	FRASCATI
LAMBs	50 k€	PISA S.J. only if CDF will run in 2013.

TOTAL 110 k€
\+ 50 k€ S.J.

Summary

Bologna	10 keuro
Frascati	30 keuro
Milano	25 keuro
Pavia	30 keuro
Pisa	15 keuro + 50 s.j.

Trasferte

- Responsabilita':
  - P. Giannetti coordinatore italiano L2
  - G. Volpi Responsabile del software di FTK L3
  - Dovremmo definire le altre responsabilita' in futuro

- Attivita' specifiche:
  - Vertical slice a Bologna: 2-3 k€ a sezione? (Fr, Mi, Pv, Pi) controllare con la propria sezione la criticita' di trasferte in Italia.
  - Vertical slice al CERN: 2 persone x 2 mesi.

People

Percentuali in FTK

Milano

- V. Liberali 50%, M. Riva 30%, M. Citterio 20%, C. Meroni 10%, A. Andreazza 10%, servizio elettronica 12 mesi con A. Andreani e F. Sabatini

Pisa

- P.Giannetti 60%, M.Dell'Orso 50%, F. Crescioli 70%, M. Piendibene 60%, C. Roda 20%, R.A. Vitillo 20%

Pavia

- A. Lanza 40%, A. Negri 20%, V. Vercesi 30% + servizio elettronica

Frascati

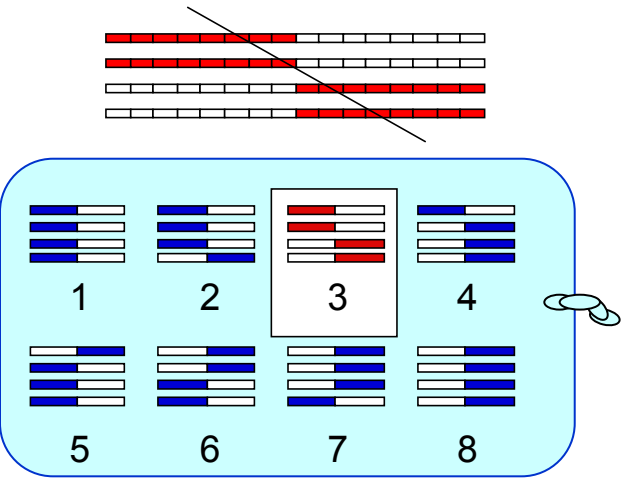
- A. Annovi 50%, G. Volpi: 70%, M. Beretta xxx%

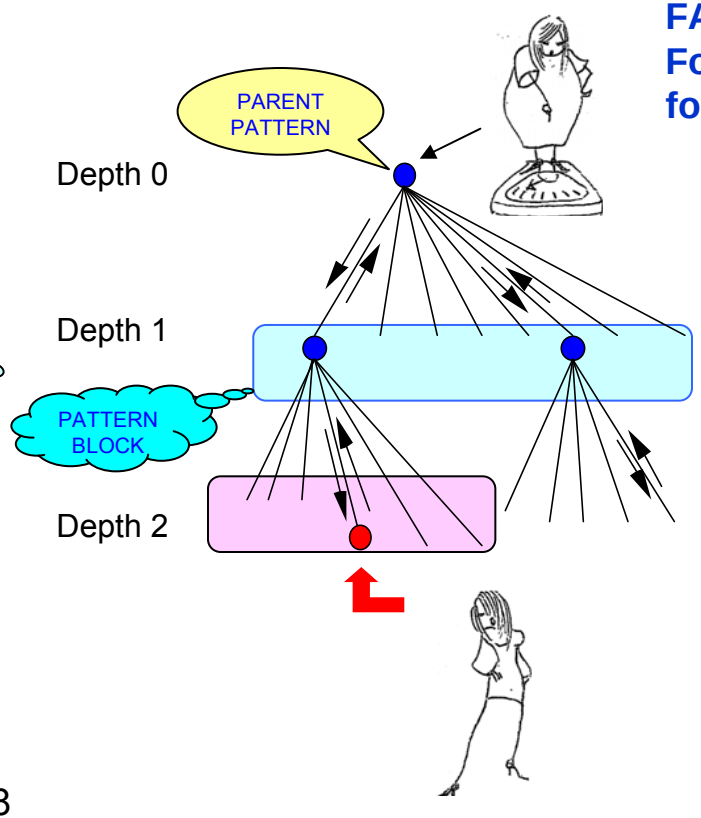
Bologna

- M. Villa xxx%, F. Giorgi xxx%

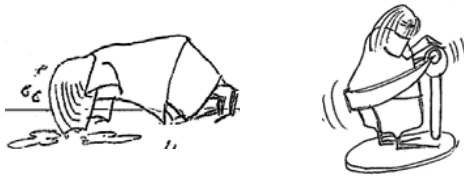
BACKUP

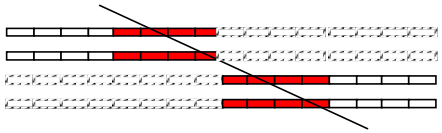
The Tree Search Processor (TSP): Binary search to go down to better SS resolutions



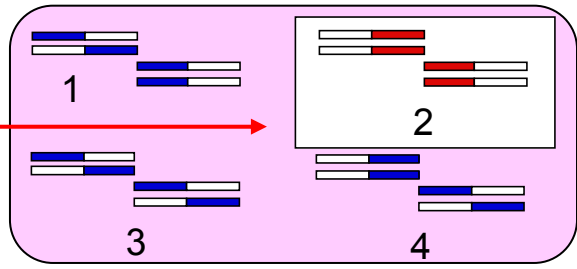


FAT ROAD
Found by AM (default SS for example)





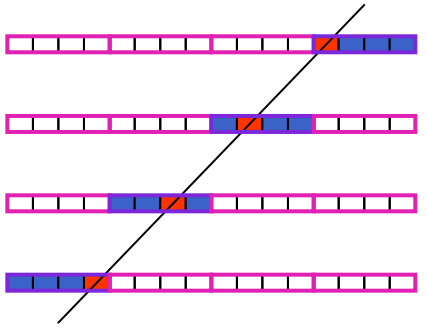
THIN ROAD



Algorithm: NIM A287 (1990) 436-438
http://www.pi.infn.it/~paola/Tree_search_algorithm.pdf
Tree Search Processor: NIM A **287**, 431 (1990),
http://www.pi.infn.it/~orso/ftk/NIMA287_431.pdf
IEEE Toronto, Canada, November 8-14 1998
http://www.pi.infn.it/~paola/TSP_v14.pdf

Higher resolution SS (sub-ss) to be stored in AM or into a Mini-DO & LSB bits should be provided to TSP

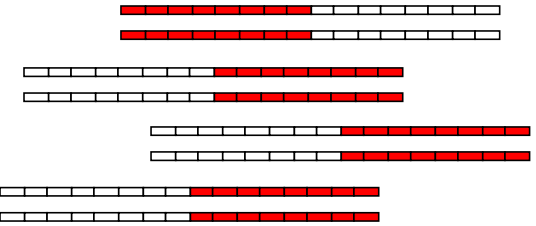
Example: 2-Level TSP → divide by 4 each SS



The **AM chip** for each found road could provide:

1) The Road IDentifier (address)
2) The Bitmap : one bit per layer, saying which SSs are empty & which are full (11 bits: 11101111111 eg.)
3) 4 more bits for each layer, Sub-SS, saying which of the 4 SS subdivisions are empty and which are full (4 bits × 8 Layers).

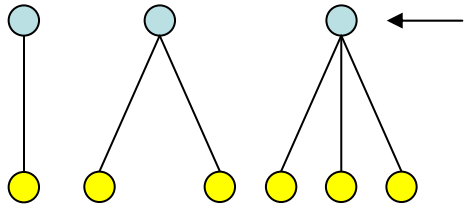
A new idea that could have a large impact: variable precision patterns



# of Kids (combinations of high resolution SS)

$258 = 2^8$

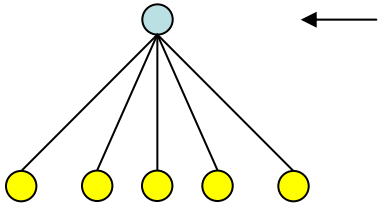
if only **1, 2 or 3** over possible 256 kids **are good track** → It is convenient to insert high resolution patterns into the AM



Parent pattern with 1 or 2 or 3 kids

(1) # of patterns do not increase very much

(2) Probability to fire as fake road is smaller



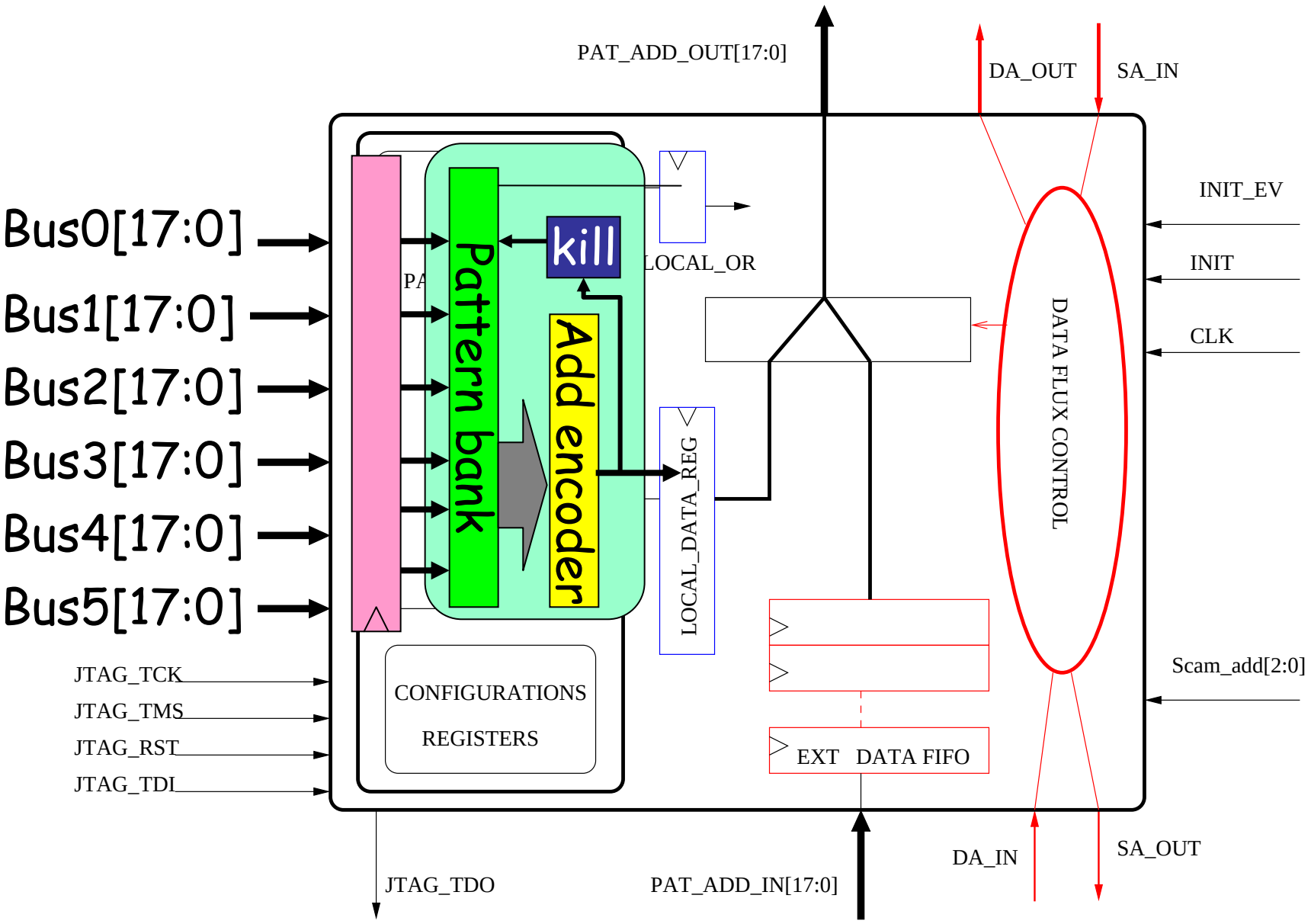
Parent pattern with more kids

(1) # of patterns do increase if we go deeper

(2) Probability to fire as fake is ~ the same

SS will have enough bits to do the matching of all patterns at high resolution, but the less significant bits can be set as DON'T CARE and not participate to the matching (the kids are not loaded into AM if the DON'T CARE is set).

The CDF final AMchip architecture

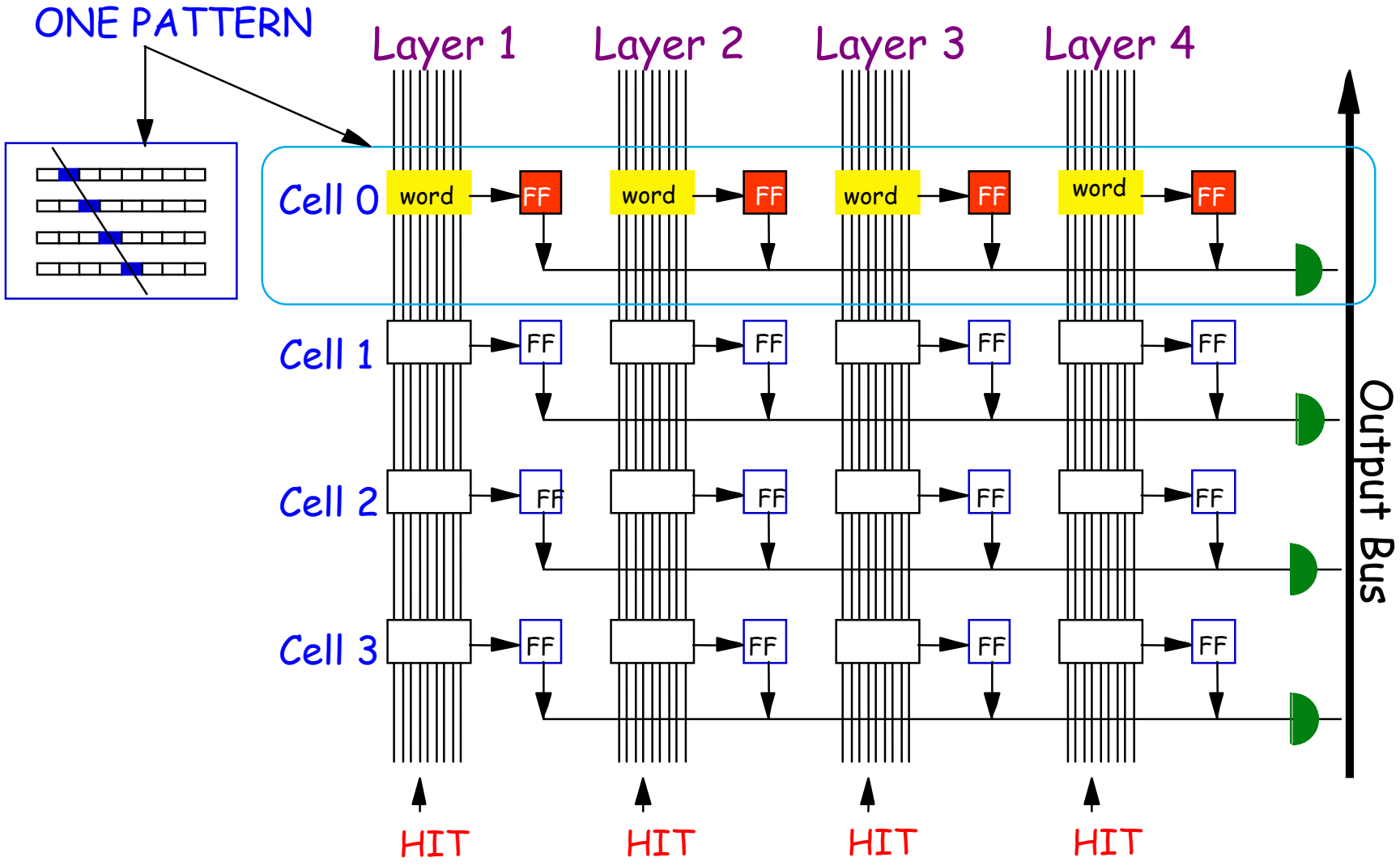


Power consumption

Old Chip:	corr. Factor	1,8 Watt
180 nm 1,8 V Core		
New chip 90 nm 1 V Core	1/(1,8*1,8)	0,56 Watt
Frequency 40 MHz		
New chip 100 MHz	100/40	1,39 Watt
Area 1x1 cm**2		
New chip 4 cm**2	4/1	5,56 Watt
New: Pre-match feature	1/3 (1/2)	1,85 (2,78) Watt
Per crate 16 x 128 = 2048 chips		3,8 (5,7) kW

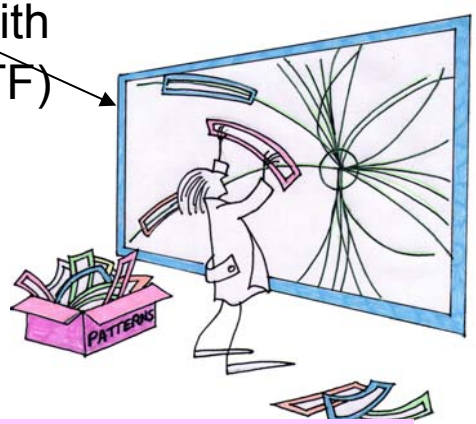
IF the pre-match feature save at least 1/3,
new 2D chip (1,85 W) ~ old chip (1,8 W)
ANY OTHER IDEA TO GAIN IN POWER INCREASES
THE POTENTIALITY TO GROW IN THE THIRD DIRECTION

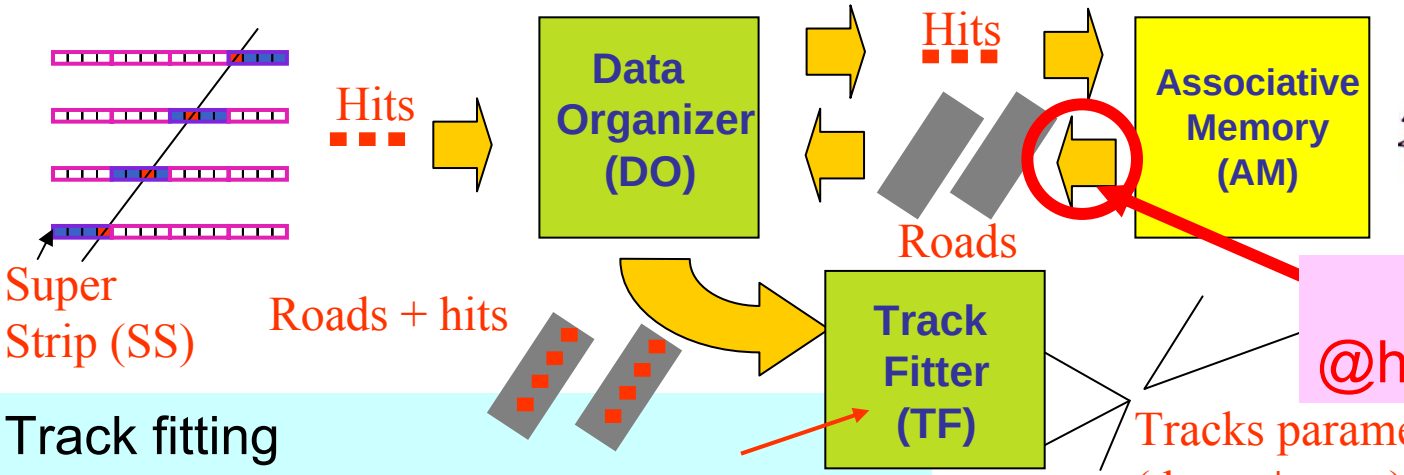
A schematic drawing of the AM



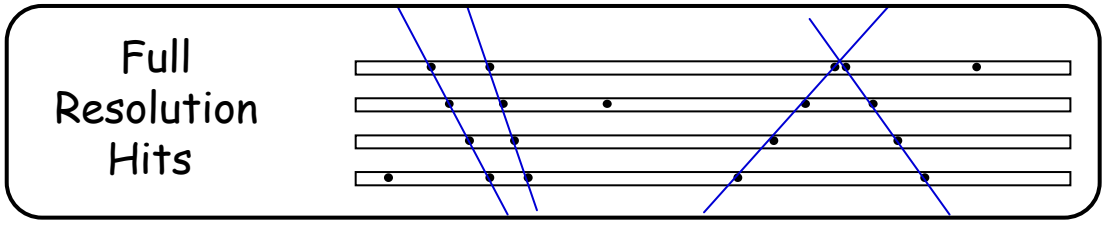
More powerful is the AM better it is. WHY?

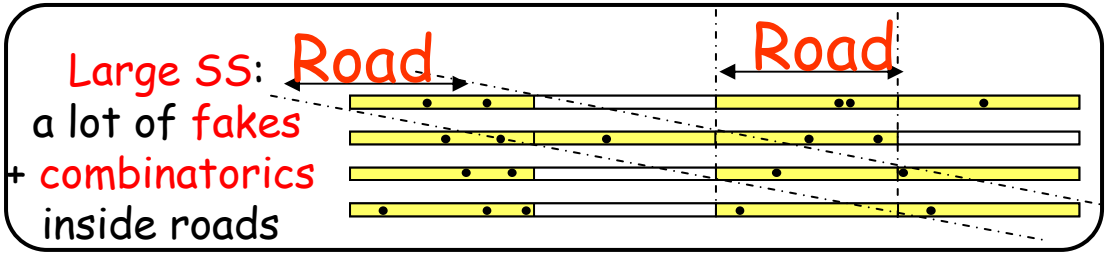
Tracking in 2 steps: find Roads first (*Pattern Matching* with *Associative Memory*, AM) then find Tracks inside Road (Fit by TF)





Track fitting
using full resolution of the detector





Road size: a parameter to balance the AM size & the DO-TF workload

The whole system: Data Formatter + 8 core crates