

PIERRE
AUGER
OBSERVATORY

SDEU: stato produzione, installazione e test

G. Marsella

Introduction

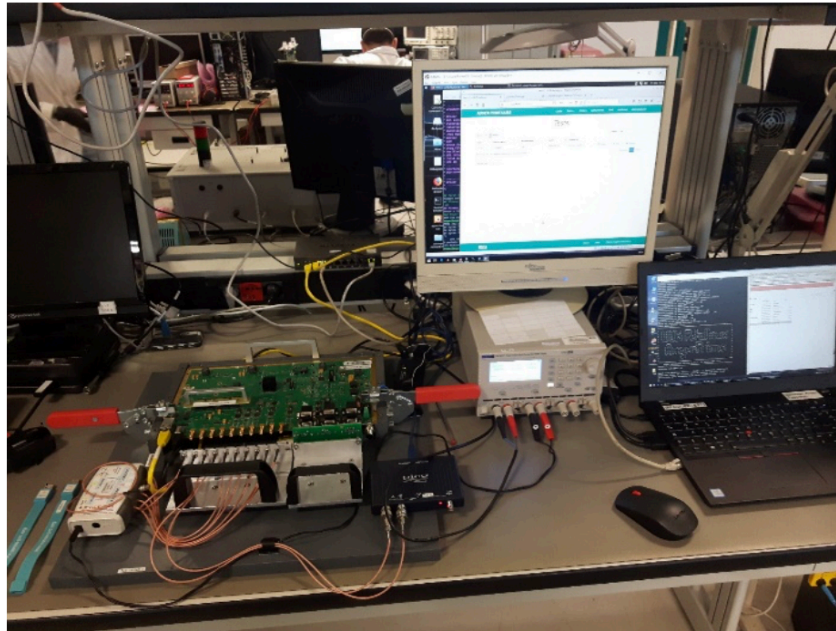
- Stato di Produzione
- Test
- Installazione

Produzione

- Dal 2020 le UUB sono in produzione presso la SITAEL (Mola di Bari, BA)
- Sono già stati prodotti 2X50 batches
 - Dall'esperienza delle prime schede alcune modifiche:
 - 3 hardware engineering changes required: R424/R428, USB power and Jitter Cleaner solder mask
 - Configurazione V_{ref} degli ADC errato (4 Master-1 slave-> montaggio di resistenze)
- Quasi tutte recuperate.
- 5 con problema Efuse
 - 2 mandate in Inghilterra per sostituzione FPGA

TEST System

- One of the manufacturing test bench (KIT) was installed to SITAEI early March.
- All UUBs from the first batch of 50 were tested in SITAEI with remote help.
- The second test bench Has been installed in February 2021.
- At the beginning many problems due to the test-bench itself.
 - Comment: UUB is a complexe board. Only very few people knows details.



Le prime 100

SDE_UUB_UPGRADE - Problem Solving Situation

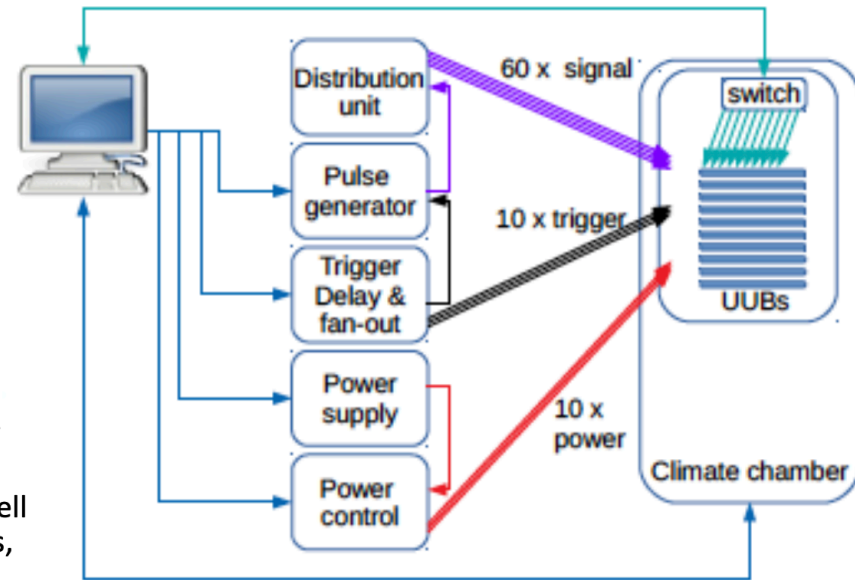
16/12/2020

Part Number	Board	S/N	Test Issue	Failure Analysis
BI9226PMX.10	SCHEDA SDE_UPGRADE_UUB	106	INTERFACCIA ESTERNA 1-2 KO	No short or interruption of the line that arrives on pin 12 of U38 the resistive divider R411 / R417 is ok. At the suggestion of Matthias, U38 was replaced
BI9226PMX.10	SCHEDA SDE_UPGRADE_UUB	150	adc ko	No boot.All the power supplies on the board are OK, except +/- 3V3 ANA (which is enabled after the end of the boot). It seems a problem related to the FPGA. To investigate the issue further, a special JTAG Tools is required which will be provided by G. Marsella
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	119	Boot KO	No boot.
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	115	Reboot	Boot ok, but then the board reboots. All Power Supplies are ok. To be verified together with G. Marsella (like 198)
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	152	comunicazione usb ko	No boot.All the power supplies on the board are OK, except +/- 3V3 ANA (which is enabled after the end of the boot). It seems a problem related to the FPGA. To investigate the issue further, a special JTAG Tools is required which will be provided by G. Marsella
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	177	comunicazione con usb ko	No boot.All the power supplies on the board are OK, except +/- 3V3 ANA (which is enabled after the end of the boot). It seems a problem related to the FPGA.To investigate the issue further, a special JTAG Tools is required which will be provided by G. Marsella
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	183	update ko	Similar to 177, 152, 194, with the difference that the flashing procedure starts but then it returns the error message "Flash Corrupt". To be verified together with G. Marsella
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	187	M68 lifted	M68 has been re-soldered correctly. After that, the board failed the 5mA Test. Problem Solving in progress.
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	189	tank power ko	<i>Manufacture issue. Repaired</i>
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	191	1V ko	<i>Manufacture issue. Repaired</i>
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	194	Boot KO	No boot.All the power supplies on the board are OK, except +/- 3V3 ANA (which is enabled after the end of the boot). It seems a problem related to the FPGA. To investigate the issue further, a special JTAG Tools is required which will be provided by G. Marsella
BI9226PMX.50	SCHEDA SDE_UPGRADE_UUB	198	Boot KO	Boot ok, but then the board reboots. All Power Supplies are ok. To be verified together with G. Marsella (like 115)

Test System

- An ESS test System is installed in Prague

- After green light from manufacturing tests, UUBs are shipped to Prague for ESS tests.
- Prague has now 2 ESS test benches in operation.
 - Pre-test: noise with open connectors, ramp, IR image – one by one
 - Burn-in: (21 hours of rapid temperature cycling), SC values monitored
 - Temperature cycling: -20°C – $+70^{\circ}\text{C}$, dwell time 15 min. at extremes, temperatures, SC values (recorded every 30 sec.)
 - Data acquisition at each measurement point (every $20\text{-}25^{\circ}\text{C}$) triggered by external trigger
 - Results stored in database that will be mirrored to Malargue



ESS test bench

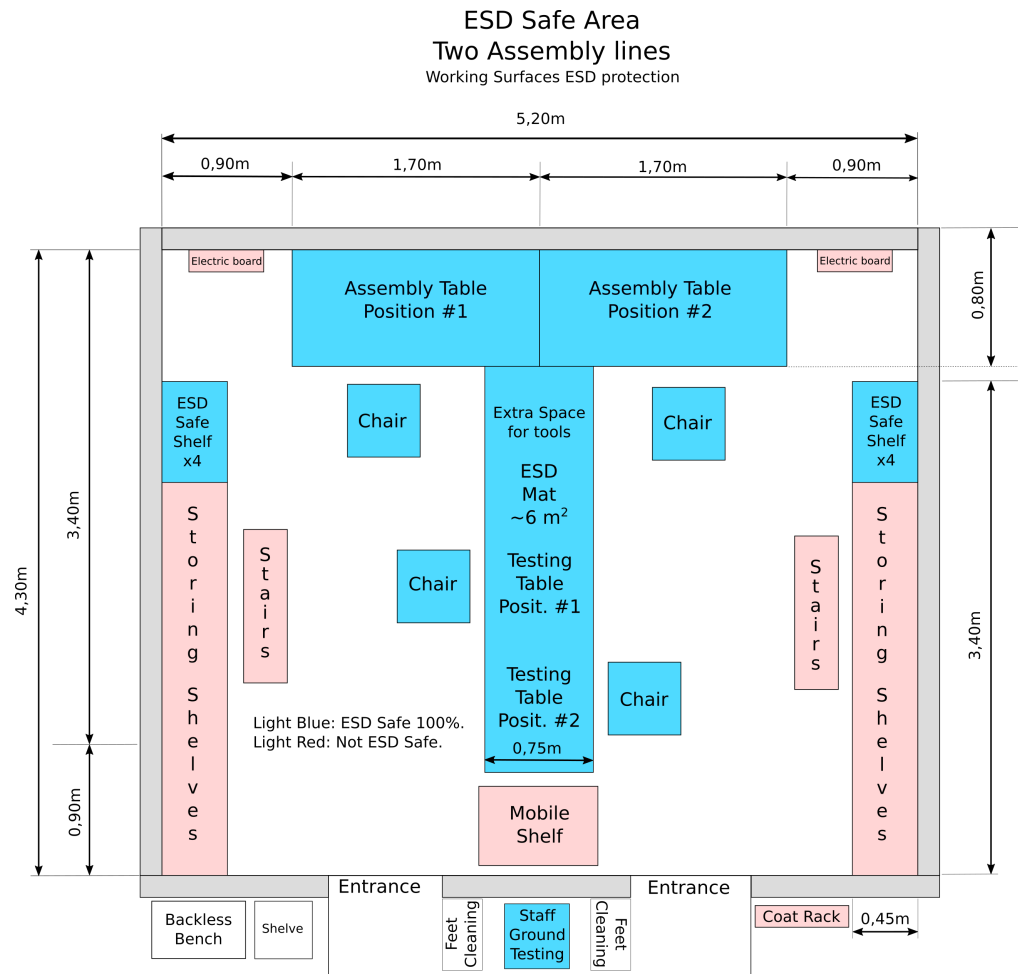
Some little defect detected
(not critical)

Nuova produzione

- 100 schede
 - Su indicazione del panel di review, visti i problemi precedenti, 2 step: 25+75
 - Le prime 25 assemblate e testate: solo 2 failure, 1 l'ho riparata ieri (riprogrammazione flash memory da tftp server...)
- Produzione notevole miglioramento:
 - Nuovo macchinario per ispezione X 3D (permette verifica molto precisa della distribuzione dello stagno)
 - Maggior esperienza (Errori delle prime 100 fisiologici)

Installazione a Malargue

- Nuovo Laboratorio con norme ESD



Installazione nel campo

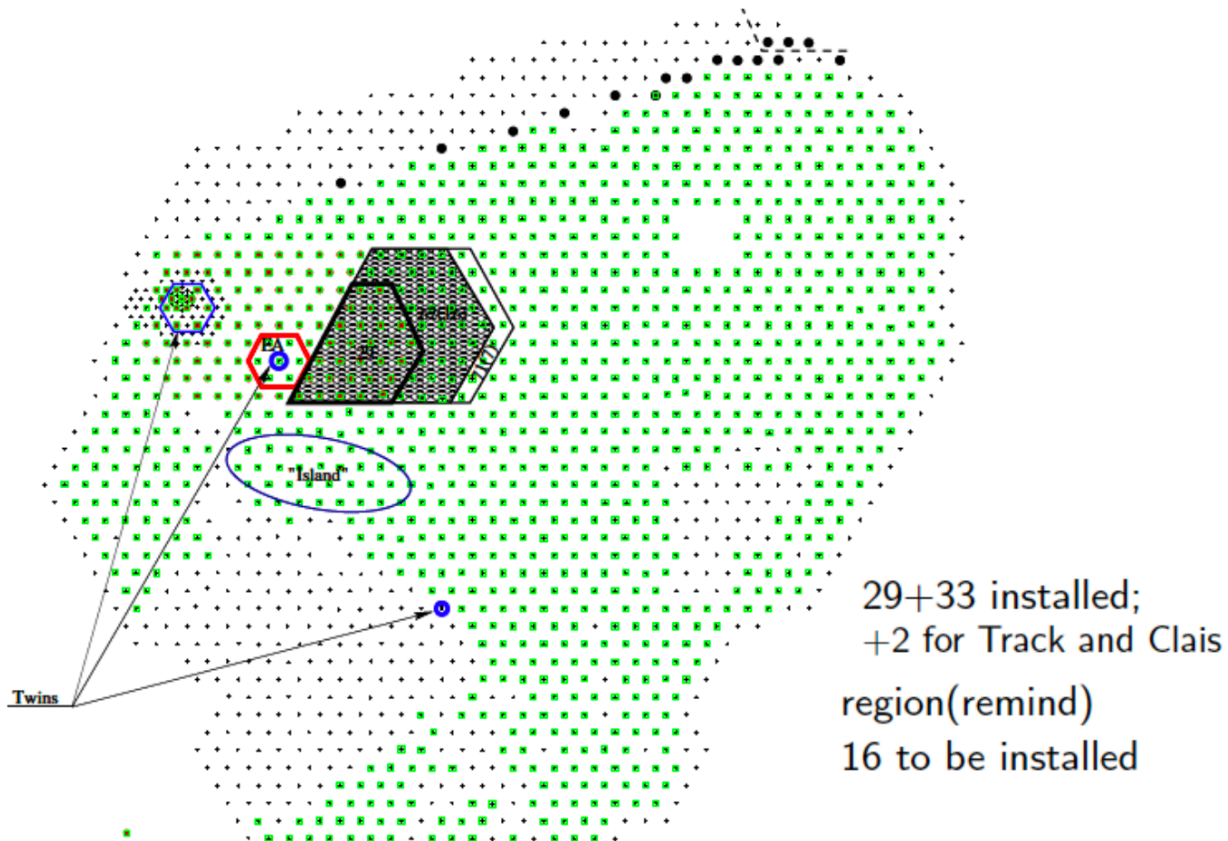


Figure 1: Map of the current pre-production array.

Installazione nel campo

- 7 - EA:

1742*

1744*

1738

1739/56*/59

1737*

1736

1733

- UUB are older version. Are there some additional tests?
- SSD - most are older version. May it be replaced?
- "*" - has RD electronics.
- RD - if installed, maybe not necessary to move.

The list of the remaining UUBs from the 2nd batch, i

StId	UUB	Internal Serial	GPS
56	120	70_cdb0-1401-0000_d4	190244
59	144	70_69b9-1401-0000_a7	190234
833	136	70_a5b6-1401-0000_2a	190232
836	155	70_4fae-1401-0000_8e	190215
1185	159	70_cbc4-1401-0000_14	190228
1214	117	70_60af-1401-0000_d1	190223
1733	169	70_d1bb-1401-0000_82	190176
1736	108	70_b0ad-1401-0000_96	190214
1737	158	70_3db4-1401-0000_b9	190202
1738	147	70_5bd3-1401-0000_88	190231
1739	116	70_22c3-1401-0000_fa	190222
1742	172	70_96cf-1401-0000_00	190229
1744	154	70_56c1-1401-0000_3d	190230
1880	128	70_21cf-1401-0000_82	190212
1881	112	70_cfd9-1401-0000_58	190257

UUB fabrication schedule

The currently estimated schedule is below.

