# FaLaPHEL - Fast Links and Rad-Hard Front-End with Integrated Photonics and Electronics for Physics

## Specifications' document - ver 0.2

## 1 Introduction

Falaphel project has the goal of improving the state of the art of high-speed data links and mixed-signal readout circuits for future high rate pixel detector applications, and of studying the integration of these data links and of analog/digital front-end blocks in a prototype readout circuit. The project targets the tracker of the FCC-hh experiments [1], with the opportunity to replace the innermost layers of the pixel detector systems of the HL-LHC experiments [2] after 2030. The project will exploit innovative circuits and system solutions for system-in-package integration of SiPh components and high-speed electronics. A demonstrator will be fabricated, which will result in a hybrid assembly of an electronic chip (EIC) and of a Silicon photonics chip (PIC).
Two kinds of SiPh modulators will be studied: ring modulators (RM) and Mach-Zehnder modulators (MZM). The EIC will be developed in 28nm TSMC CMOS technology and will include key building blocks able to sustain high-end speed performance in harsh operating conditions.
Key building blocks to be designed and integrated into the final demonstrator are:

- multi-Gbps SerDes, which should be able to combine (Ser) and demultiplex (Des) multiple input sources, e.g. from sensor front-ends (FE), while keeping unaltered their coding (e.g. DC balancing) properties, with particular emphasis on keeping low its power consumption;
- PLL-based frequency synthesizers;
- MZM driver, generating driving signals of 2V while being supplied at about 1V;
- RM driver, generating signals around 1V;

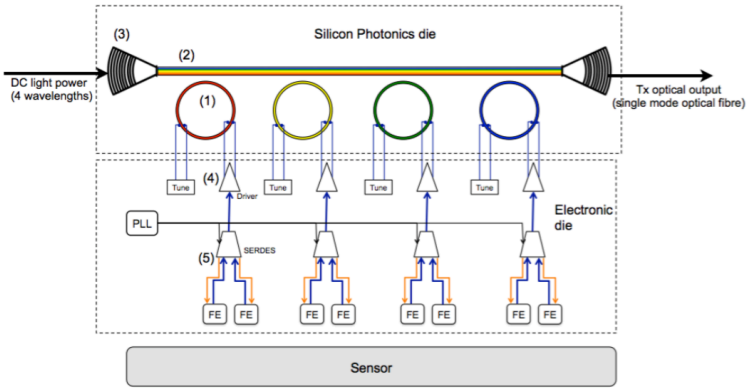


Figure 1: Schematics of the proposed demonstrator. Ring resonators (1) with different and tunable resonator wavelengths are located along horizontally drawn bus waveguides (2) which are connected to optical glass fibres by efficient and robust focusing grating couplers (3). Data from the front-ends (FE) and serializers (5) are sent to the drivers (4). The Front-End (FE) is embedded in the demonstrator but it can be bypassed. The sensor is not part of the demonstrator.

- Analog front-end circuits: low-noise charge-sensitive preamplifier, discriminator for Time-Over-Threshold measurements. An important goal of the project is the definition of criteria to achieve low noise and low threshold dispersion with rad-hard analog circuits operating at low-power in a high-speed digital environment.

Different solutions for the final demonstrator will be investigated, before its realization, optimizing the speed, the power and the integration aspects. The tentative solution is based on Wavelength Division Multiplexing (WDM) with four ring modulators as shown in Fig. 1, tuned at different wavelengths. In the final demonstrator the front-end matrix could be by-passed and replaced with a pseudo random bit stream (PRBS) generator.
A selection of the main requirements for the blocks to be integrated in the final demonstrator is given in the following.

## 2 General specifications

The most critical requirements are associated with the extremely high data rates and radiation levels foreseen for the tracker systems of next generation *hh* colliders. This

specifications' document is shaped on the requirements for the outer layers of the tracker at a FCC-hh detector, with a possible upgrade of the Phase 2 LHC pixel detectors in mind. The requirements for the main performance parameters of the demonstrator to be developed in the Falaphel project are listed in Table 1. The quoted operating temperature range is

Table 1: Main specifications

| **Specification** | **Value** | **Comments** |
|---|---|---|
| Operating temperature | -40°C to + 85°C | perform in this range |
| Typical operating temperature | -20°C | |
| Total Ionizing Dose | $\leq$1 Grad | delivered at room T |
| 1 MeV equivalent neutron fluence | $< 5\times 10^{16}$ n/cm$^2$ | |
| Pixel hit rate | 6 GHz/cm$^2$ | |
| Data rate | 100 Gb/s | aggregated |

the standard industrial. In this range, the developed blocks have to be operational, even if not complying with specifications. Ensuring that the main blocks work in the upper limit of this range will allow the chips to work in basic test setups where cooling may not be available. The compliance with a 6 GHz/cm$^2$ hit rate and 100 Gb/s data rate should be preserved at the highest expected irradiation levels.

## 3 Analog front-end specifications

The analog front-end to be developed in the Falaphel projects inherits the basic structure, shown in Fig. 2 with some transistor level details, of the RD53 Linear Front-end [4]. The readout chain includes a charge sensitive amplifier (CSA) featuring a Krummenacher feedback [5] complying with the expected large radiation induced increase in the detector leakage current. The signal from the CSA is fed to a low power comparator exploited for time-to-digital conversion. Channel to channel dispersion of the threshold is addressed by means of a local circuit for threshold adjustment. An injection circuit will allow to generate programmable test signals at the front-end input. The analog channel will be equipped with a bank of capacitors, shunting the preamplifier input, with the purpose of emulating the presence of a detector capacitance. A bump pad will be laid out in each cell, enabling the connection of the final demonstrator to available sensors. The requirements for the main performance parameters of the analog front-end are summarized in Table 2.
A target pixel cell size of 25 $\times$ 50 $\mu$m$^2$ will be pursued in Falaphel. This is a factor of two smaller with respect to RD53 pixels, and can potentially provide improved pile-up mitigation and vertex reconstruction capabilities in the pixel systems of the HL-LHC. About half of the total pixel cell area will be allocated to the analog front-end.

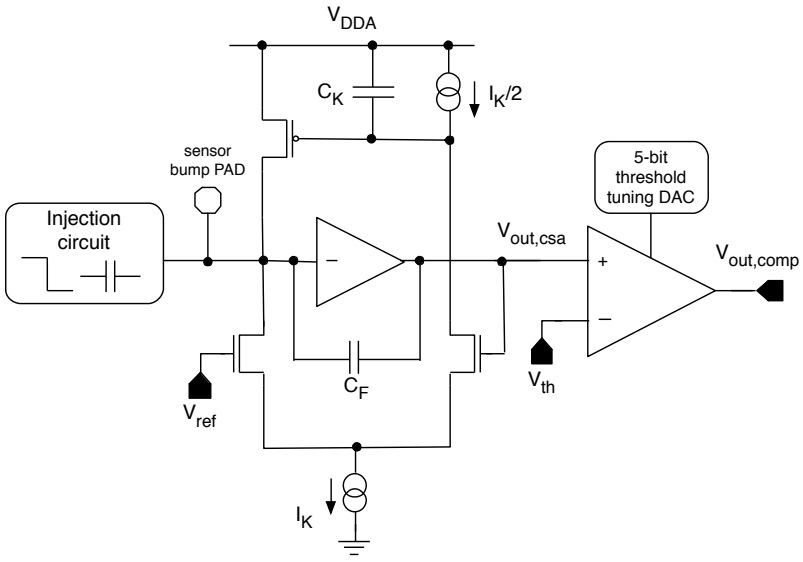


Figure 2: Schematic of the CMS analog front-end

The requirement of a maximum power dissipation density of 0.5 W/cm$^2$ leads to the definition of 6.25 $\mu$W per-channel power consumption.
A detector capacitance smaller than 100 fF has been specified. Its actual value obviously depends on pixel geometry and technology (planar or 3D sensors). Nonetheless, the front-end must be stable also with no sensor connected to the readout matrix.
Un upper limit of 20 nA has been specified for the detector leakage current. The front-end should be fully operational at such a limit, with a leakage compensation circuit preventing any effect of the sensor leakage current on the preamplifier response to detector signals. Nonetheless, an increase in the equivalent noise charge is expected for non-zero detector leakage currents. Noise performance, together with threshold dispersion properties of the front-end, has to ensure operation with a noise occupancy smaller than $10^{-6}$.
The front-end channel should handle a dynamic range from around 0.1 MIP up to 10 MIP. A linear behaviour, even though not strictly needed, should be pursued in a range from 0.1 up to 4 MIP. A recovery time not exceeding 1 $\mu$s has to be ensured for large signals (>4 MIP) in order to keep channel dead-time under control.
Time-walk performance is also of utmost importance: a so-called in-time overdrive of 300 e$^-$ has been specified, meaning that for a 600 e$^-$ minimum threshold a 900 e$^-$ signal will have a 50% probability of generating a hit signal at the comparator output with a time delay within 25 ns of very large signals.
Last, analog front-end circuits need to be isolated from the digital section of the pixel

Table 2: Front-end specifications

| **Specification** | **Value** | **Comments** |
|---|---|---|
| Pixel size | $25 \times 50$ $\mu m^2$ | analog and digital circuits |
| Power consumption | 0.5 W/cm$^2$ | periphery consumption not included |
| Sensor signal polarity | negative | collection of electrons |
| Detector capacitance | <100 fF | |
| Detector leakage | <20 nA | |
| Minimum MIP charge | 4000 e$^-$ | at highest irradiation level |
| Minimum stable threshold | 600 e$^-$ | 50 fF load |
| In-time overdrive | 300 e$^-$ | min. charge above threshold resulting in <25 ns time walk |
| Minimum in-time threshold | 900 e$^-$ | 50 fF load. Simply the sum of the two above lines |
| Noise occupancy | $<10^{-6}$ | 50 fF load |
| Hit loss from in-pixel pileup | $\leq$1% | at 6 GHz/cm$^2$ hit rate |
| Recovery from saturation | <1 $\mu$s | |
| Isolation of analog circuits | analog DNW only | digital circuits in global substrate |

readout chip. Digital-to-analog interferences should be kept below the electronic noise level. This should be accomplished by avoiding the integration of any transistor in the analog front-end in the global p-type substrate of the chip. Instead, all transistors should be isolated using N-wells (PMOS) or deep N-wells (NMOS).

# 4 Specifications for the high-speed electronics

Recent and future developments of pixel detectors require to transmit an increasing amount of data off the readout chip. As mentioned in section 2, Falaphel targets an aggregated data rate of 100 Gb/s. The key building blocks to be developed, integrated and tested are:

- 25 Gb/s serializers/SerDes;
- 25 Gb/s drivers;
- 25 GHz PLL.

The main specifications for serializers and drivers are reported in Tab 3. The performance

Table 3: Main specifications for serializers and drivers

| **Specification** | **Value** | **Comments** |
|---|---|---|
| Data rate | 25 Gb/s | |
| Power consumption (SerDes) | <1.5 W | for a 20-bit SerDes. <1 W in the case of a simple serializer. |
| Power consumption (Driver) | < 25 mW | |
| Area (SerDes) | < 0.25 $mm^2$ | for a 20-bit SerDes |
| Area (Driver) | < 0.30 $mm^2$ | |

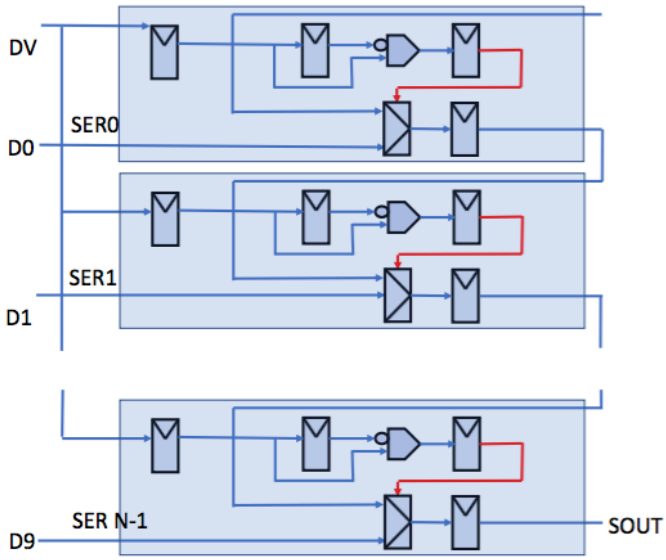


Figure 3: General architecture of the SerDes

of serializers and drivers should be retained also at the highest expected radiation levels. The architecture of the SerDes is based on a daisy chain of identical cells with load internally generated at the rising edge of the *data valid*, as shown in Fig. 3.

The main specifications of the PLL, operating at a nominal frequency of 25 GHz, are gathered in Tab. 4. A number of additional output frequencies should be generated by the PLL. In particular:

- 6.25 GHZ (standard spacefiber);

Table 4: Main specifications for the PLL

| **Specification** | **Value** | **Comments** |
|---|---|---|
| Operating frequency | 25 GHz | |
| Power consumption | < ~~50 mW~~ 100 mW | |
| Phase noise | < -90 dBc/Hz at 1 MHz | |
| Area | < ~~0.10 mm$^2$~~ 1.0 mm$^2$ | |

- 3.125 GHz (maybe we can remove this?);
- 1.5625 GHz (maybe we can remove this?);
- 312.5 MHz;
- 156.25 MHz;

## 5 Specifications for the ring modulator

The baseline solution for the development of the demonstrator is shown in Fig. 1 and is base on WDM with four ring modulators. Compared to classic VCSEL, or LED light transmitters, Silicon Photonics optical modulators (such as ring modulators or MZM) are more robust to radiation [4]. In SiPh-based optical links, the possibility to use remotely located single-mode laser sources reduces the requirement on the radiation hardness of the light source. The advantages of using RM are their small footprint (dense integration), low power, high speed, suitability for wavelength division multiplexing. Wavelength tuning of the modulators and receivers is required for channel selection and in order to compensate for fabrication tolerances and temperature changes. Thermal tuning, using local heaters on top of the ring structures, will be used and optimized through coupled thermo-optic

Table 5: Main specifications for the ring modulators

| **Specification** | **Value** | **Comments** |
|---|---|---|
| Ring radius | 5 $\mu$m | |
| Free spectral range | 19-20 nm | at 1550 nm |
| Heater efficiency | 0.18 nm/mW | |
| Modulation efficiency | 40 pm/V | |
| Insertion loss | 5 dB | |

simulations to achieve low power operation.
The main specifications of the ring modulator are gathered in Tab. 5.

## References


[1] Abada, A., Abbrescia, M., AbdusSalam, S.S. et al. "FCC-hh: The Hadron Collider". *Eur. Phys. J. Spec. Top. 228*, 755-1107, 2019.

[2] CMS Coll. "The Phase-2 Upgrade of the CMS Tracker", *CERN-LHCC-2017-009 ; CMS-TDR- 014.*

[3] M. Garcia-Sciveres and J. Christainsen, "RD Collaboration Proposal: Development of pixel readout integrated circuits for extreme rate and radiation", *http://cds.cern.ch/record/1553467, CERN-LHCC-2013-008.*

[4] L.Gaioni et al. "Design of analog front-ends for the RD53 demonstrator chip", *PoS Vertex 2016 036*, 2017.

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