Falaphel INFN Project

WP 2 Silicon Photonics

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INSTITUTE
OF COMMUNICATION,
INFORMATION
AND PERCEPTION
TECHNOLOGIES

Scuola Superiore
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WP 2 Silicon Photonics

WP2 (Silicon Photonics) It will develop the SiPh building blocks.including RM, MZM,bus waveguides, optical couplers and splitter, integrated thermal heaters. It will submit the MPW of a mini-block chip (2.5x~5 mm^2). The fabricated mini-block will be characterised, providing information for the design and fabrication of the second full block chip (5x~5 mm^2) that will be tested allowing the final integration with EIC.

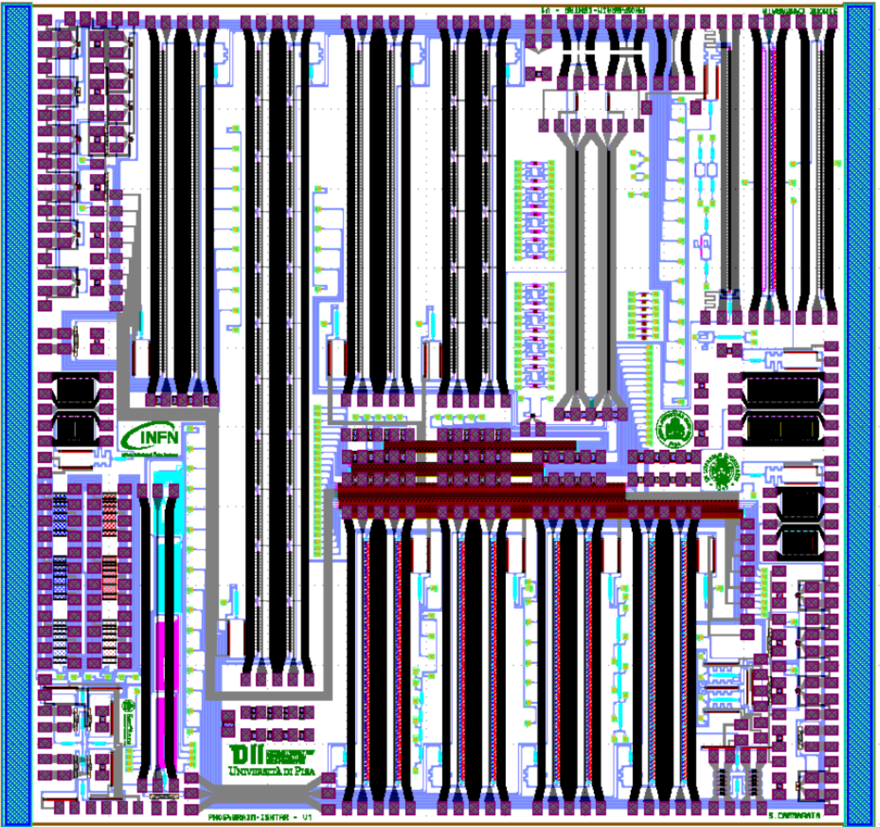
D2.1 SiPh submissions for the MPW run of the first miniblock including the building blocks (SSSA, INFN PI, UNIPI, UNIMI) (T0+7)

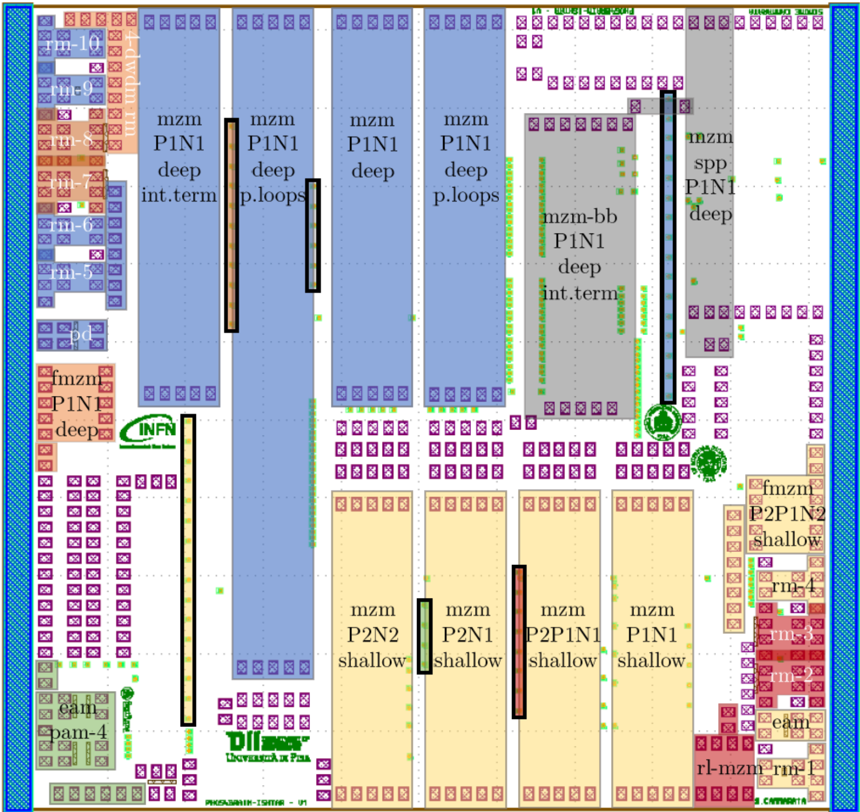
D2.2 SiPh submission for the MPW run full final block (SSSA, INFN PI, UNIPI, UNIMI) (T0+19)

D2.3 SiPh final PIC characterization (SSSA) (T0+31)

Phos4Brain Chip

Final chip delivery postponed in August 2021





Tape Layout of the submitted design (June 2020)

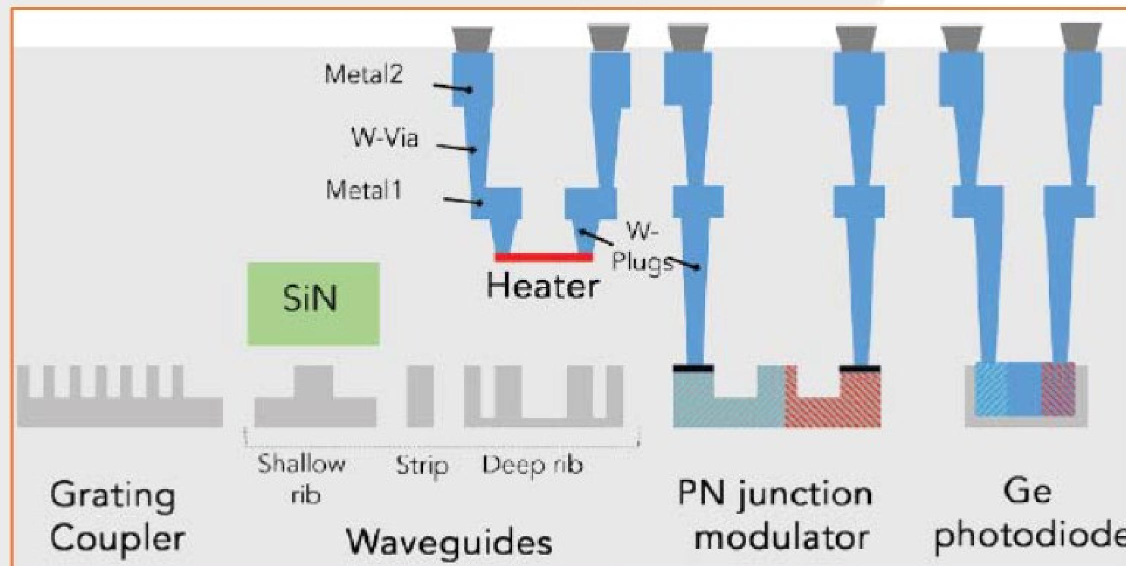
MPW run deadline 2021

SiPh submissions for the MPW run of the first miniblock
2021 IMEC MPW run schedule
Half block 5.15mm x 2.5mm Price : 19 k€

imec

imec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
imec Si-Photonics Passives+					12					13		
imec Si-Photonics iSiPP50G			10					25				
imec SiN-Photonics BioPIX 300					4							
imec GaN-IC on SOI 200V				21								
imec GaN-IC on SOI 650V	20									20		

CEA/LETI Platform



200mm **SOI substrate** with
310nm Si and
2µm buried oxide
6 implant levels for p-type and n-type for modulators and doped Si heaters

Cost with SiN Module 1500 €/mm2

Active components
High speed Photodetectors
High speed Modulators

Option
Optical edge coupler
Under Bump Metallization
Bumps & µ-Bumps deposition

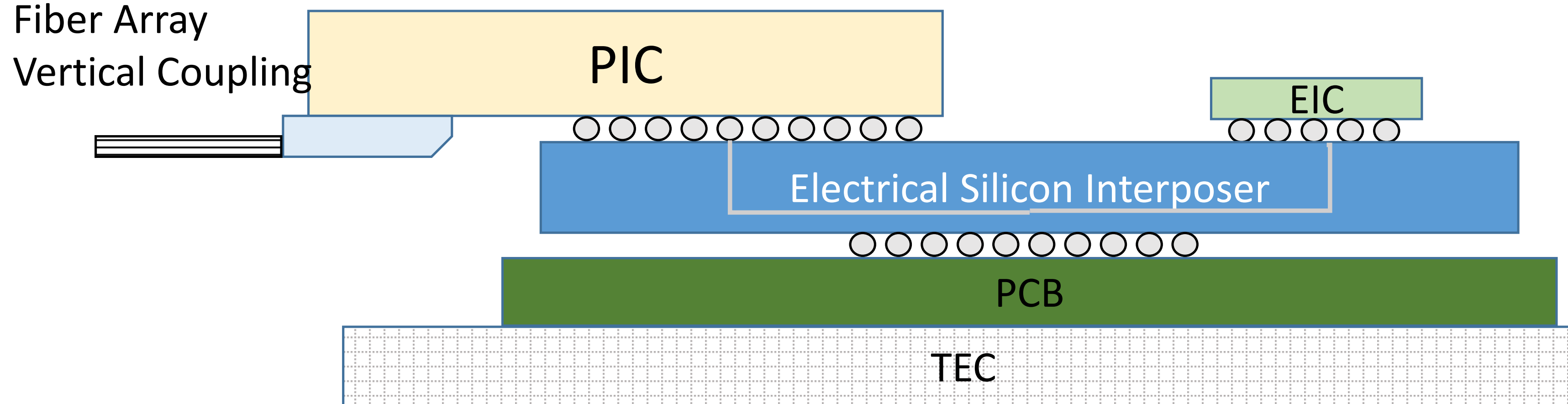
MPW Run deadline October 2021

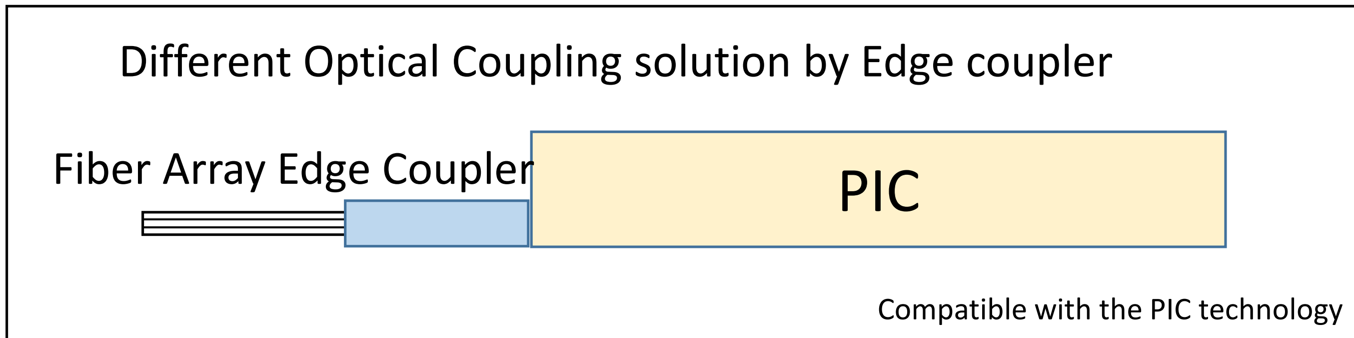
PIC/EIC Integration

Exploring possible solutions with the following technology centers

- Inphotec (2D Integration , 3D integration)
- Tyndall (2D and 3D integration)
- CEA –Leti (2.5 D integration through silicon interposer)

PIC/EIC 2.5 Integration - Interposer





To be defined Bond Bump Material and packaging rules (Pitch, exclusions,…..)
Silicon Interposer for rad hard applications

PIC (1 chip)
Technology IMEC
Dimension (IMEC) 5x5 mm^2
Evaluating other Technology: LETI (?)

Optical I/O max 16 Optical Fiber
Pitch fiber array 127 μm

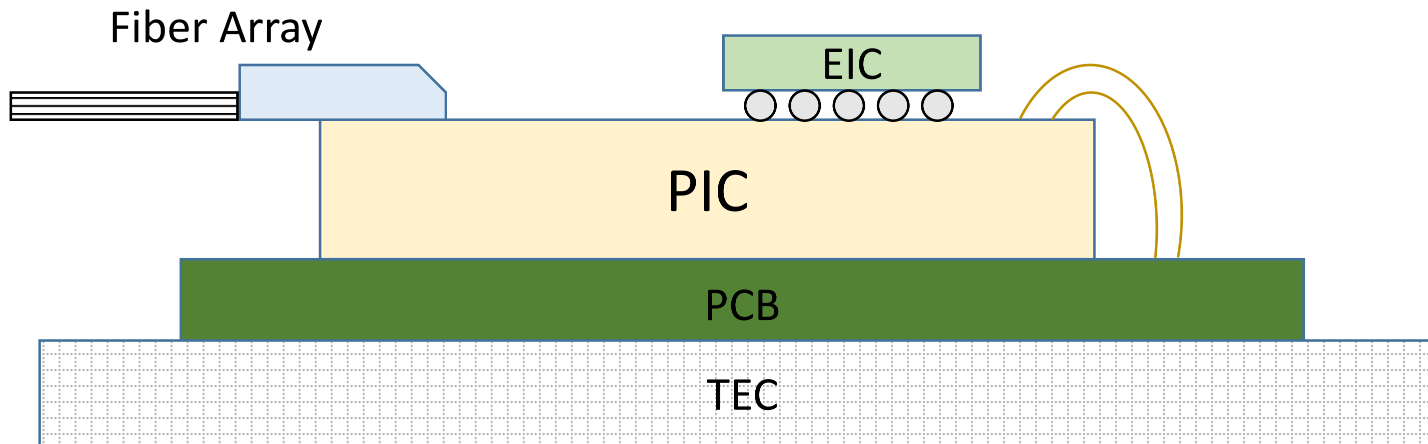
Electrical Pad dimension
Pad 75x55 μm^2
Pitch 100 μm

Data rate 10-25Gbs

EIC (4-5 Chip)
Technology 28 nm TSMC
Pitch 50-100 um
Dimension 1 -2 mm^2

Thermal Issues to be taken into account

PIC/EIC 3D Integration



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Pitch 100 μm

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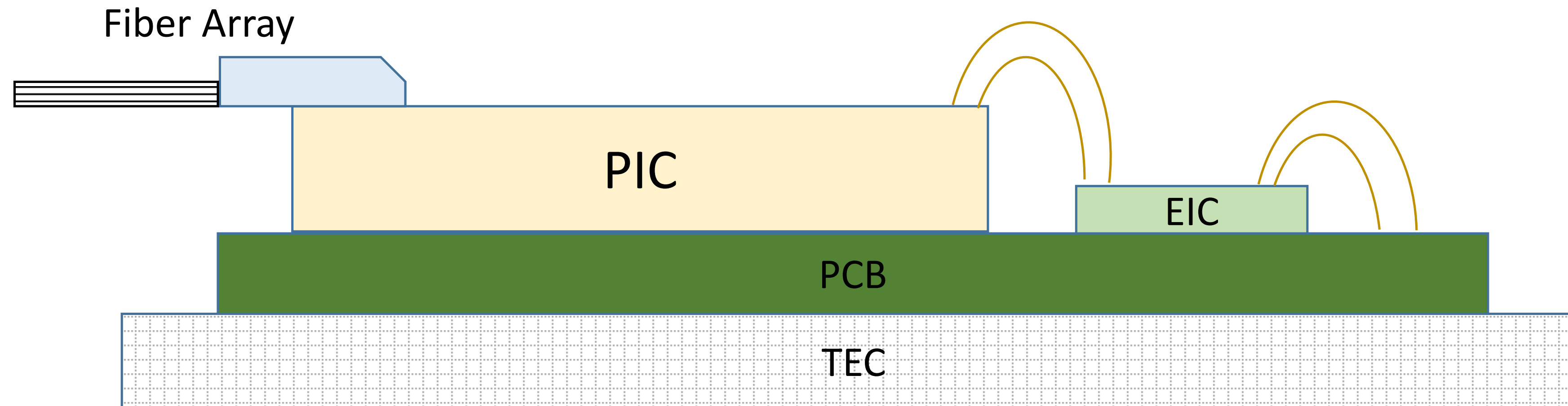
EIC (4-5 Chip)
Technology 28 nm TSMC
Pitch 50-100 um
Dimension 1 -2 mm^2

Thermal Issues to be taken into account

PIC/EIC 2D Integration



To be defined Bond Bump Material and packaging rules (Pitch, exclusions,…..)

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Technology IMEC
Dimension (IMEC) 5x5 mm^2
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Pitch 50-100 um
Dimension 1 -2 mm^2

Thermal Issues to be taken into account

AdR Recruitment

Table 6. Requested AdR. Type: Junior (J) / Senior (S)

AdR #	Type	Unit	Months	Research Topic
1	J	PI	30	PIC design and test. PIC-EIC integration and test
2	S	PI	24	Driver design. PIC-EIC integration and test
3	J	PI	18	PLL/CDR design and test
4	J	PV	30	DAC design and test
5	S	PV	24	FE design, test and integration in the demonstrator
6	J	PD	24	Irradiation tests and analysis

INFN Call n. 23192/2021 to award 1 grant for technological research:
Topic: Design and test of integrated, radiation-tolerant photonic circuits for high-energy physics experiments

Deadline for the application 11th of June 2021