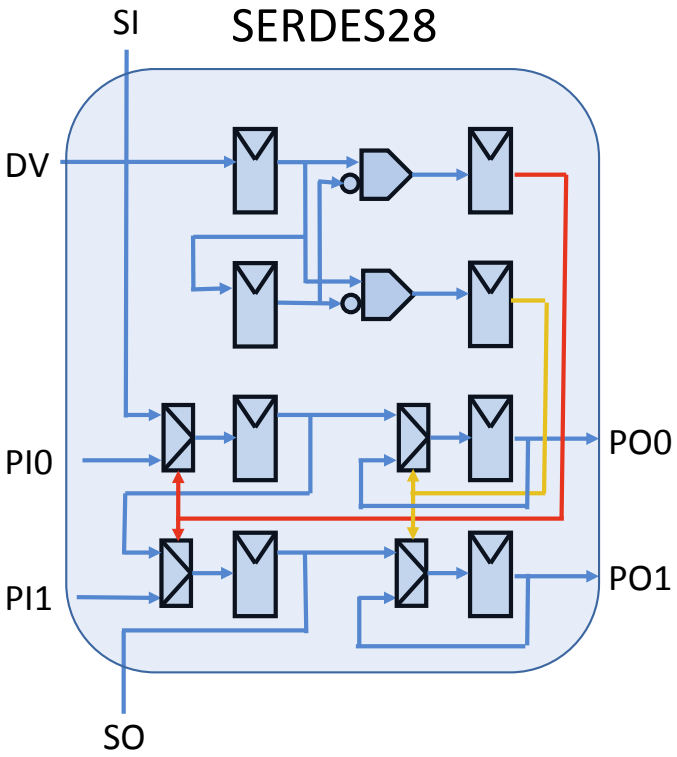
WP3 – IP Cores

Falaphel Meeting – June 8th 2021

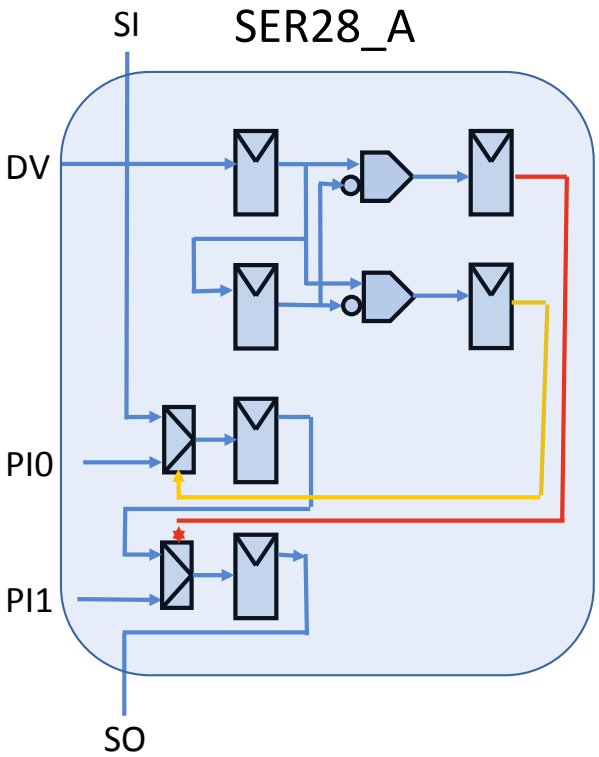
IP Cores: Tasks & Resources

- Guido Magazzu'
  - SERDES
  - SLVS TX/RX (1.25GHz)
- Gabriele Ciarpi
  - I/O Pads
  - CML TX/RX (25GHz)
  - RO Driver (25Gbps)
- Danilo Monda (Paolo Prosperi and Daniele Vogrig)
  - VCO28 Test and Characterization
- Valentino Liberali (Luca Frontini)
  - Built-In Test Engine for SER Test and Characterization

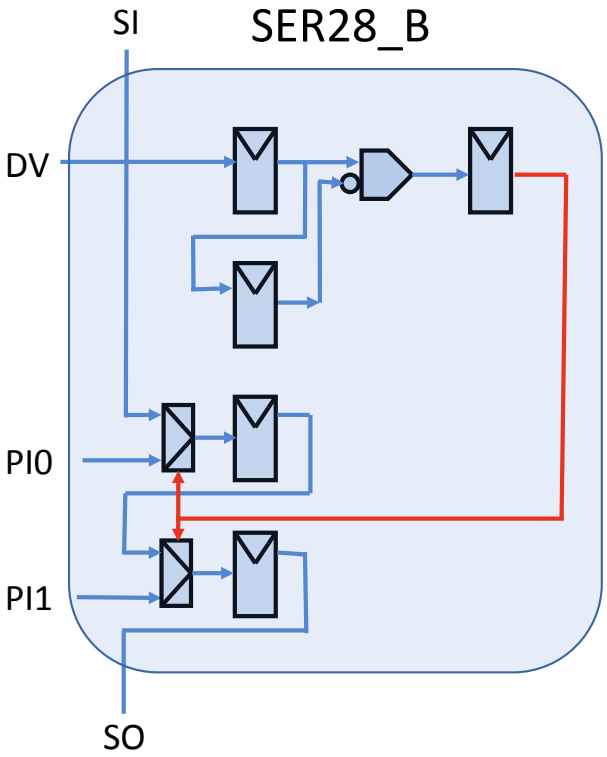
SERDES28 (1)



5x8 = 40 rows (6-stages clock tree)



5x6 = 30 rows (5-stages clock tree)

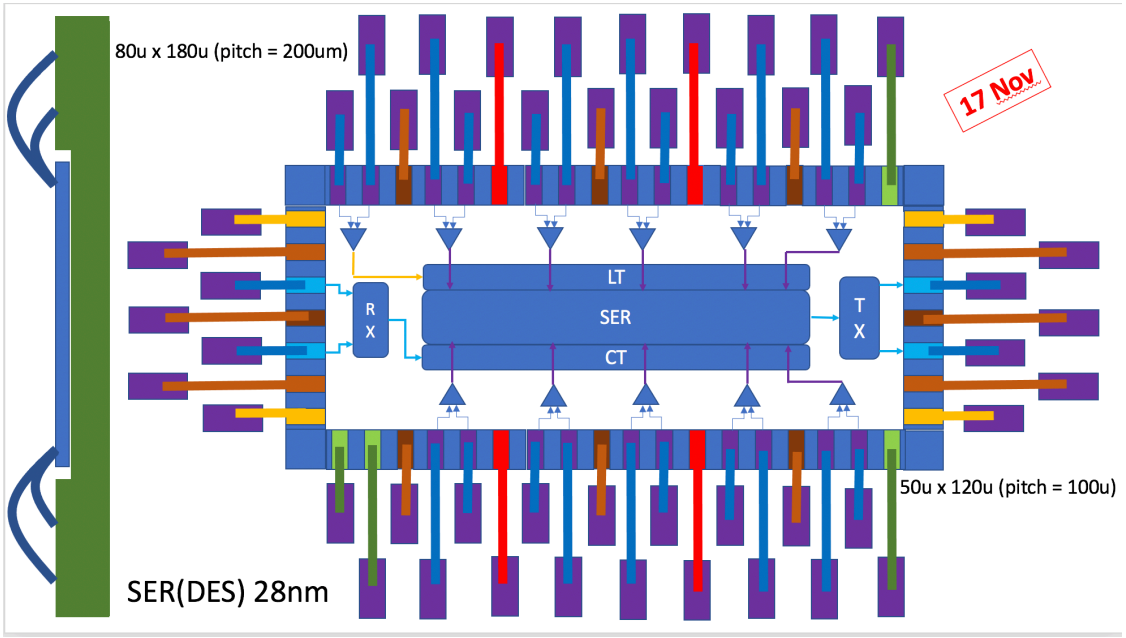


5x5 = 25 rows (5-stages clock tree)

SERDES28 (2)

- Project Status @ May 31st (before WS failure)
  - layout of the SERDES28 array and of the Clock Tree completed
  - Post-layout simulations performed (max data rate = 12.5Gbps in typical conditions)
- On-Going activities (goal => higher data rate)
  - Design of SER28_A and SER28_B arrays
  - New DFFMUX designed with a reduced voltage swing (200/300mV vs. 400mV)
  - Design of SLVS TX/RX (with Gabriele)
- Milestones
  - August 15th => Design of SERDES (SER) and SLVS TX/RX completed
  - September 30th => Integration with CML TX/RX (from Gabriele) completed
  - October 31st => Final verifications completed
  - November 17th => Chip submission

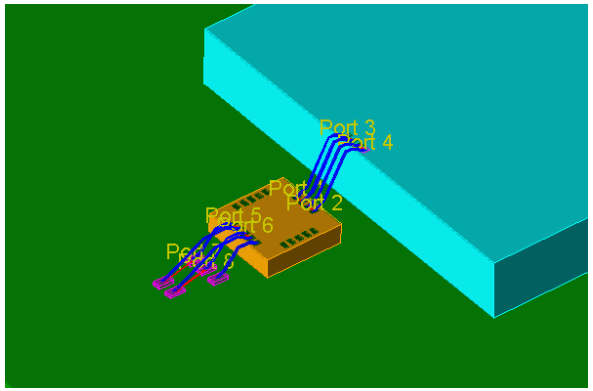
SERDES28 (3)

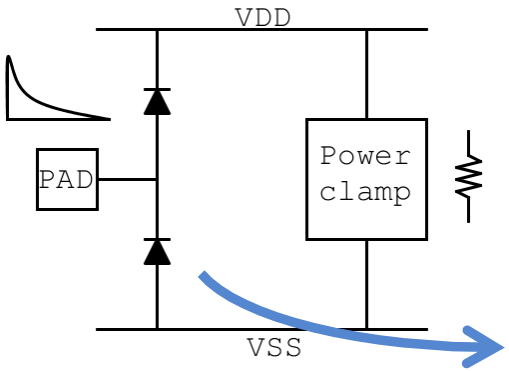


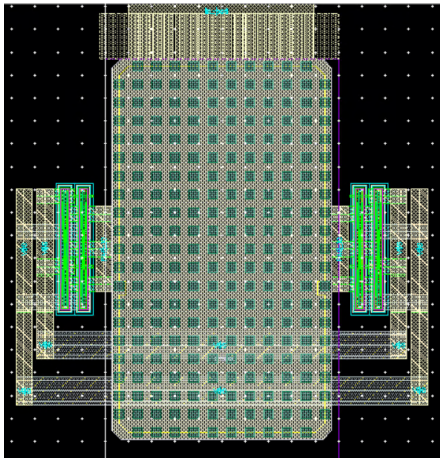
Signal	Type	#
Parallel Input	SLVS	2 x 10
Data Valid	SLVS	2 x 1
Clock	CML	2 x 1
Serial Out	CML	2 x 1
VDD (CORE)		4
GND (CORE)		6
VDD (IO)		4
GND (IO)		6
VBIAS		4
		50

PADs and ESD protections

- ESD parasitics reduce the bandwidth of the EIC-PIC and EIC-board links.
- Low parasitic (capacitance) ESD should be designed for high-speed communication.
- Low capacitance ESD could lead to low ESD protection





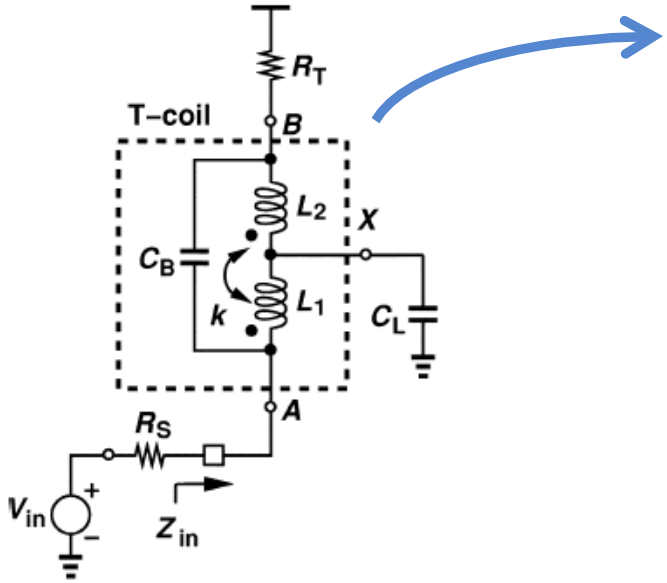


In-house (HPC tech)

- 1 kV and 2 kV HBM ESD with low capacitance (100-200 fF)
- Low resistance Power clamps

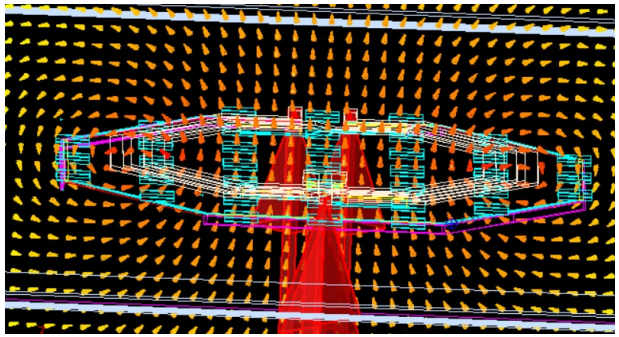
Inductors: EM simulations

- Circuital techniques could be used to face the large ESD parasitics capacitance for high-speed link.



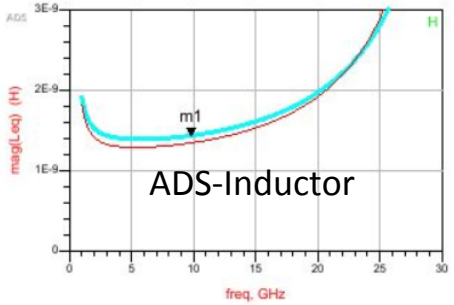
S. Galag, B. Razavi, «Broadband ESD Protection Circuits on CMOS Technology», IEEE Journal of Solid-State Circuits, vol. 38, n. 12, 2013

Custom inductor design in ADS Keysight

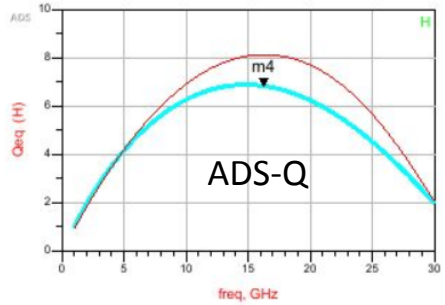


PDK-ADS discrepancies

ΔL=9.89%

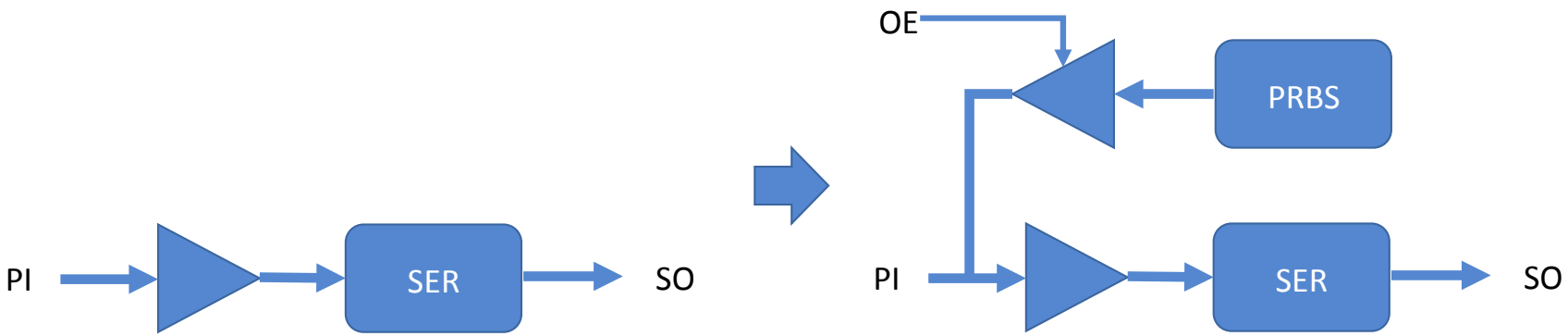


ΔQ=55% ?

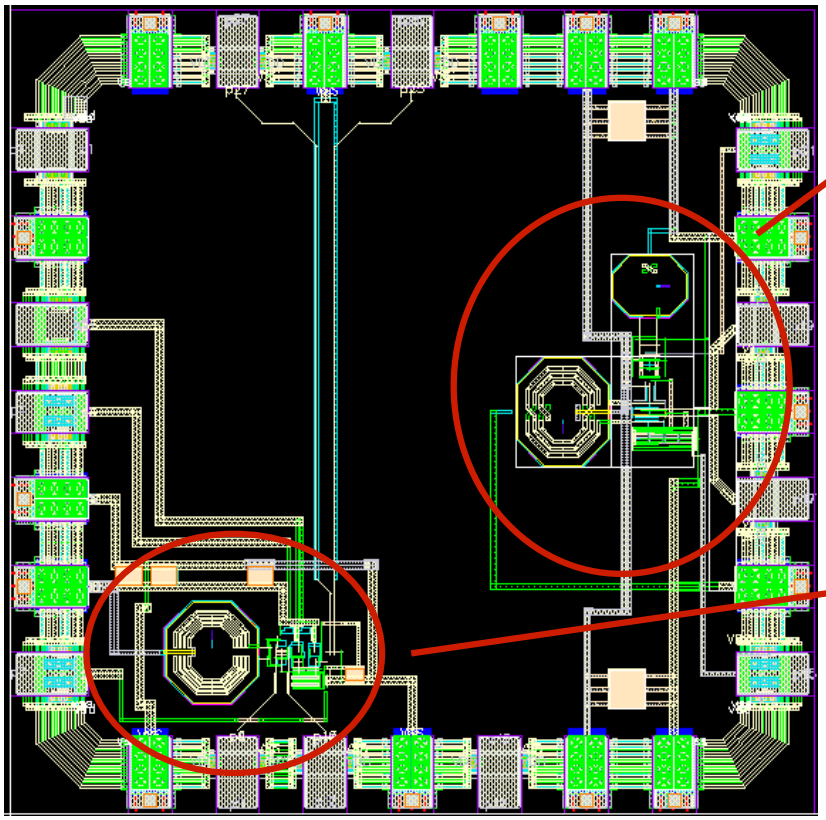


Built-In SER Test

- Built-In Test required for ”large” SER prototypes (Nbit > 10)
  - Limited number of pads available for parallel port in IC prototypes (max 10 bits)
  - Difficult access to DUTs in Irradiation Test facilities



VCO



VCO28 prototypes delivered and ready to be tested and characterized

LC-Tank VCO

- Complementary VCO architecture
- Two-stage output buffer with inductive peaking
- Working frequency 23.8 GHz ÷ 26.47 GHz
- Phase Noise ≈ -100 ÷ -115 dBc/Hz
- Power consumption < 3 mW
- Rad-hard design

Driver

- High speed 25 Gb/s driver for ring resonators
- CML architecture with inductive peaking bandwidth enhancement
- TID tolerant techniques implemented

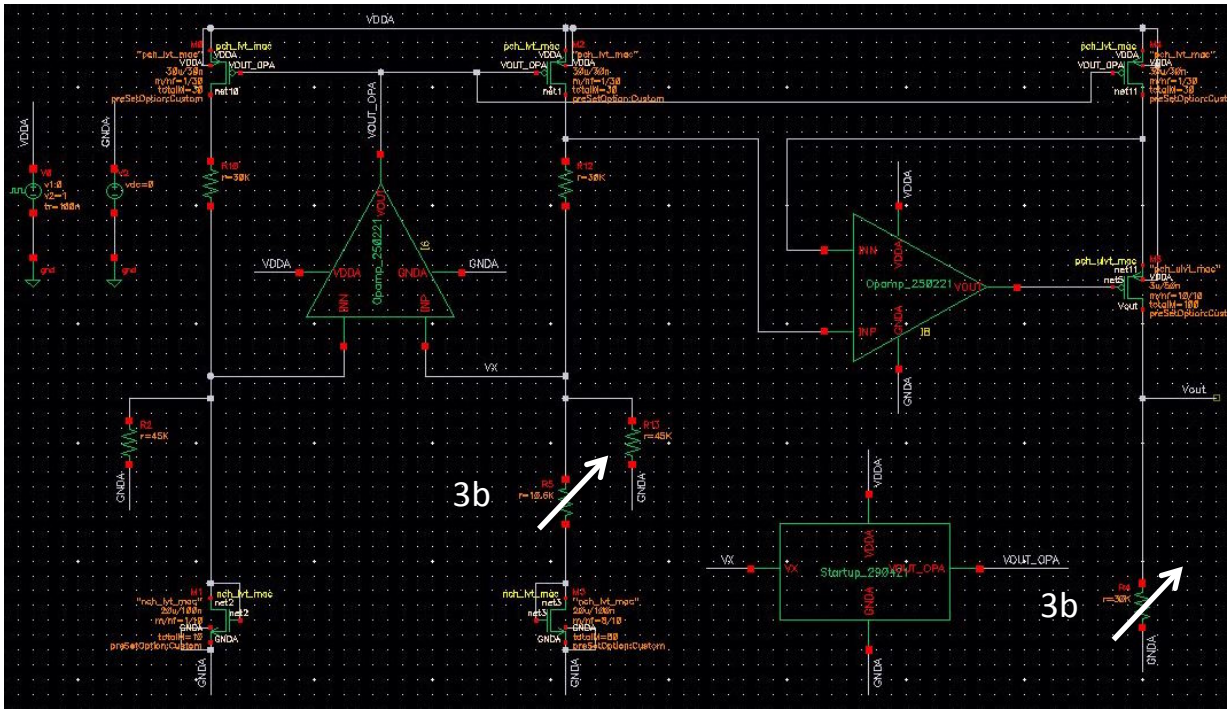
Danilo Monda

WP3 – FE

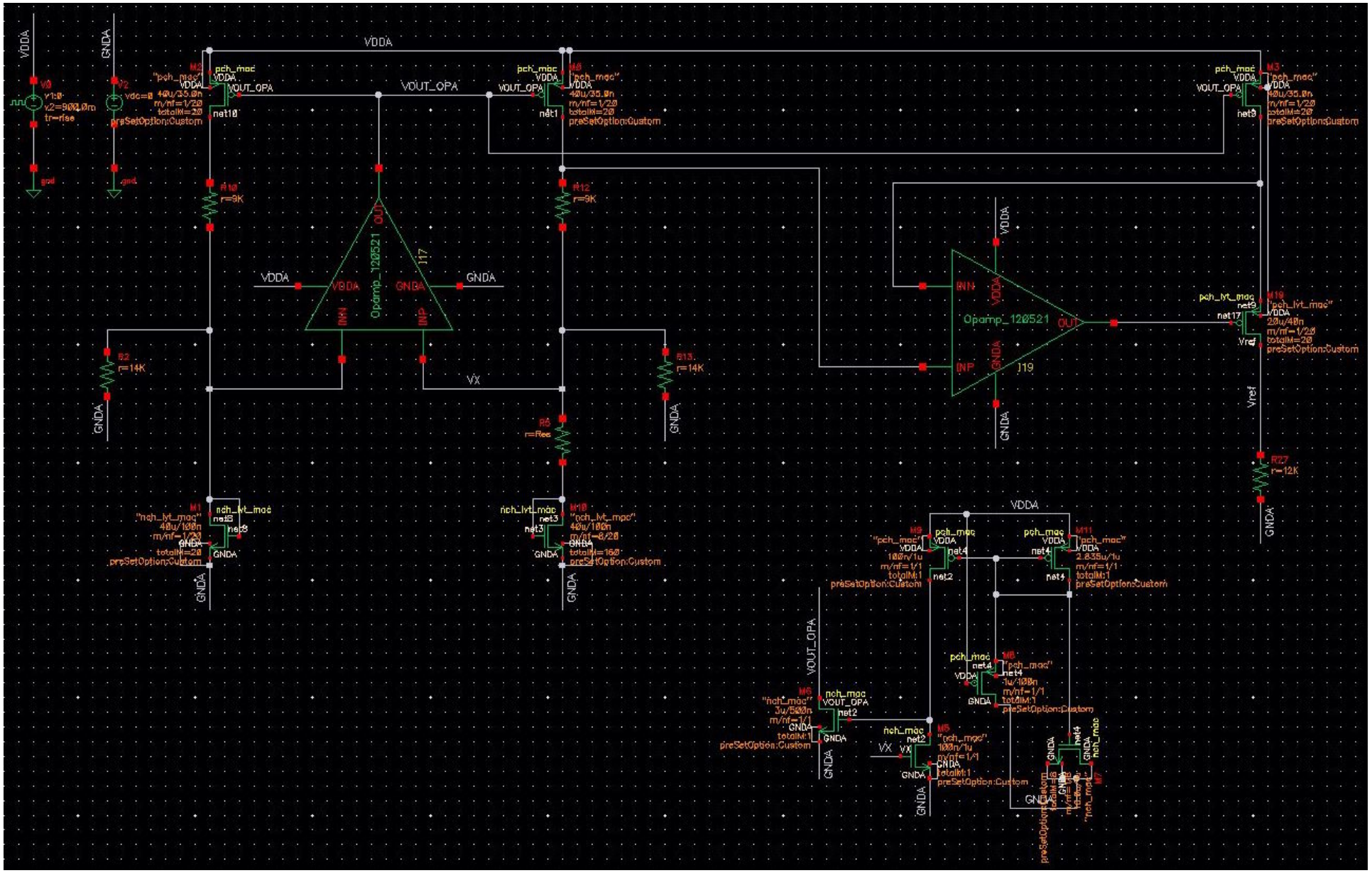
Falaphel Meeting – June 8th 2021

Design specifications and characteristics

Parameter	Value
Size	O 250um X 250um
Supply voltage (V_{DD})	0.9 V ± 10%
Power	O 100 uW
Temperature range	-40°C + 60°C
$\Delta Vref_{MAX}$ vs T	450 mV ± 3 mV (temperature coefficient to be calc.) More than one value?
$\Delta Vref_{MAX}$ vs $0.9V_{DD} \div 1.1V_{DD}$	2mV (line regulation to be calc.)
PSR	<-20dB @100Hz and <-20dB @10MHz
Metal layers used	M1-M2-M3-M4
Capacitor	MOMCAP ?

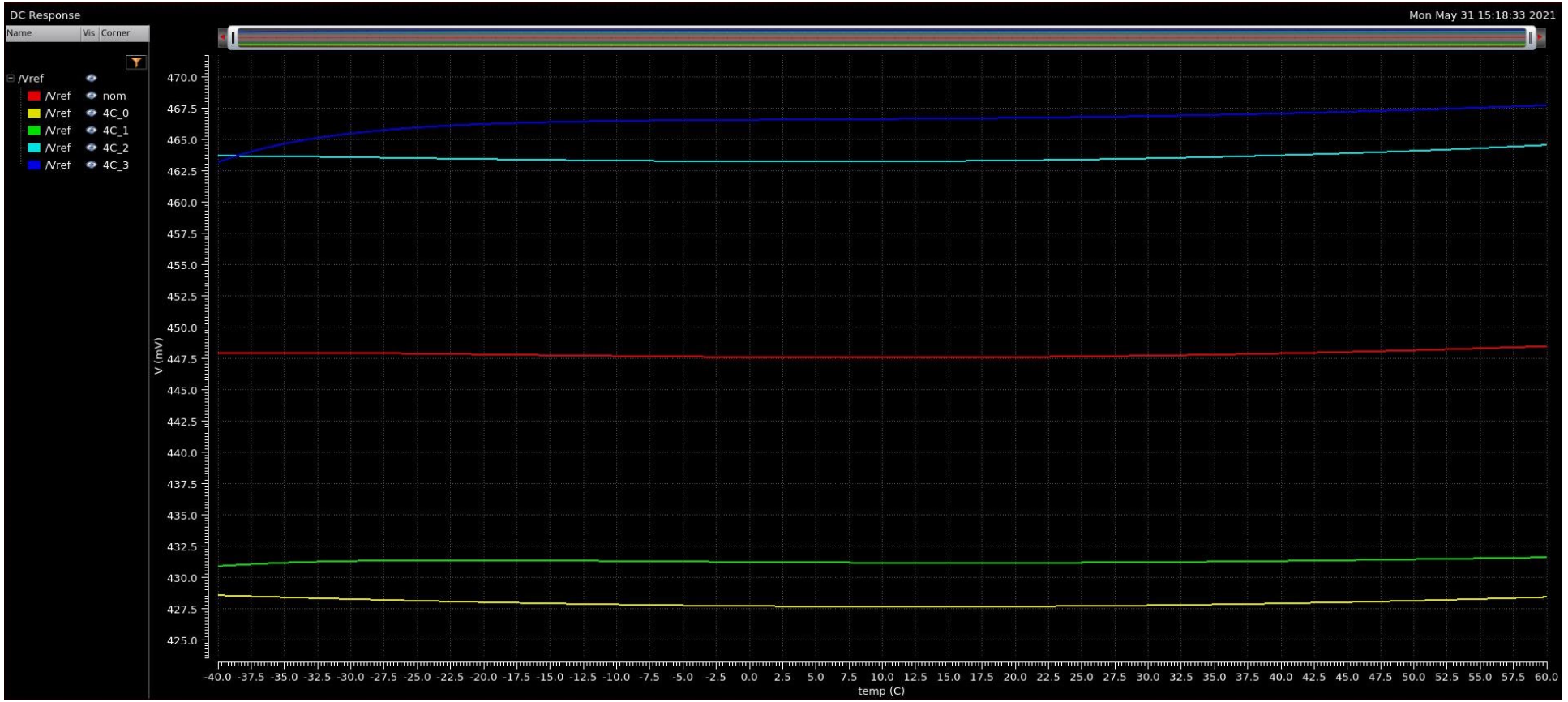


BGR - Schematic

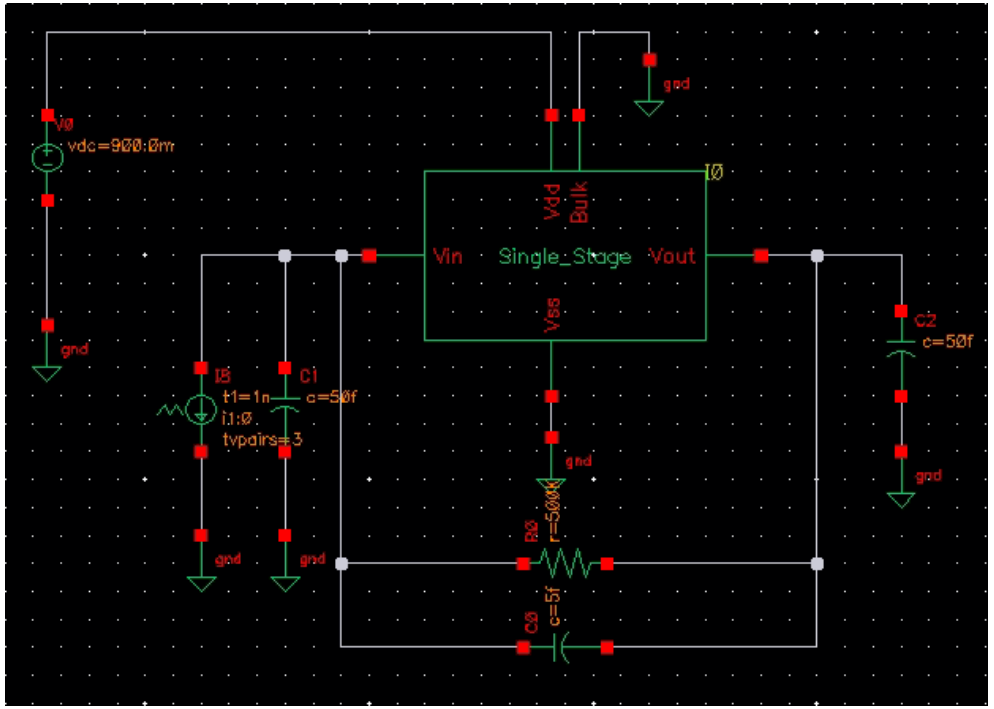


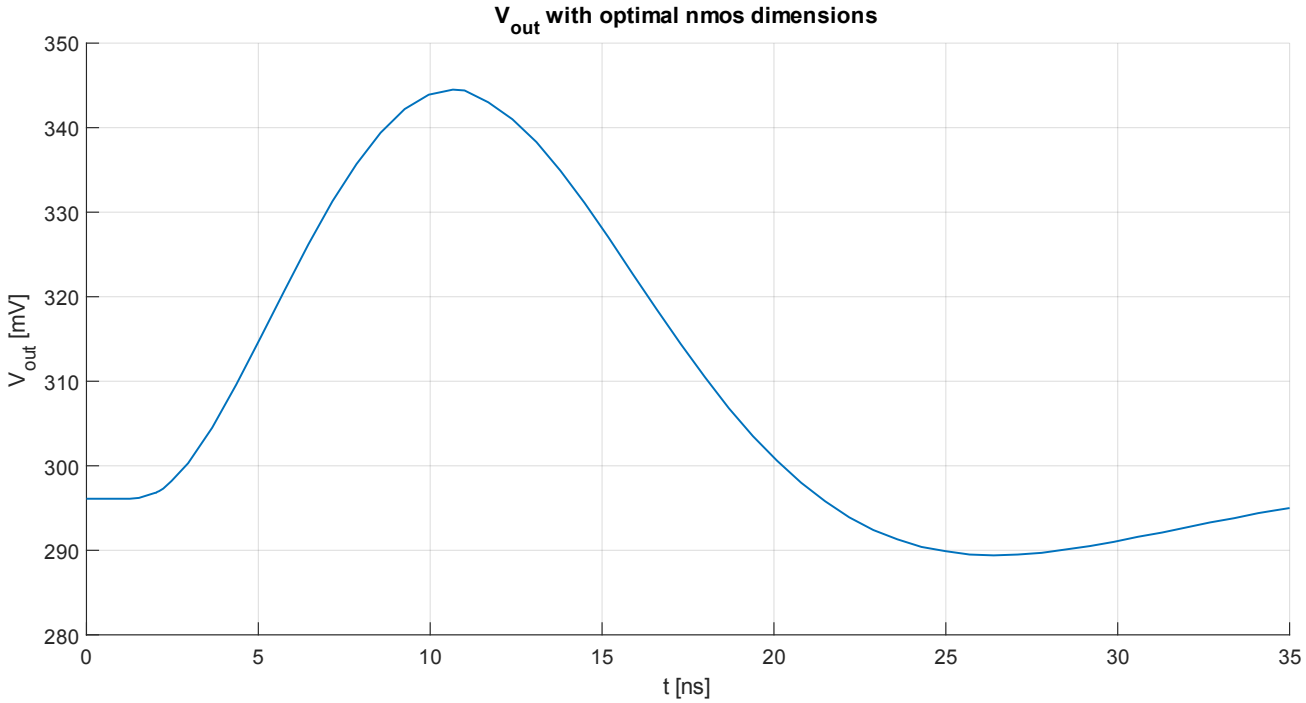
Simulation in tt and four corners

Corner	toplevel.scs
nom	top_tt
4C_0	top_ff
4C_1	top_fs
4C_2	top_sf
4C_3	top_ss



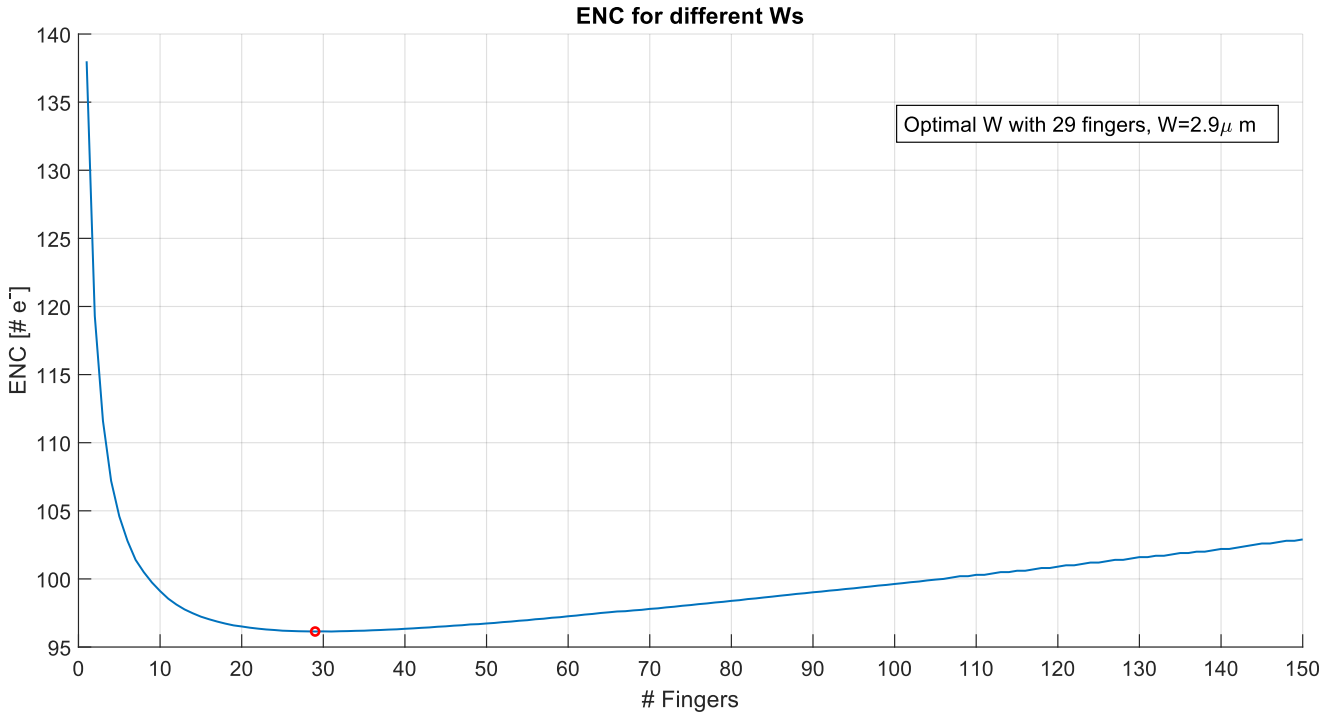
Single Stage Preamplifier





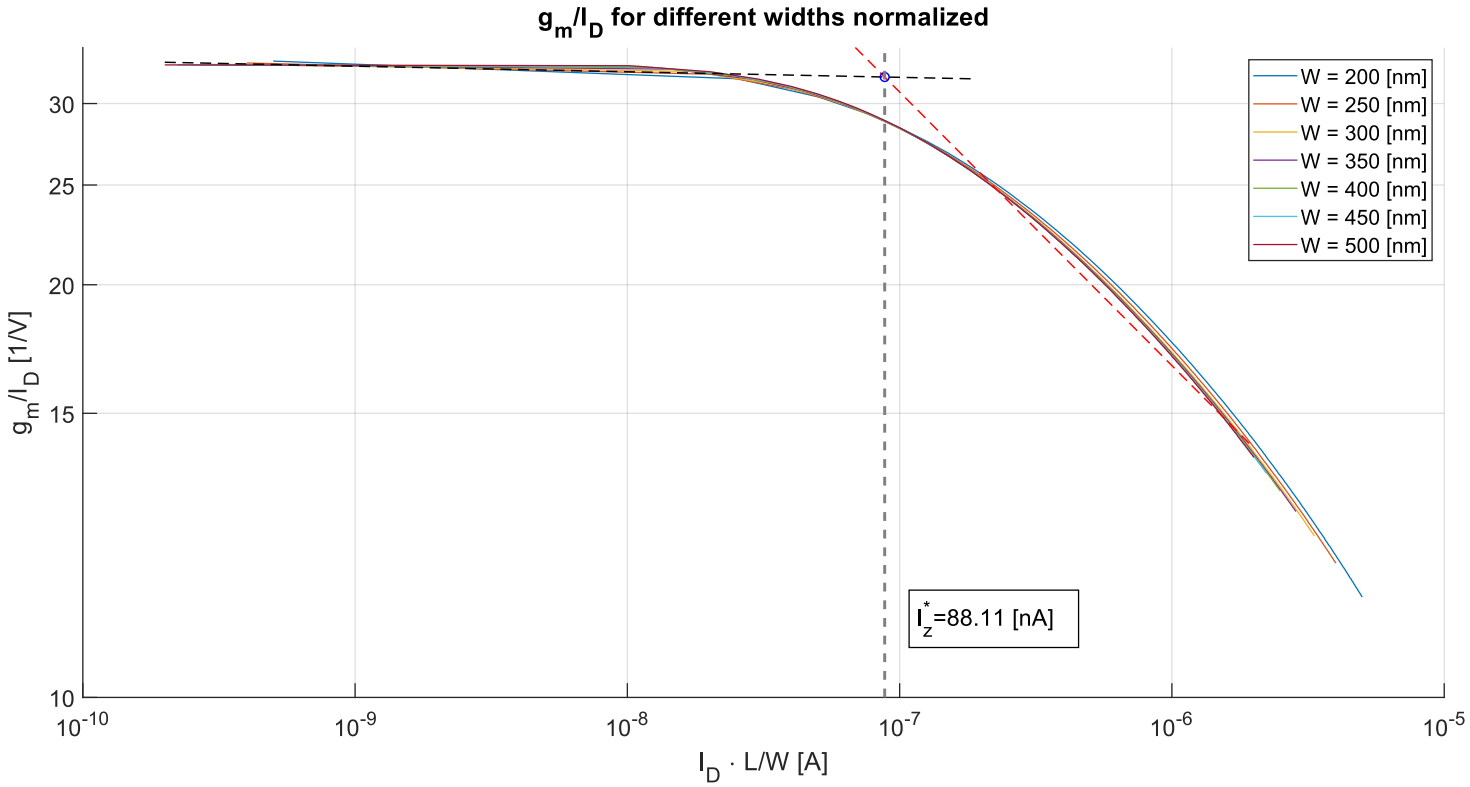
- Primo step del preamplificatore di carica
- Risposta in transitorio per una carica pari a $6000\ e^-$

ENC and Optimal W



- $ENC = \frac{\left(\frac{\sqrt{\overline{noise}}}{V_{max}-V_{min}}\right)}{Q_{inj}}[e^-]$
- Il valore di W ottimo che si ottiene è pari a $2.9\mu m$
- Con W ottima e L minima ($100\ nm$) si ottiene un ENC di circa $96\ e^-$, ottenendo un rapporto, rispetto alla carica inietta di $6000\ e^-$, pari al 98.4%
- Tempo di picco pari a $6.842ns$, discosta dell'ottimo di $0.338ns$
- Gain $31.71\ dB$, discosta dall'ottimo di $0.01dB$

Transconductance efficiency



- Rapporto $\frac{g_m}{I_D}$ valutato per differenti W
- La I_Z^* che si ottiene interpolando i due tratti della curva come rette è pari a $88.11\ nA$