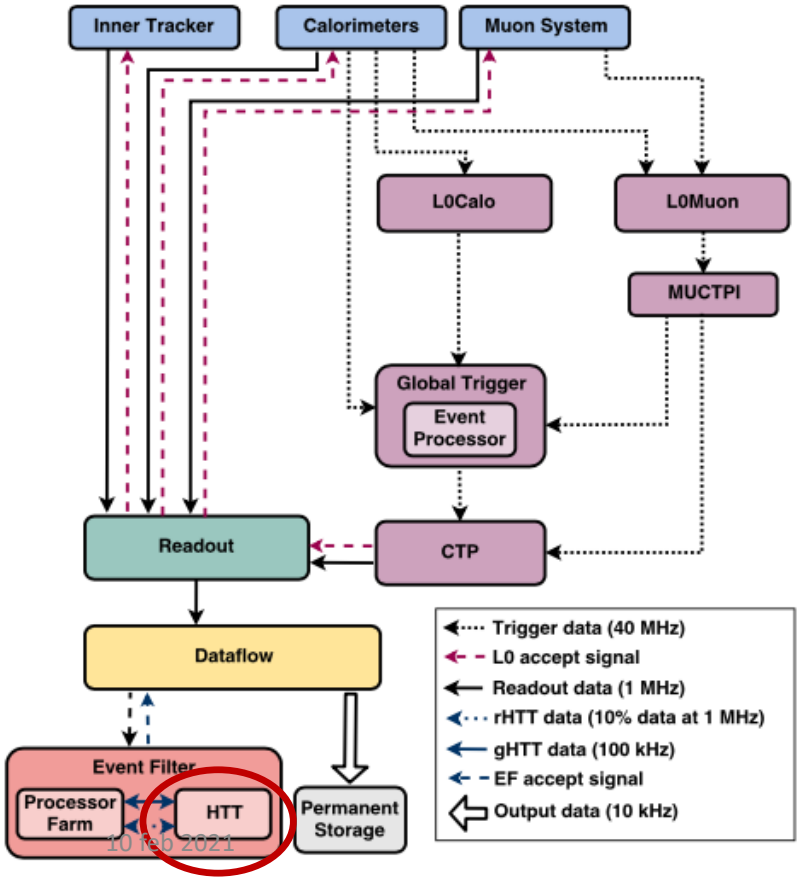
Aggiornamenti sulla scelta per EF tracking

Alberto Annovi

Pisa

Status at the time of TDR

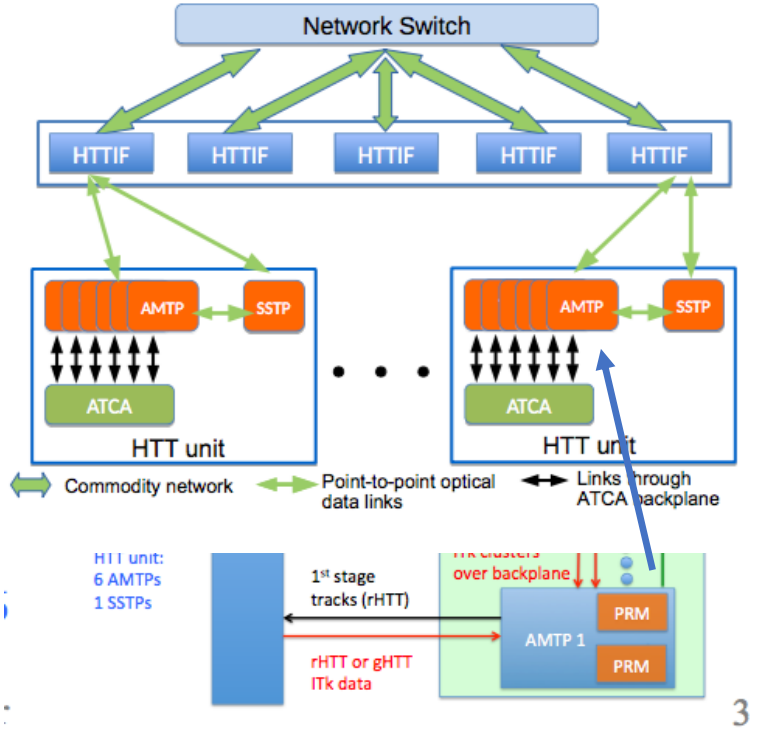


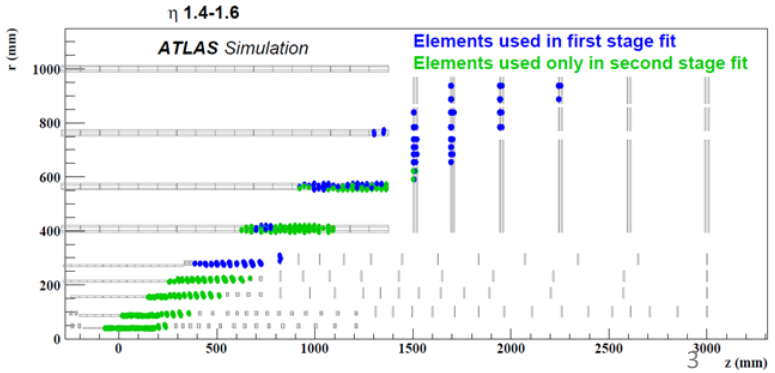
- HTT provides regional and global tracking to the Event Filter Farm
- HTT is an array of ATCA modules based on FPGAs and AM ASICs

Hardware Track Trigger

- A single system that performs both regional and global tracking
  - regional: 10% of ITk data at 1MHz (p_T>2GeV)
  - global: full events at 100kHz (p_T>1GeV)
- 1st stage processing (AMTP)
  - AM pattern matching + track fitting using 8 ITk layers
  - Essential part of L1Track as well
- 2nd stage processing (SSTP)
  - Extrapolation to inner layers

- Italian core for PRM and AM ASIC
- Italian activities for AM ASIC, PRM, SW, Hough Transform
- The study of pattern recognition with Hough Transform started as a back up plan for the Associative Memory ASIC.





EF tracking choice

- Three technologies being compared
- Custom HW (HTT like with a single ATCA card flavor)
  - Full processing (complete tracking)
  - Two pattern recognition options
    - AM ASIC
    - or Hough Transform on FPGA
- Commodity
  - FPGA accelerator based on Hough Transform
- SW Tracking
  - HLT optimized version of ITk tracking
  - Current estimates with CPU only
  - Past evaluation of GPU not competitive, to be repeated later on

Next steps

- Review process on going
- Last update at Upgrade week
- Reports being delivered in May
- Review reccomendation to eTDGS by the end of May
- Expect an open meeting in the first half of June (TBC)
- eTDSG choice mid June (date being decided)

Preliminary system cost

SW only

Cost of tracking

- Software tracking worth ~3.5 MCHF
- Care needs to be taken when comparing this value to other task forces
  - e.g. CPU resources required to turn “hardware tracks” into “software tracks”, refit, etc.

	Run-4 (2027)	Run-5 (2032)	Total Run-4&5
Compute cost [CHF/HS06]	1.0	0.5	
Cost range [CHF/HS06]	[0.7–1.3]	[0.2–0.8]	
Cost Tracking [MCHF]	2.67	+0.87	3.54 [2.22–4.86]
Cost Other reco. [MCHF]	1.86	+0.21	2.07 [1.38–2.75]
Cost Total [MCHF]	4.53	+1.07	5.60 [3.60–7.60]

Spending profile

- Actual cost is significantly smaller
- “Incoming” Run-3 farm already provides 2.85 MHS06
- ~2.8 MCHF for total farm (tracking+other)
  - 2/3 of which could be attributed to tracking alone (~1.9 MCHF)

	CPU [MHS06]	Extension cost [MCHF]
Run-3 farm	2.85	n/a
Run-4 required	4.53	1.68
Run-5 required	6.67	1.07
Total Run 4+5 (+3% for services)		**2.83 [1.65–4.01]**

Estimated System Size

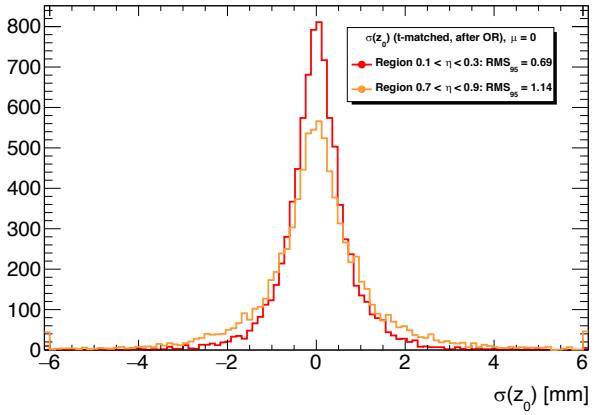
	Firmware Implementations		
Per Event	**ANL**	**Bologna/ Uppsala**	**Penn/UCI**
Loading Time (ms)	4.3	5.1	~0.8
Readout Time (ms)	3.4	2.5	~1.3
Total Time (ms)	**7.7**	**5.1**	**~1.3**
	(sum)	**max(loading, readout)**	
Processing Rate (Hz)	**129**	**195**	**500-750**

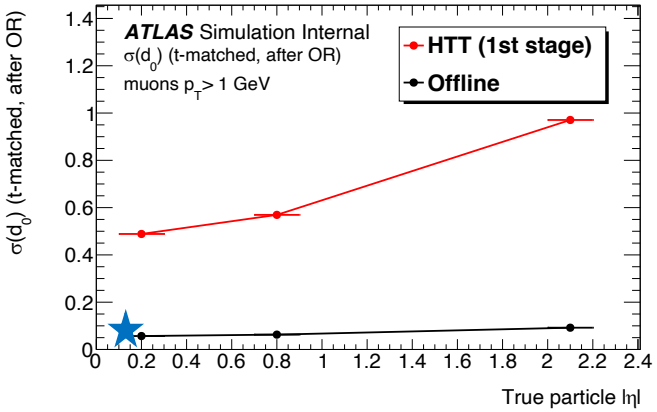
Event Filter Tracking Rate (kHz)	150	150	150
#Accelerators	**1,161**	**769**	**200-300**

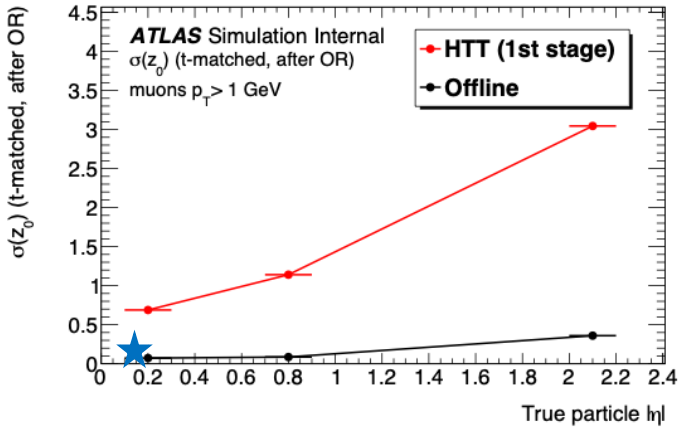
FIRST STAGE TRACKING RESOLUTIONS

F. Pastore
HTTSim group

Custom TF







★ Resolutions with all layers (2nd stage) see next slide

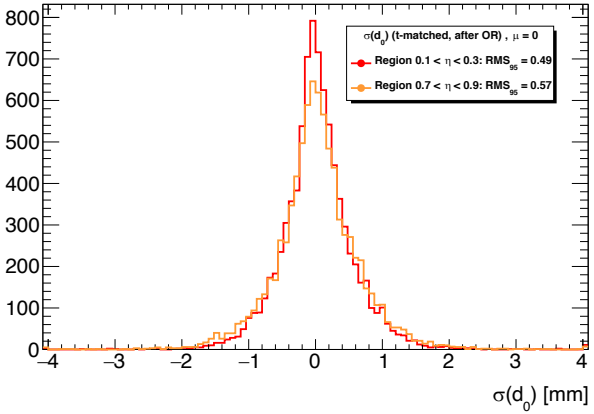


Table 4: First-stage track fitting resolutions ($rms_{95\%}$) for muons ($p_T > 1$ GeV)

muons, $p_T > 1$ Gev, no PU, RMS95						
η range	Conf	η	ϕ	q/p_T $[^{-1}]$	d_0 [mm]	z_0 [mm]
$0.1 < \eta < 0.3$	Base 2WC	0.0030	0.0027	0.0064	0.49	0.69
$0.7 < \eta < 0.9$	Base 2WC	0.0035	0.0031	0.0075	0.57	1.14
$2.0 < \eta < 2.2$	Base 2WC	0.0068	0.0062	0.0317	0.97	3.04

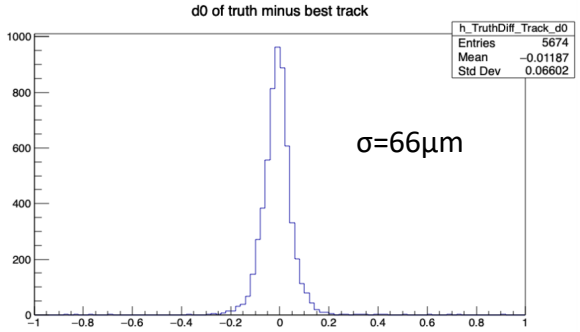
Table 5: Efficiency and counts with single muons ($p_T > 1$ GeV) + PU200

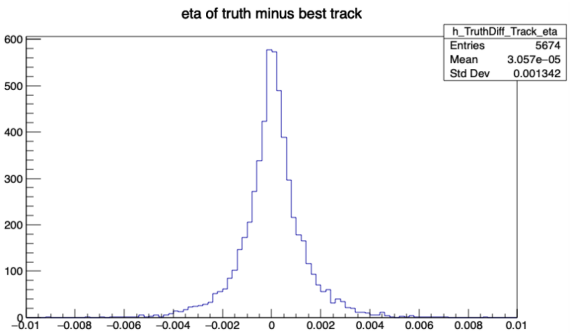
η range	Conf	efficiency%	# roads	# tracks OVR	# fit constan
$0.1 < \eta < 0.3$	Base ttbar	100	151	8.4	8.1
$0.1 < \eta < 0.3$	Base mu+PU	100	149.0	8.3	7.9
$0.7 < \eta < 0.9$	Base mu+PU	100	84.7	5.9	5.7

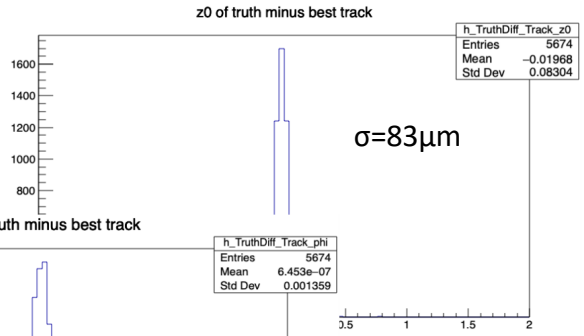
Preliminary performance from HTTSim with AM simulation.
Same performance expected if using Hough Transform, since resolutions are driven by the fitting stage.

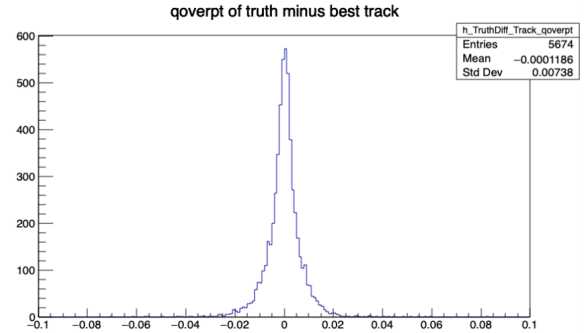
SECOND STAGE TRACKING RESOLUTIONS

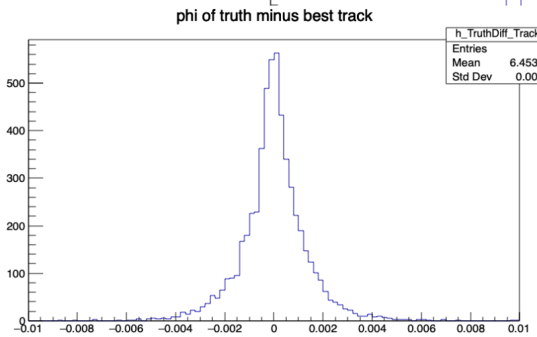
F. Pastore
HTTSim group











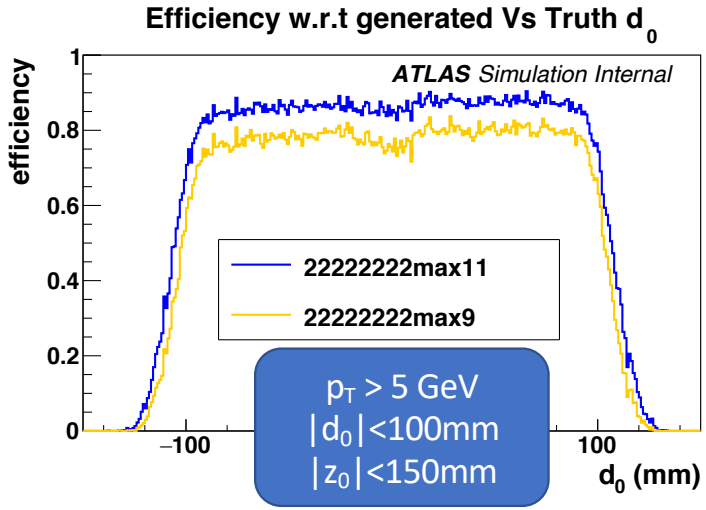
Preliminary second stage performance for the 0.1-0.3 η region from HTTSim with AM simulation.

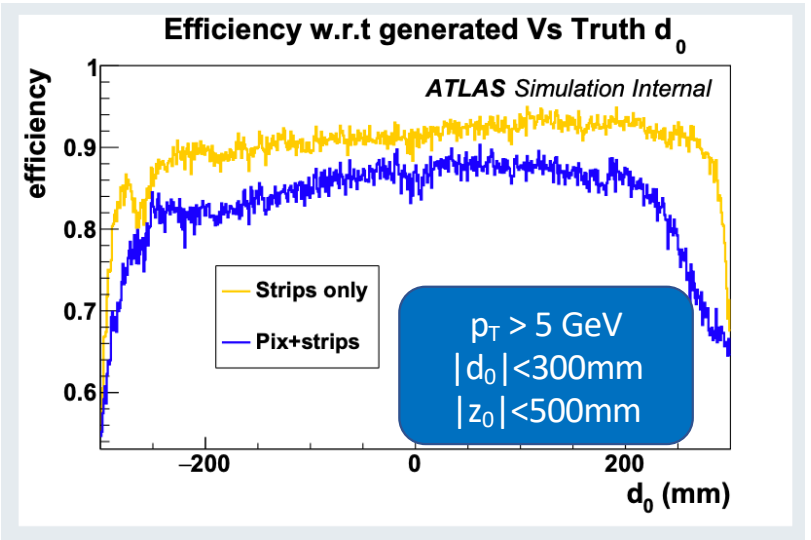
Same performance expected if using Hough Transform, since resolutions are driven by the fitting stage.

LRT pattern matching WITH AM ASIC

Custom TF

- AM approach for LRT uses dedicated LRT patterns.
- The required number of patterns has been tuned for the 4 working points (previus slide).
  - Enough pattern to control the downstream processing rate
- Previous slide reports the additional shelves required for each working point.
- Once the system size is chosen SRT and LRT will be performed by a single system and there is flexibility to change the resource allocation.





- Given the limited time for the studies, we expect significant room for future improvement.
- The strip only configuration is preferred for larger d0
- These results use special single muon samples for region 0.1-0.3 η, 0.3-0.5 φ0

FOCUS ON PATTERN RECOGNITION OPTIONS

- A single-type custom-built ATCA card will host FPGAs to perform all tracking algorithms, with the possible exception of the pattern recognition stage.
- In either case, the pattern recognition will be followed by a 1st-stage tracking (using 8 ITk layers). In either case, this system will provide full 13-layer tracks from a 2nd-stage fitting.
- We have investigated two options for pattern recognition
  - AM ASIC
  - Hough Transform on FPGA (on a custom ATCA blade)
- According to the mandate, we should present a single option
- We think that it is important to include the reviewers opinion in the decision in order to have broad inputs and make a choice in the best interest of all involved stake holders
- Next slides compare the system level implications of the two choices
- Dedicated review meeting on Tuesday.
  - Comparison of AM ASIC and Hough Transform in slides

SYSTEM SIZE

P. Mastrandrea

- Require the same performance for both systems
- AM system size 10 shelves
- HT system size 20 shelves
- The system size is driven by 1st stage track fitting, i.e. the amount of fake candidates after the AM or HT filtering
- Core costs corresponding to the two options are in later slides.
- Hough Transform system size assumes the most mature of the available implementations

Table 2.4: HTT SRT processing rates for AM-based and HT-based systems.

System parameters			SRT	
Name	Unit	Available Resources	TFB	Hough Transform
ATCA shelves	#		10	20
FPGA's	#		280	560(+280)
Peak cluster rate/ layer	MHz	250	105	
Average cluster rate/ layer	MHz	100	82	
Roads rate / FPGA (DO or H.T. output)	MHz	500	302	127
Roads rate / FPGA (Track Distributor)	MHz	312	302	127
Constants readout (chi2) Rate / FPGA	MHz	160	157	66
Fit rate (chi2) / FPGA	MHz	1502	1441	1360
Core costs (MCHF):			5.4	7.2

TFB is the Task Force baseline tracking:
100 kHz global + 1 MHz 5% regional

Conclusioni

- L’attività di studio delle 3 opzioni e di documentazione è nella fase finale
- Nell’ambito della custom task force a breve sceglieremo fra AM ASIC e Hough Transfrom tenendo conto del feedback dei reviewers
- La decisione principale fra le 3 opzioni è prevista intorno a metà giugno
  - La scelta avrà un impatto importante sulle attività italiane

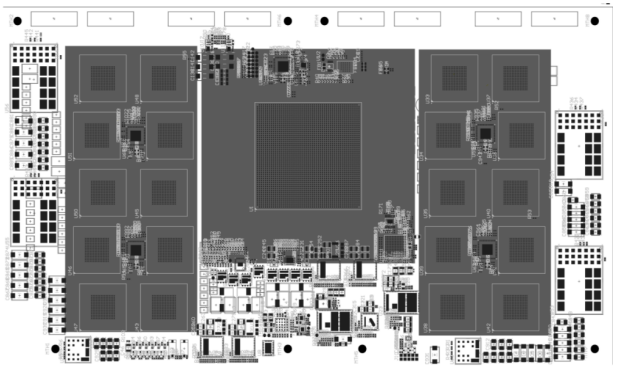
Status at the time of TDR

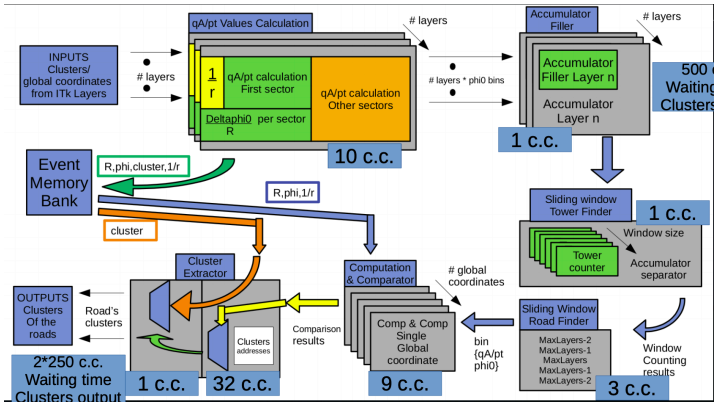
- CPU tracking cost estimated at 80 MCHF
  - 40 MHS06 with a forecast of 2 CHF/HS06 in 2026
- HTT system core cost 17.4 MCHF
  - based on 48 ATCA shelves
- One of the motivation of the HTT system was the TDAQ evolution to a dual level trigger
  - Difficulties in implemented the detector readout described in the TDRs eventually lead to a decision to have a L0 only system without evolution (2020)

HTT (BO, GE, MI, PI, PV)

Attività in corso con forte contributo italiano (coordinatori):

- PRM (Paolo Francavilla)
  - PCB in arrivo a Febbraio
  - Sviluppo firmware per l'FPGA di controllo
  - Il FW con la funzionalità di tracking è assemblato e in fase di debug
- AM ASIC (Tommaso Lari)
  - Disegno AM08 a 28nm sottomesso!
  - E' emersa un carenza di personale rispetto agli obiettivi, che è diventa molto critica con l'inizio del periodo covid. Il personale coinvolto in FTE è raddoppiato e dovrebbe aumentare nei prossimi mesi.
- SW (Andrea Negri)
  - Prima versione del framework per il software online messo a disposizione
- FW (Alessandro Gabrielli)
  - Firmware per Hough Transform in stato avanzato e trainante. Attività compatibile con due scenari futuri: custom HW e commercial FPGA.
  - Sviluppo del framework di continuous integration
- Integration (Paolo Mastrandrea)
  - Preparazione del setup dell'integrazione: HW, SW e procedure





HTT system optimization in 2020

- Taking advantage of the L0-only context, of developments since TDR, and more mature estimates of algorithm performances the HTT system has been optimized in 2020

- Baseline HTT core cost 17.4 MCHF at TDR
- HTT L0 optimized system with 24 shelves provide
  - mu200 HTT processing with current best estimate rates (CBE)
  - 20 AM ASICs + 2 FPGAs / board (336 cards in 24 shelves) core cost 9.8 MCHF
  - Consider cost increase to 32 shelves as uncertainty +2.2 MCHF
- The new HTT system reduces the core cost from 17.4 MCHF to 12 MCHF (including uncertainty and margin), or 9.8MCHF for current best estimates