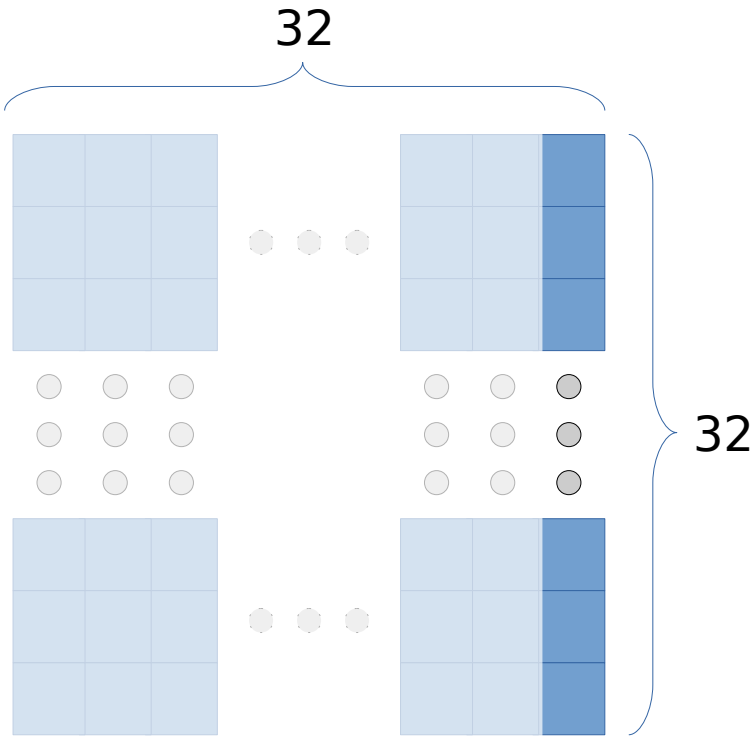
# TIIMM0 digital part analysis

Luca Federici (INFN – LNF)
27/04/2021

# Outline

TIIMM0 32 pixels column digital logic:

- Command Decoder:
  - FSM;
  - FSM’s states description
- Row Select;
- StrongPixelReader (Column):
  - Single Pixel Architecture:
    - Mask logic;
    - Pulse logic;
    - Digital pulse;
    - Analog pulse;
    - Hit arrived;
    - TOTCounter;
    - DAC Latch.



# Architecture: Building Blocks

Command Decoder

Set up the operation of the chip:
- program the DAC;
- mask a pixel;
- choose a pixel for test injection;
- etc.

RowSelect

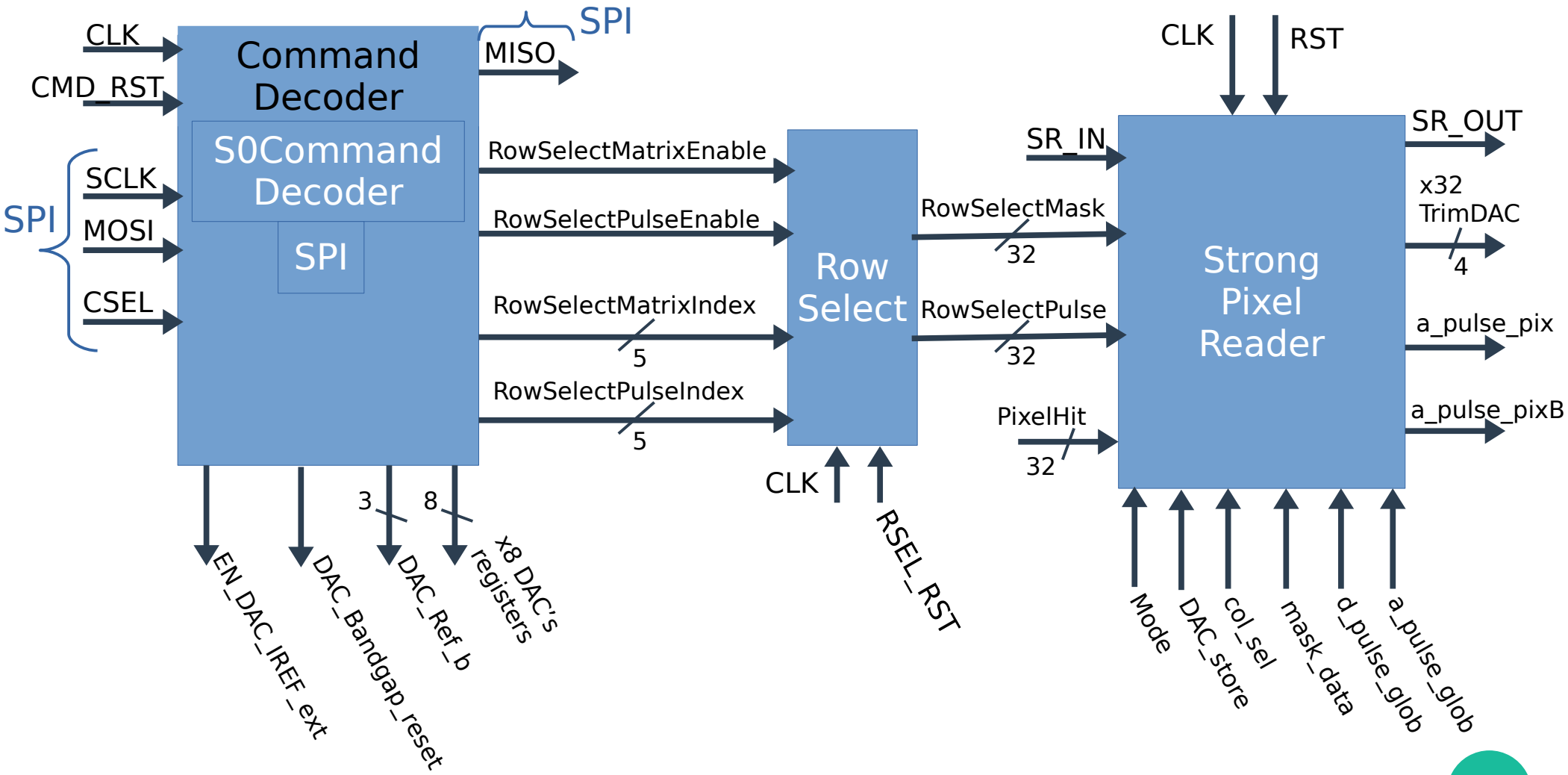
Used for:
- masking;
- injection

Separated from CommandDecoder because on side of the matrix

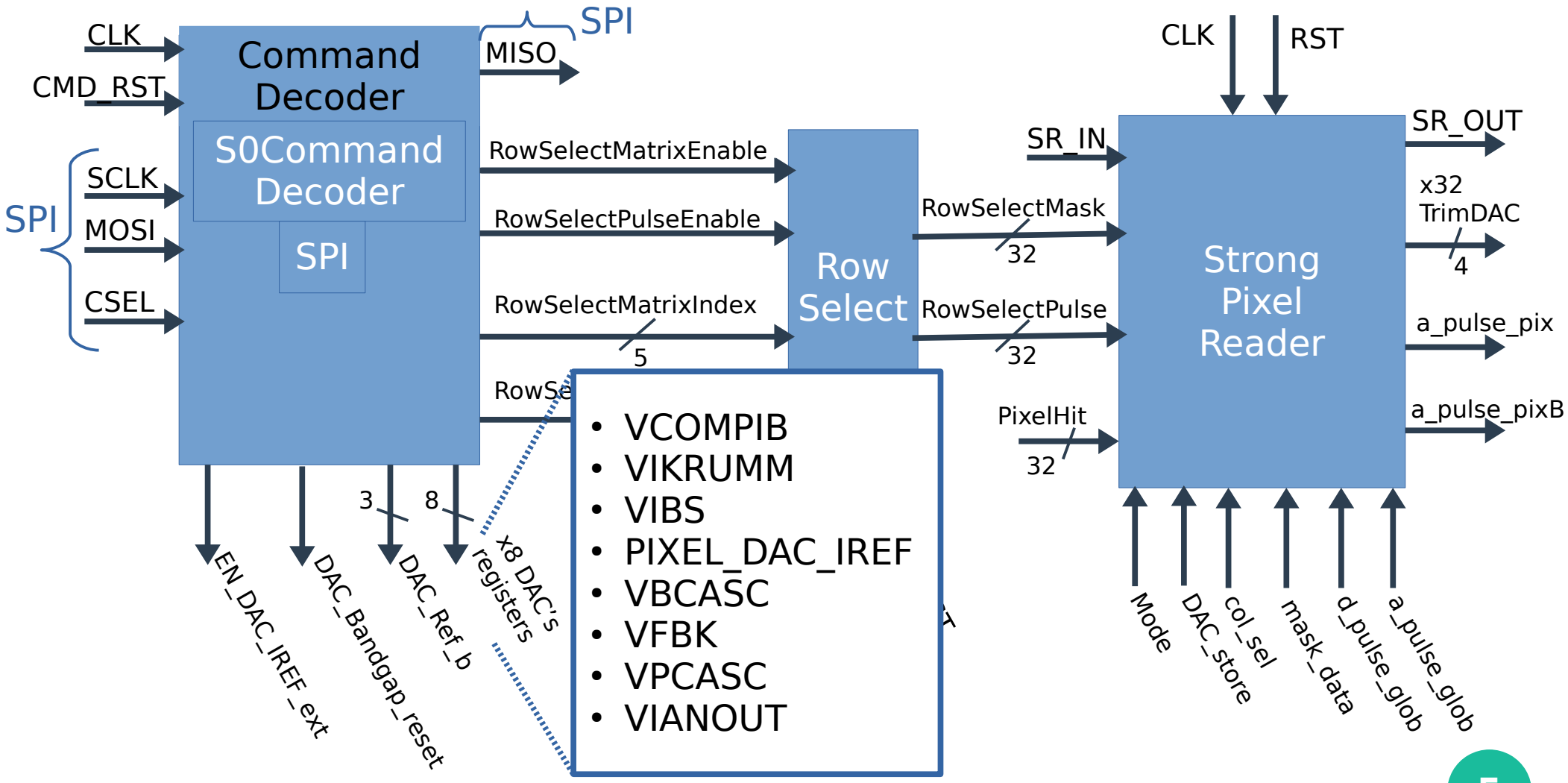
Strong Pixel Reader

Setting the in-pixel trimming DAC
- masking pixels
- counting the TOT of the pulse coming from the comparator

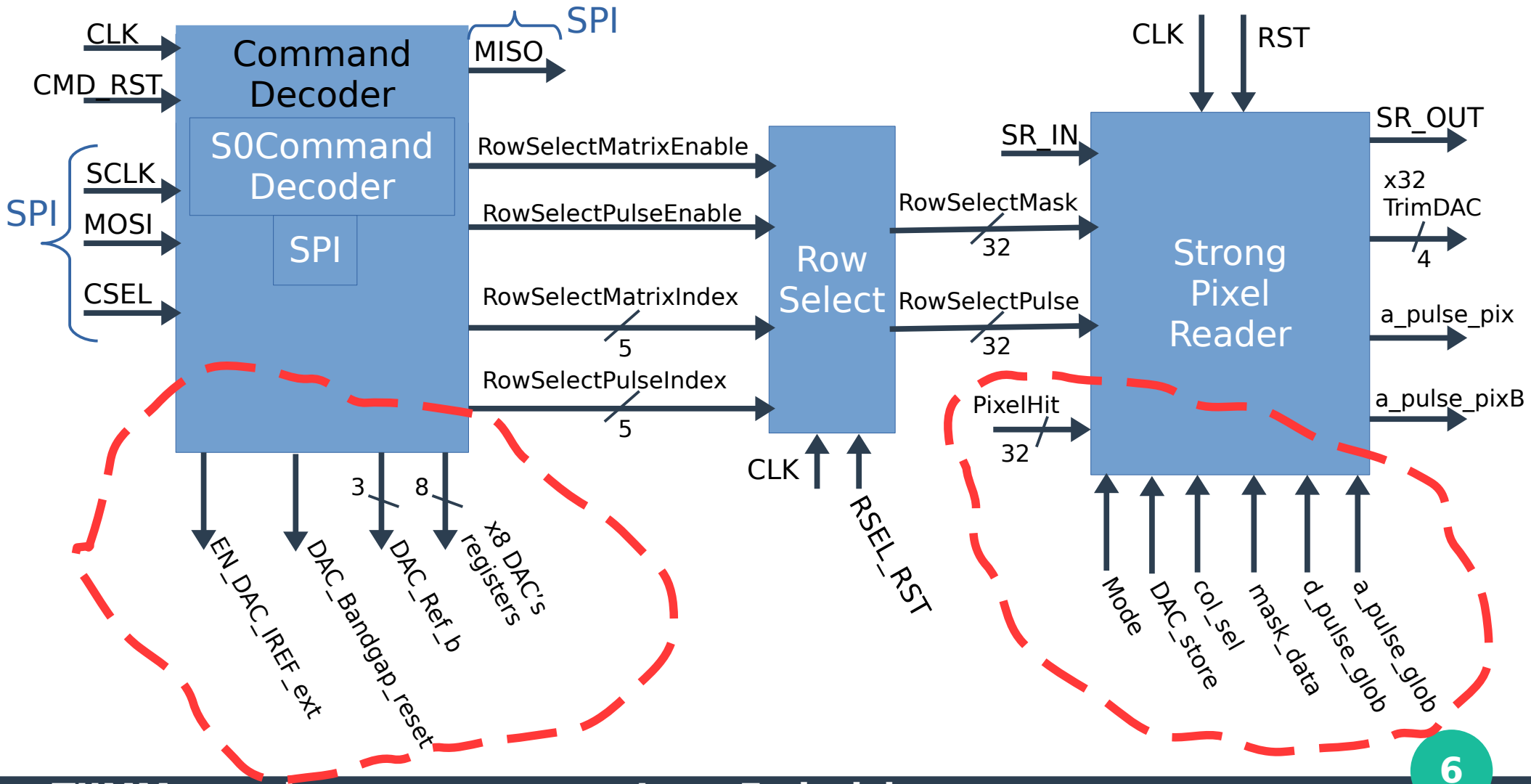
# Architecture: connections



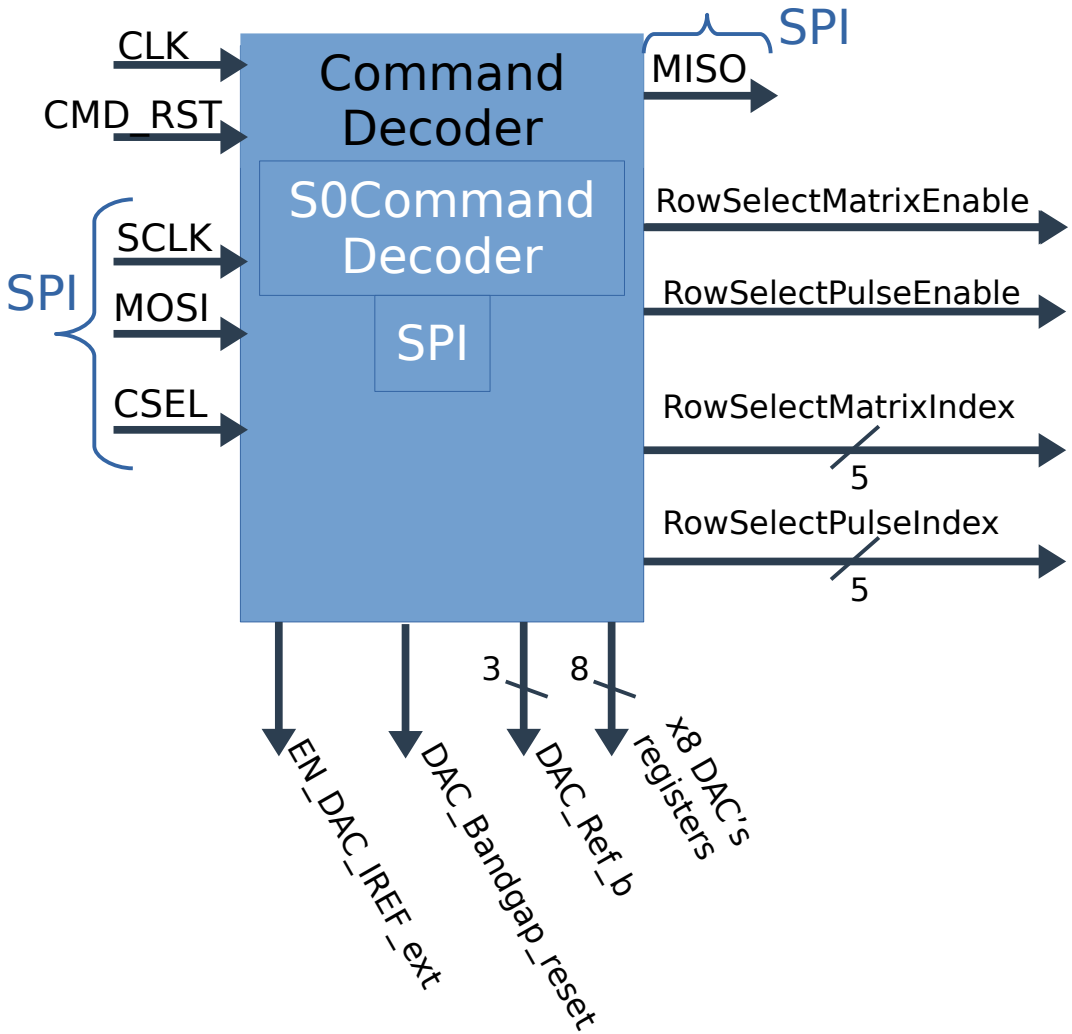
# Architecture: connections



# Architecture: connections



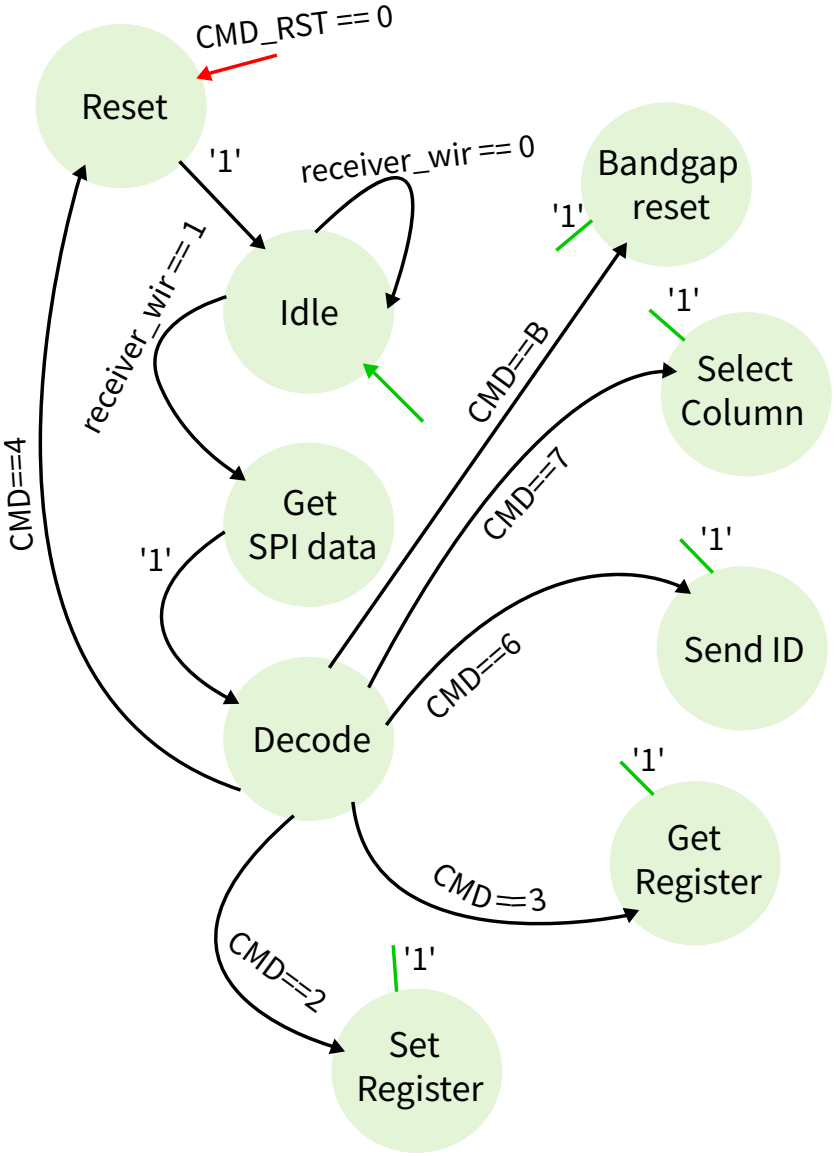
# Architecture: CommandDecoder




DAC's registers

- VCOMPIB
- VIKRUMM
- VIBS
- PIXEL_DAC_IREF
- VBCASC
- VFBK
- VPCASC
- VIANOUT

# Architecture: CommandDecoder Finite State Machine




| CMD [0x] | Destination state |
|---|---|
| 2 | SET_REGISTER |
| 3 | GET_REGISTER |
| 4 | RESET |
| 6 | SEND_ID |
| 7 | SEL_COLUMN |
| B | BANDGAP_RESET |
| Otherwise | IDLE |

# Architecture: CommandDecoder FSM's states

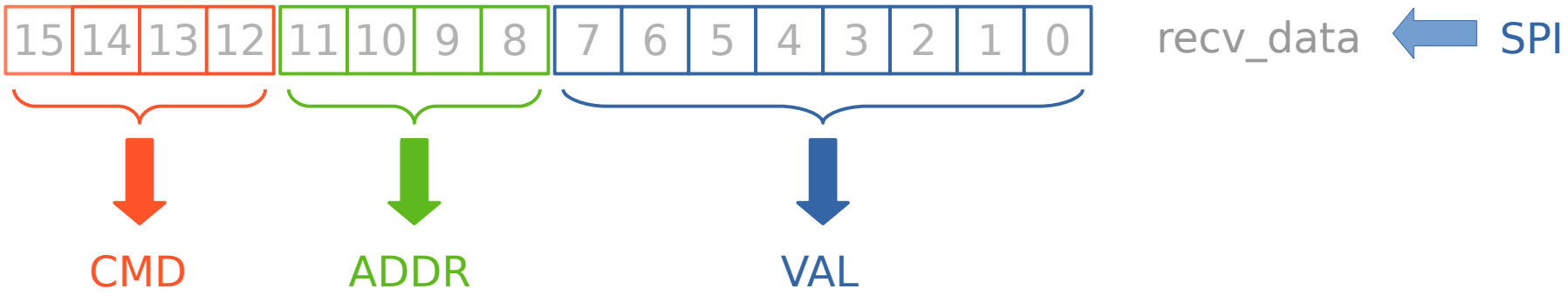
CMD_RST == 0


| Signal | Def. Value [0x] |
|---|---|
| CMD | 0 |
| ADDR | 0 |
| VAL | 0 |
| send_data | 0 |
| VCOMPIB | 5C (5μA) |
| VIKRUMM | 5C (5μA) |
| VIBS | 5C (5μA) |
| PIXEL_DAC_IREF | 5C (5μA) |
| VBCASC | 5C (5μA) |
| VFBK | 5C (5μA) |

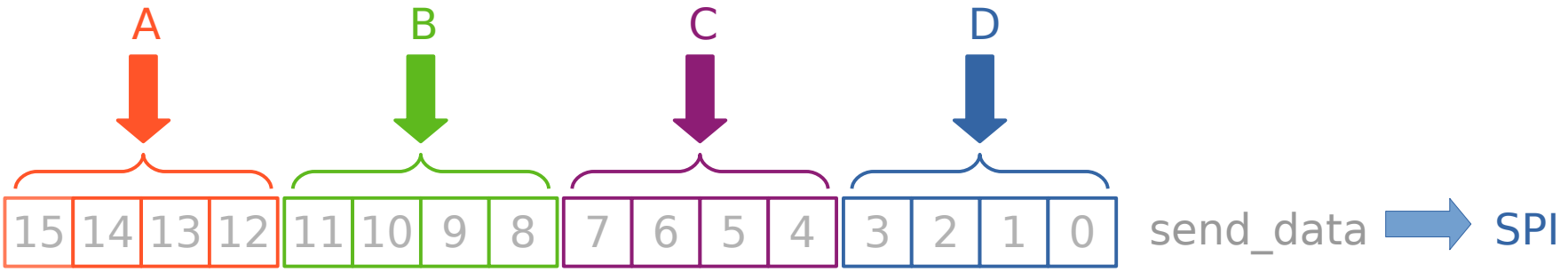
| Signal | Def. Value [0x] |
|---|---|
| VPCASC | 5C (5μA) |
| VIANOUT | 5C (5μA) |
| SelectColumnIndex | 0 |
| SelectColumnEnable | 0 |
| DAC_Bandgap_reset | 1 |
| DAC_Ref_b | 0 |
| EN_DAC_IREF_ext | 0 |
| RowSelectMaskIndex | 0 |
| RowSelectPulseIndex | 0 |
| RowSelectMaskEnable | 0 |
| RowSelectPulseEnable | 0 |
| TestReg0 | F1 |
| TestReg1 | E2 |

# Architecture: CommandDecoder FSM's states

state == GET_SPIDATA

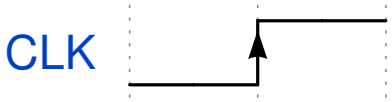




state == SEND_ID

# Architecture: CommandDecoder FSM's states

state == SET_REGISTER

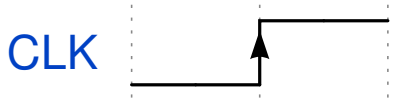



| ADDR [0x] | Instruction |
|---|---|
| 1 | VCOMPIB <= VAL |
| 2 | VIKRUMM <= VAL |
| 3 | VIBS <= VAL |
| 4 | PIXEL_DAC_IREF <= VAL |
| 5 | VBCASC <= VAL |
| 6 | VFBK <= VAL |
| 7 | VPCASC <= VAL |
| 8 | DAC_Ref_b <= VAL[3:1]<br>EN_DAC_IREF_ext <=VAL[0] |

| ADDR [0x] | Instruction |
|---|---|
| 9 | TestReg0 <= VAL |
| A | TestReg1 <=VAL |
| B | VIANOUT <= VAL |
| C | RowSelectMaskIndex <= VAL[4:0] |
| D | RowSelectPulseIndex <= VAL[4:0] |
| E | RowSelectMaskEnable <= VAL[0] |
| F | RowSelectPulseEnable <= VAL[0] |

# Architecture: CommandDecoder FSM's states

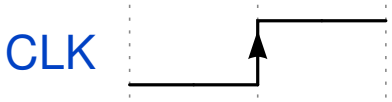
state == GET_REGISTER




| ADDR [0x] | Instruction |
|---|---|
| 0 | send_data <= CMD[3:0]+ADDR[3:0]+000+SelColumnEnable+SelectColumnIndex |
| 1 | send_data <= CMD[3:0]+ADDR[3:0]+VCOMPIB[7:0] |
| 2 | send_data <= CMD[3:0]+ADDR[3:0]+VIKRUMM[7:0] |
| 3 | send_data <= CMD[3:0]+ADDR[3:0]+VIBS[7:0] |
| 4 | send_data <= CMD[3:0]+ADDR[3:0]+PIXEL_DAC_REF[7:0] |
| 5 | send_data <= CMD[3:0] +ADDR[3:0]+VBCASC[7:0] |
| 6 | send_data <= CMD[3:0]+ADDR[3:0]+VFBK[7:0] |
| 7 | send_data <= CMD[3:0]+ADDR[3:0]+ VPCASC[7:0] |
| 8 | send_data<= 11b000+DAC_Ref_b+EN_DAC_IREF_ext+DAC_Bandagap_reset |

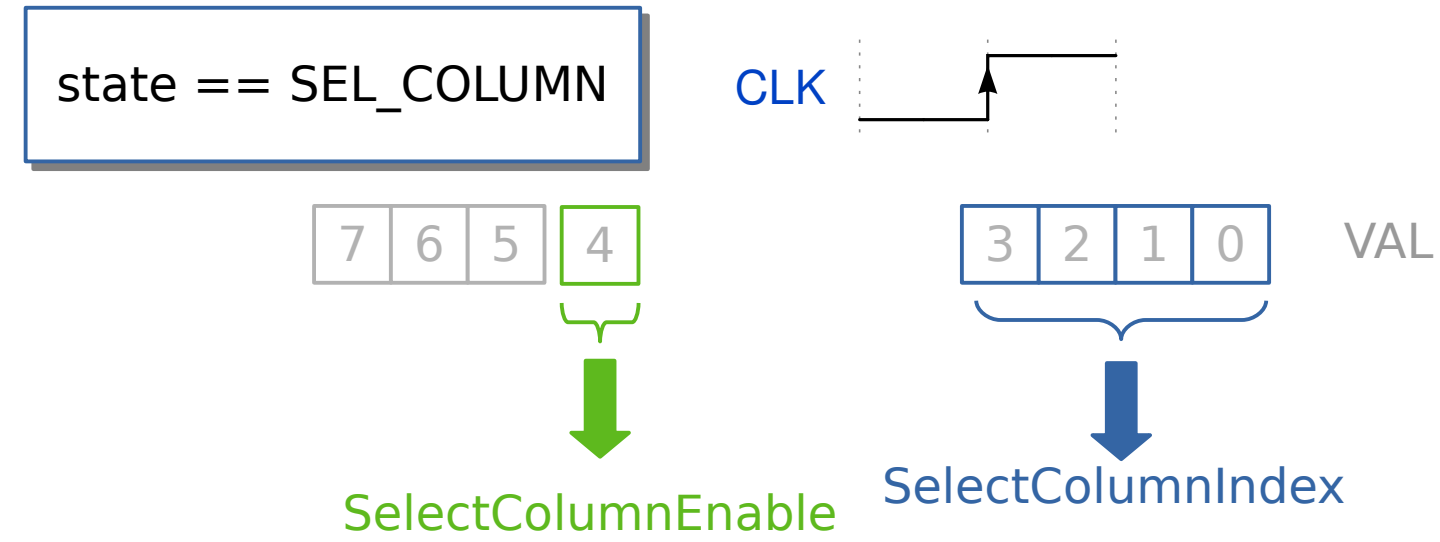
# Architecture: CommandDecoder FSM's states

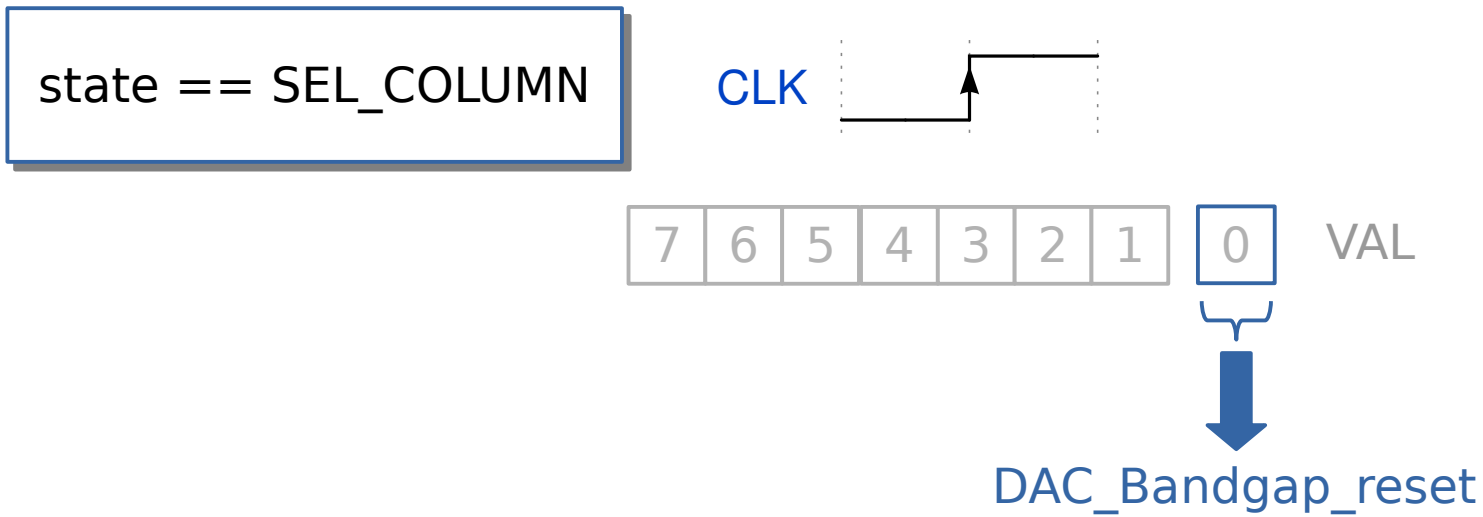
state == GET_REGISTER




| ADDR [0x] | Instruction |
|---|---|
| 9 | send_data <= CMD[3:0]+ADDR[3:0]+TestReg0[7:0] |
| A | send_data <= CMD[3:0]+ADDR[3:0]+TestReg1[7:0] |
| B | send_data <= CMD[3:0]+ADDR[3:0]+VIANOUT[7:0] |
| C | send_data <= CMD[3:0]+ADDR[3:0]+000+RowSelectMaskIndex |
| D | send_data <= CMD[3:0]+ADDR[3:0]+000+RowSelectPulseIndex |
| E | send_data<= CMD[3:0]+ADDR[3:0]+0000000+RowSelectMaskEnable |
| F | send_data<= CMD[3:0]+ADDR[3:0]+0000000+RowSelectPulseEnable |

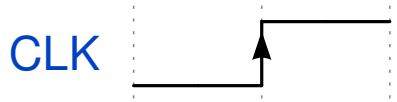
# Architecture: CommandDecoder FSM's states



# Architecture: CommandDecoder FSM's states

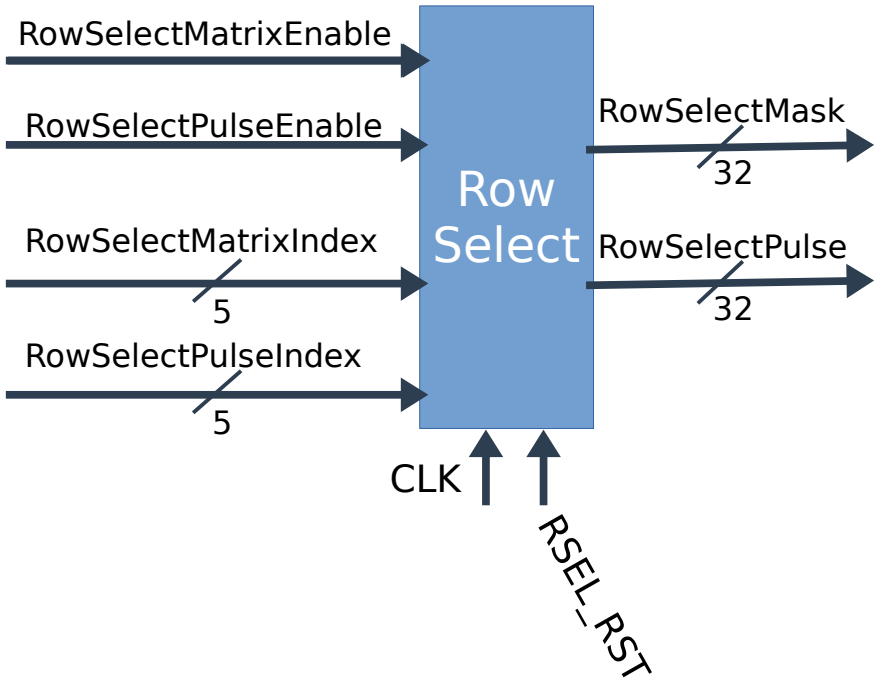
state == RESET




| Signal | Def. Value [0x] |
|---|---|
| VCOMPIB | 5C (5µA) |
| VIKRUMM | 5C (5µA) |
| VIBS | 5C (5µA) |
| PIXEL_DAC_IREF | 5C (5µA) |
| VBCASC | 5C (5µA) |
| VFBAK | 5C (5µA) |
| VPCASC | 5C (5µA) |
| VIANOUT | 5C (5µA) |
| send_data | 0 |

| Signal | Def. Value [0x] |
|---|---|
| SelectColumnIndex | 0 |
| SelectColumnEnable | 0 |
| DAC_Bandgap_reset | 1 |
| DAC_Ref_b | 0 |
| EN_DAC_IREF_ext | 0 |
| RowSelectMaskIndex | 0 |
| RowSelectPulseIndex | 0 |
| RowSelectMaskEnable | 0 |
| RowSelectPulseEnable | 0 |
| TestReg0 | F1 |
| TestReg1 | E2 |

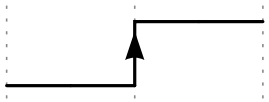
# Architecture: RowSelect



# Architecture: RowSelect

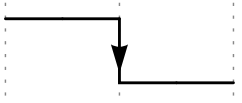
RSEL_RST == 0

CLK



or

RSEL_RST



‘0’

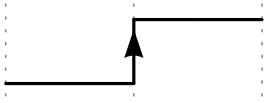
0 synch_RowSelectMaskEnable

‘0’

0 synch_RowSelectPulseEnable

RSEL_RST == 0

CLK



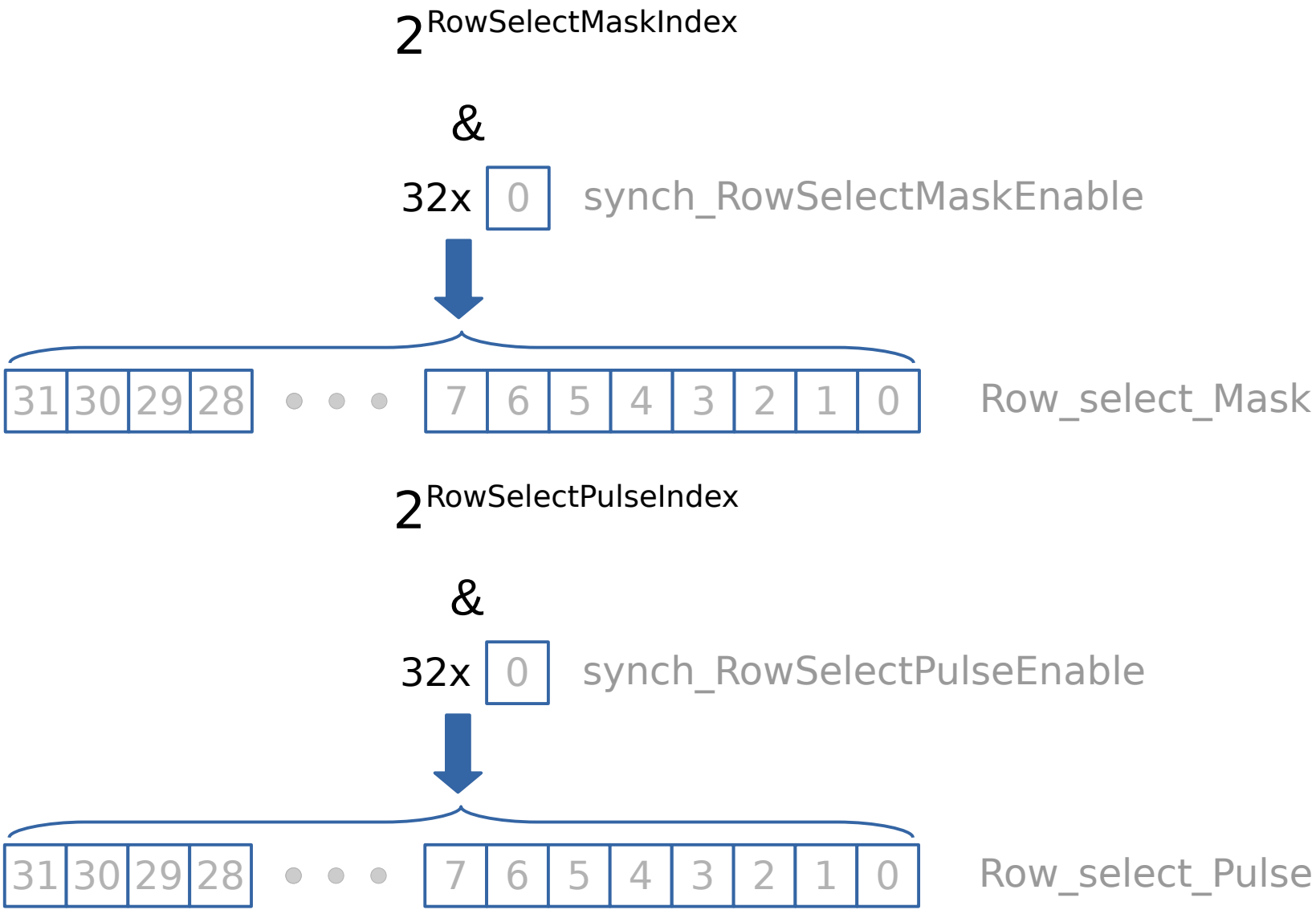
RowSelectMaskEnable

0 synch_RowSelectMaskEnable

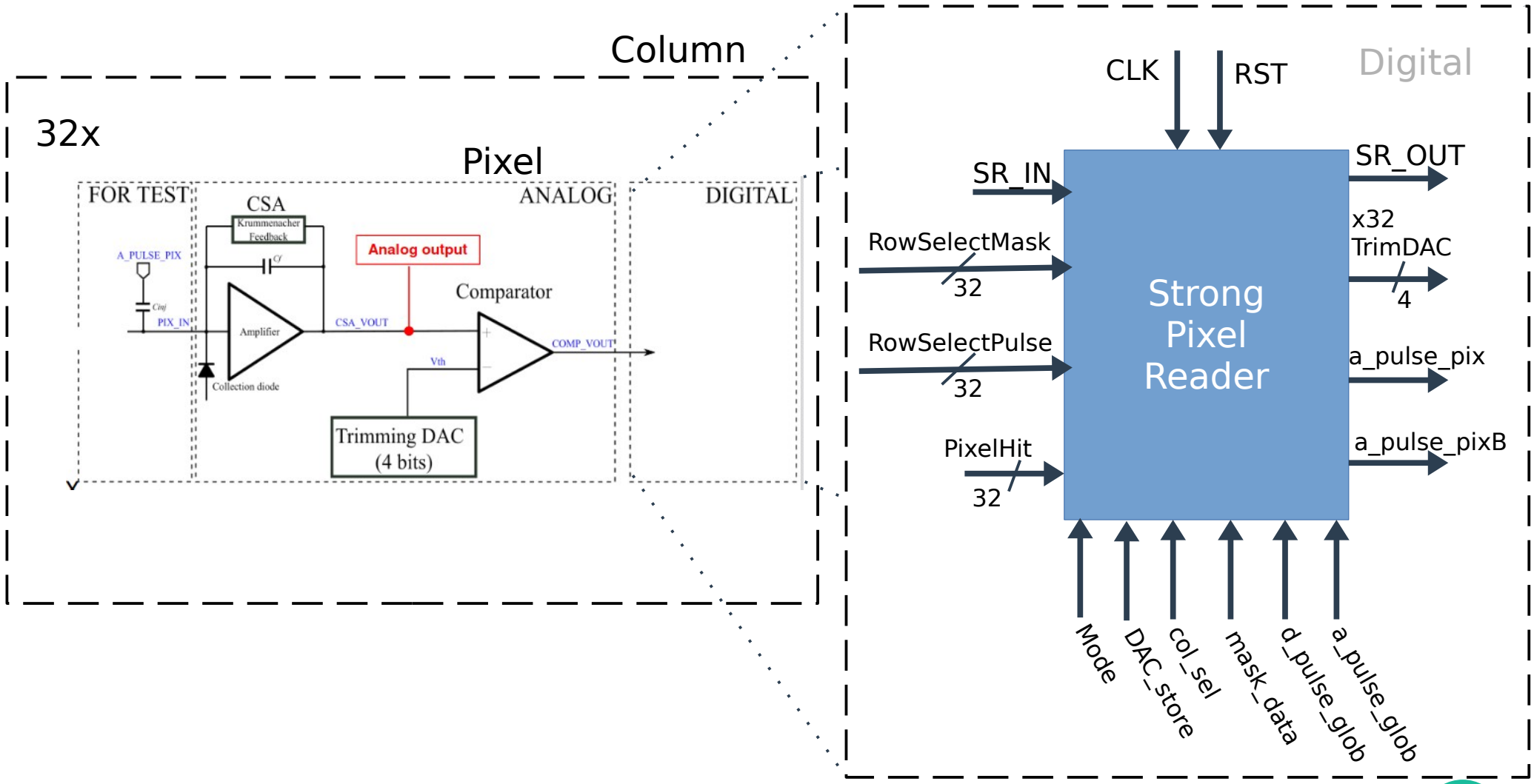
RowSelectPulseEnable

0 synch_RowSelectPulseEnable

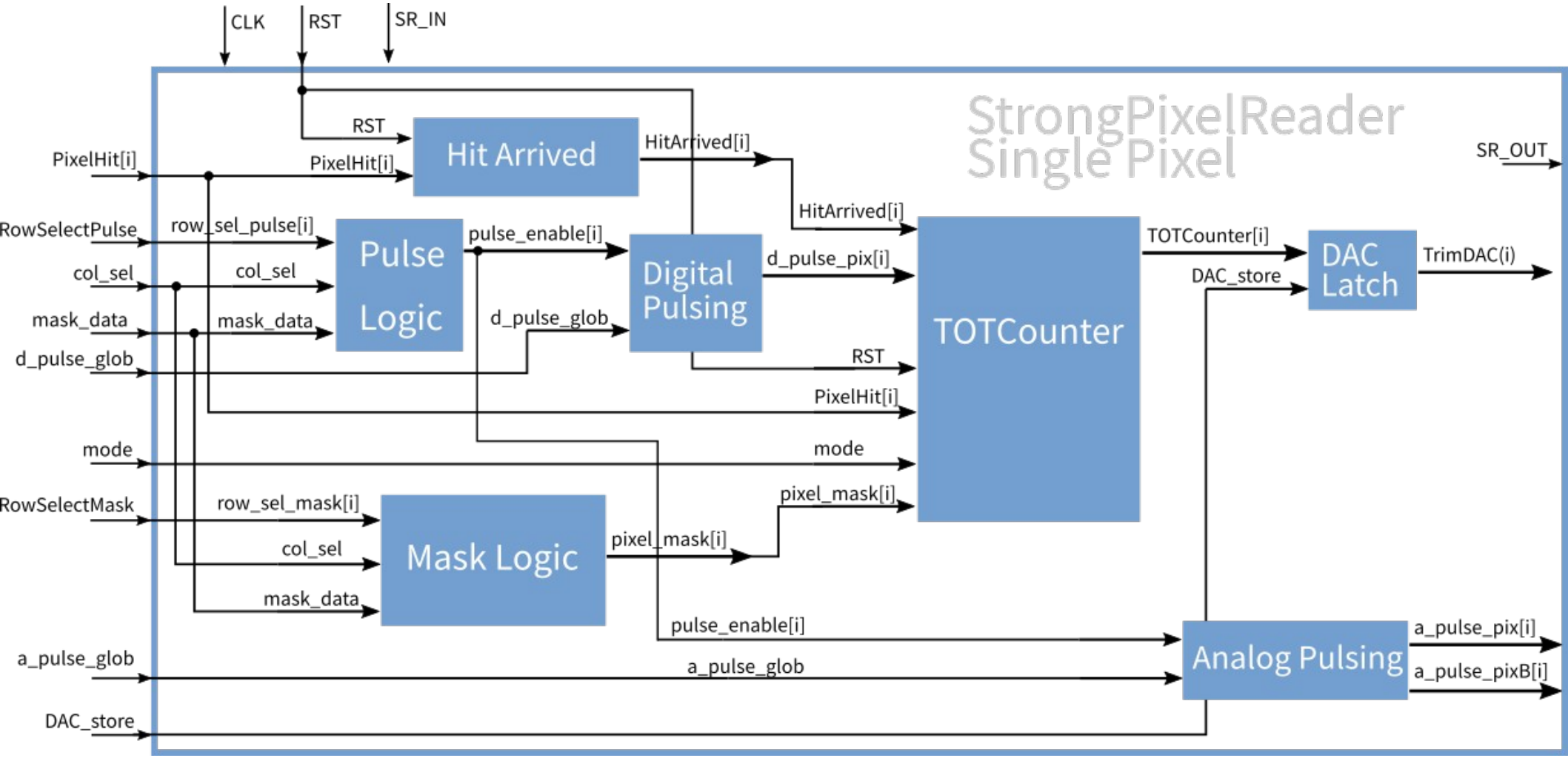
# Architecture: RowSelect



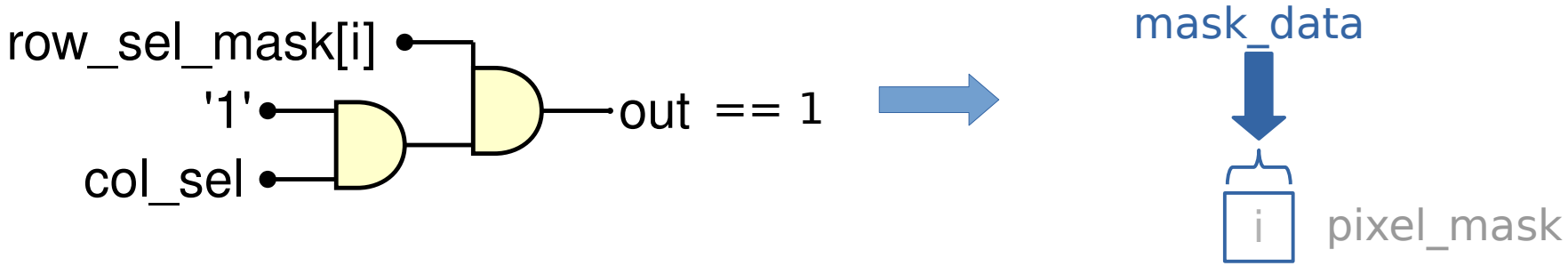
# Architecture: StrongPixelReader (32 pixels column)

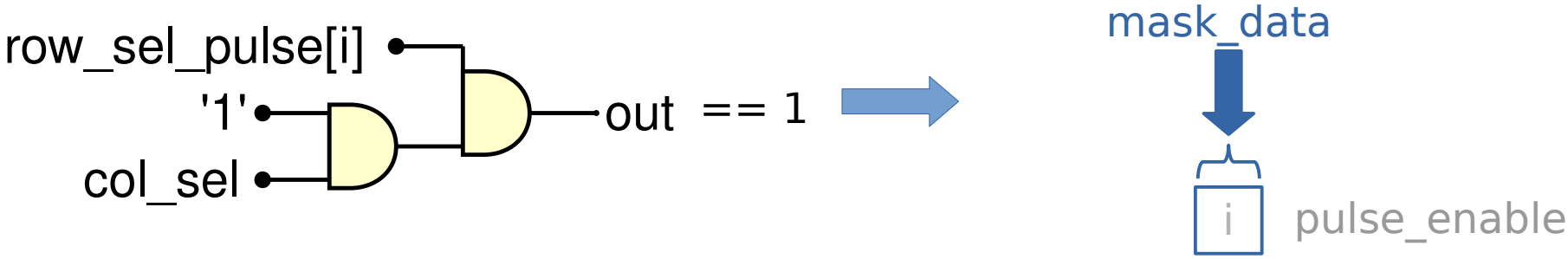


# Architecture: StrongPixelReader Single Pixel Block Diagram



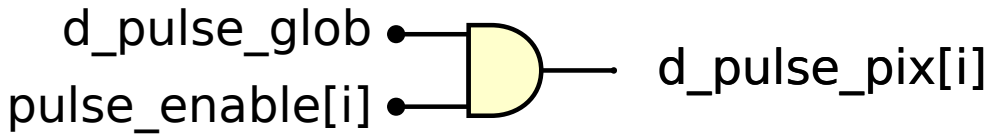
# Architecture: StrongPixelReader
# Pixel Masking Latches

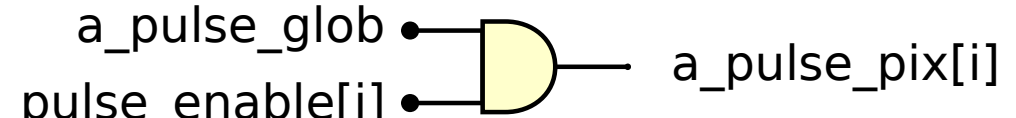



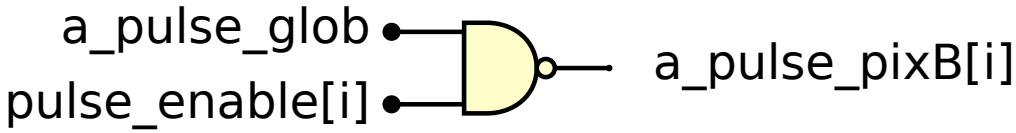
# Architecture: StrongPixelReader Pulsing circuit

Digital Pulsing Circuit

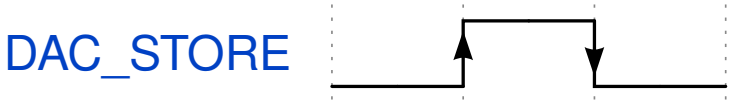



Analog Pulsing Circuit

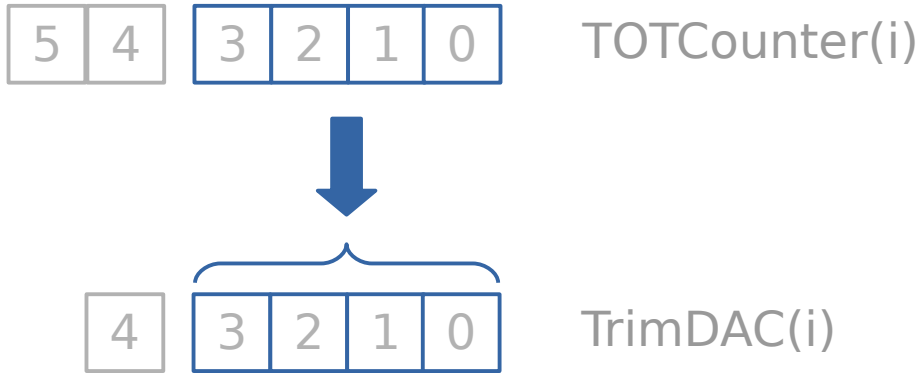


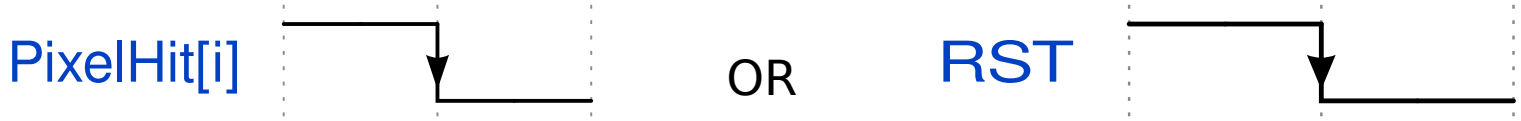
# Architecture: StrongPixelReader Trimming DAC Latches




DAC_STORE == 1

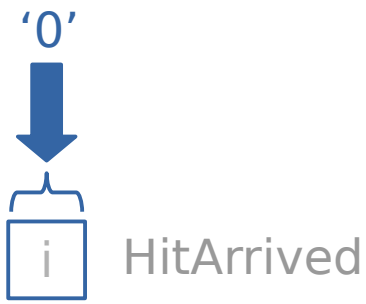


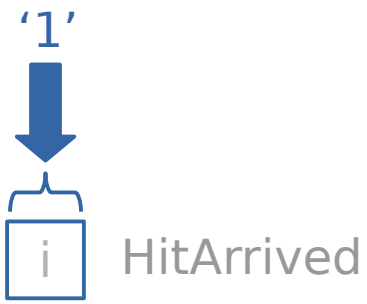
# Architecture: StrongPixelReader HitArrived




RST == 0

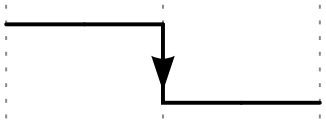
else PixelHit[i] == 0



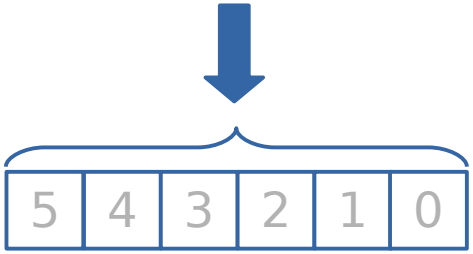



# Architecture: StrongPixelReader Counter

RST == 0

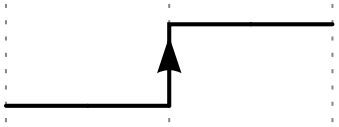


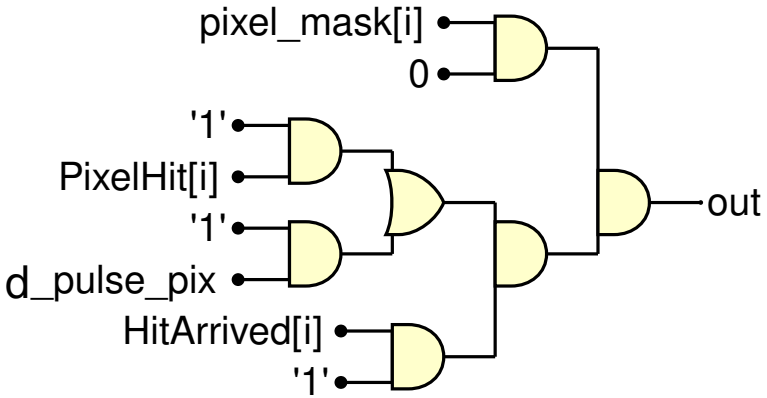

6x '0'




TOTCounter(i)

MODE 0



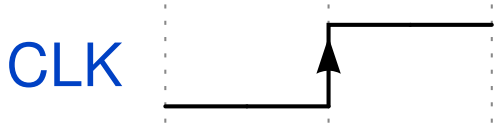



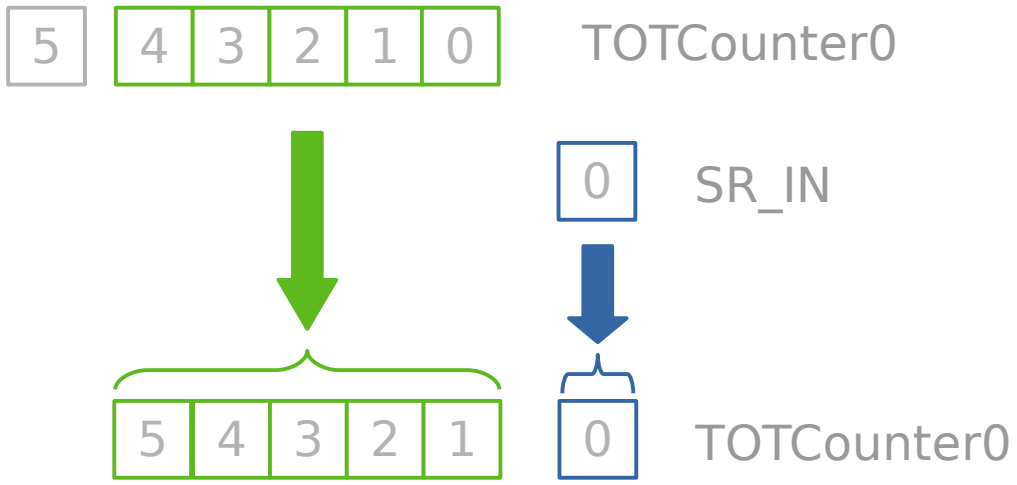

== 1 → TOTCounter(i)++

== 0 → TOTCounter(i) = TOTCounter(i)

# Architecture: StrongPixelReader Counter

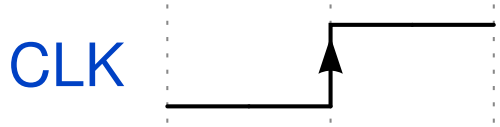
MODE 1

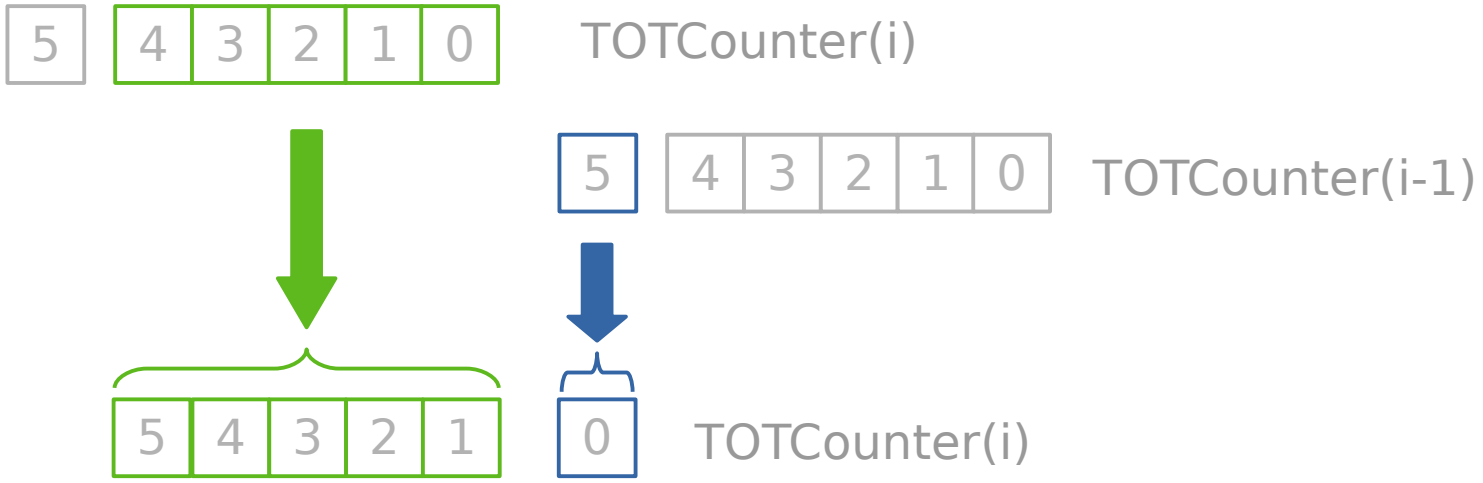


# Architecture: StrongPixelReader Counter

MODE 1



# Simulation: StrongPixelReader