Power consumption summary: total consumption of DAQ and FFE.

Most of power consumption comes from LVDS signals from T+ROC2 boards to and from Hidra2 boards, 64 of such a signals. When neglecting this power

TOTAL = $(4{,}33_{\text{HIDRA mW/Ch}} + 2{,}15_{\text{T+ROC2 mW/Ch}} + 0{,}63_{\text{T+ROC1 mW/Ch}}) * 16000\ \text{Ch} =>$

$6{,}61\ _{\text{mW/Ch}} * 16000\ _{\text{Ch}} =>$ **114W (without IO)**

Under study:

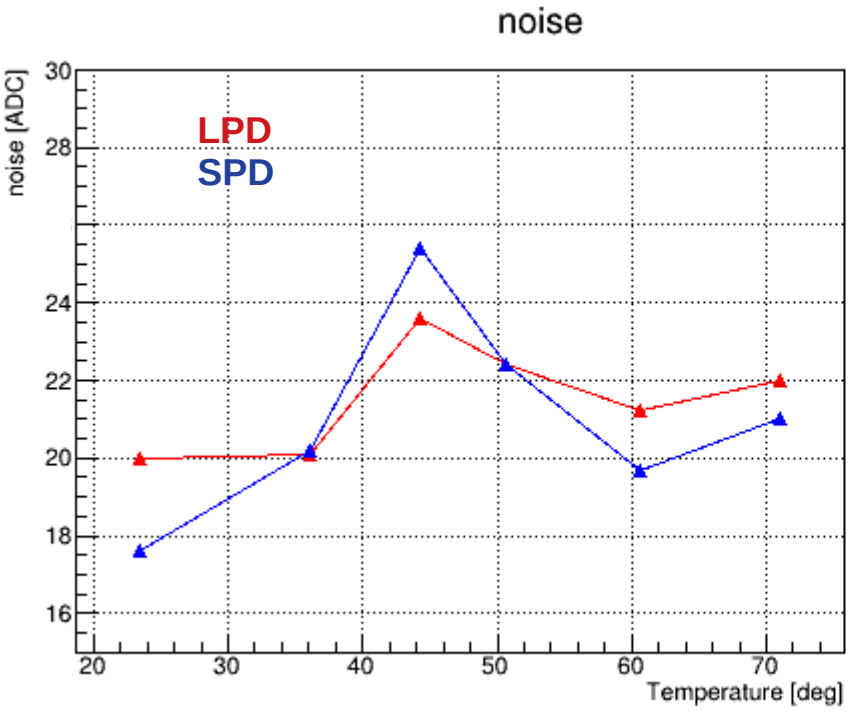
- **Getting closer T+ROC2 and Hidra2 and changing from LVDS to CMOS**
- **Disabling when not needed LVDS Tx /Rx between T+ROC1 ⊣ T+ROC2**
- **Changing to LVDS 2,5V where needed.**
- **Increasing the number of Hidra2 per T+ROC2 (from 4 to 8).**
- **…**

Estmation:

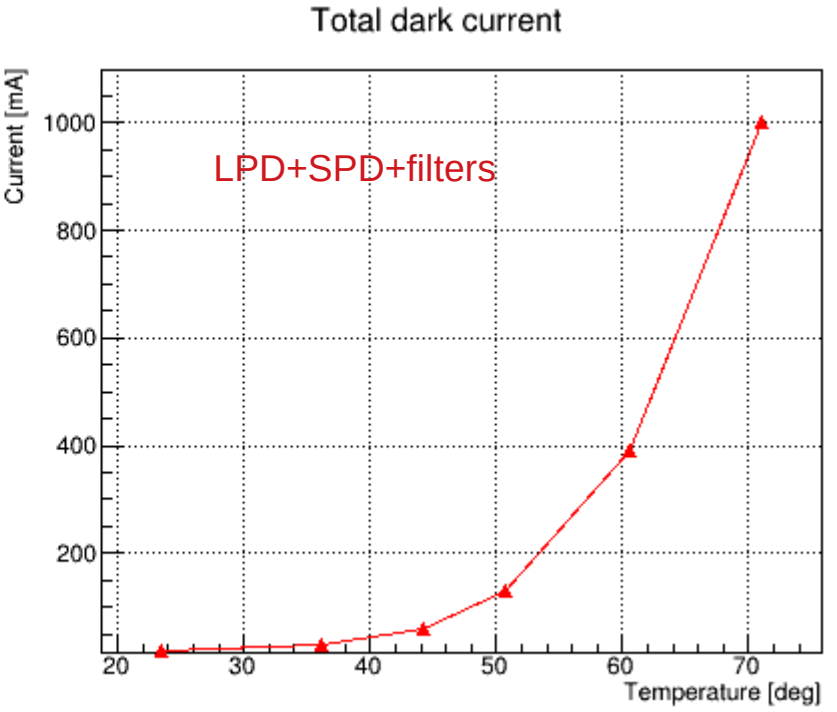
TOTAL < 150W

Using 150 W:
DAQ/FFE ~ 40%
150 = DAQ (60) + FFE (90)

First measurement at high temperature inside thermal chamber.



nA



Preliminary results (to be checked: pedestal stability; signal vs casis time ….)

Noise (i.e. pedestal distribution std. Dev.) is not strongly affected by temperature

Current strongly increase with temperature (~exponential)

Operating temperature range of PD: up to 70 deg??

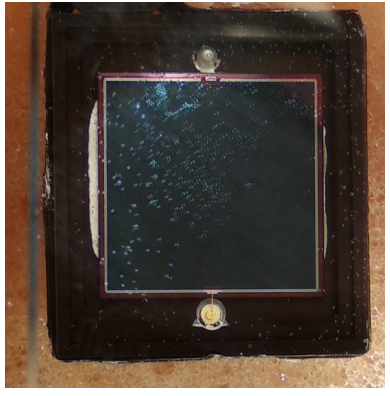
First test of low temperature for glue, cable, welds....

Thermal chamber: due to a problem we could test only a constant low temperature ~-13.7 deg: thermal cycles TBD.

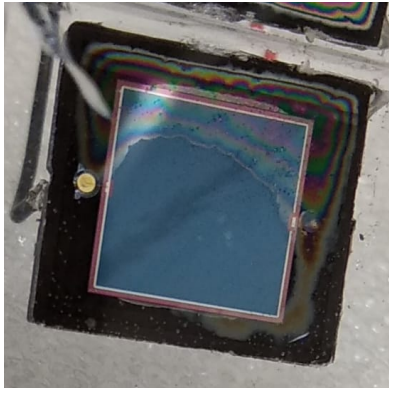
A old LPD (VTH2090) glued to a quartz crystal using the current glue for TB. The PD is connected to a kapton cable.

Kapton cable is connected to a samtec blue cable.

Before



After

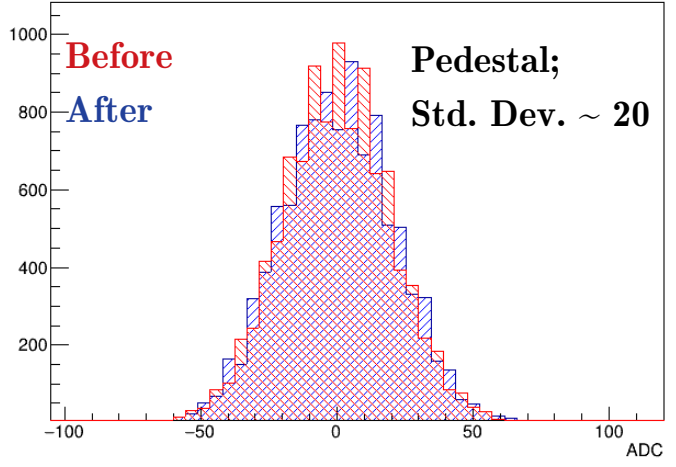


Large angle

PD quartz interface: BAD.

Bias and signal connection of PD to FFE: OK

Pedestal distribution: OK



Glue: EPOTEK 301, 24h @ room temperature

Try again with different gluing procedure.

Devices	Power (W)	Operating temperature (℃)	Storage temperature (℃)	Variation [max;min] (℃)
Photo-diodes (PD)	<0.1	15	[-10;70] (to be updated)	[-10;50]
Front-end E.	90	15	[-20;70] (to be updated)	[-20;50]
DAQ	60	15	[-20;70] (to be updated)	[-20;50]
PD bias	<10	15	[-20;70] (to be updated)	[-20;50]

Additional notes: (last update 16/04/2021)

Photo-diodes: here we include the PDs, the glue used to connect the PD to the LYSO, the kapton cables and the PD-kapton connections. The PD temperature ranges: should be updated with latest measurement results?

Front-end electronics: should be placed nearby the calorimeter bottom face in order to minimize the routing length for PDs.

DAQ: it should be near by the front-end electronics to minimize the number of differential links between boards.

PD bias: the DC-DC converters which provide the PD bias (~40 V) should be near by the front-end electronics (or those could be placed on the front-end boards) in order to minimize the bias noise and the power consumption.

Power consumption: measured at room temperature.