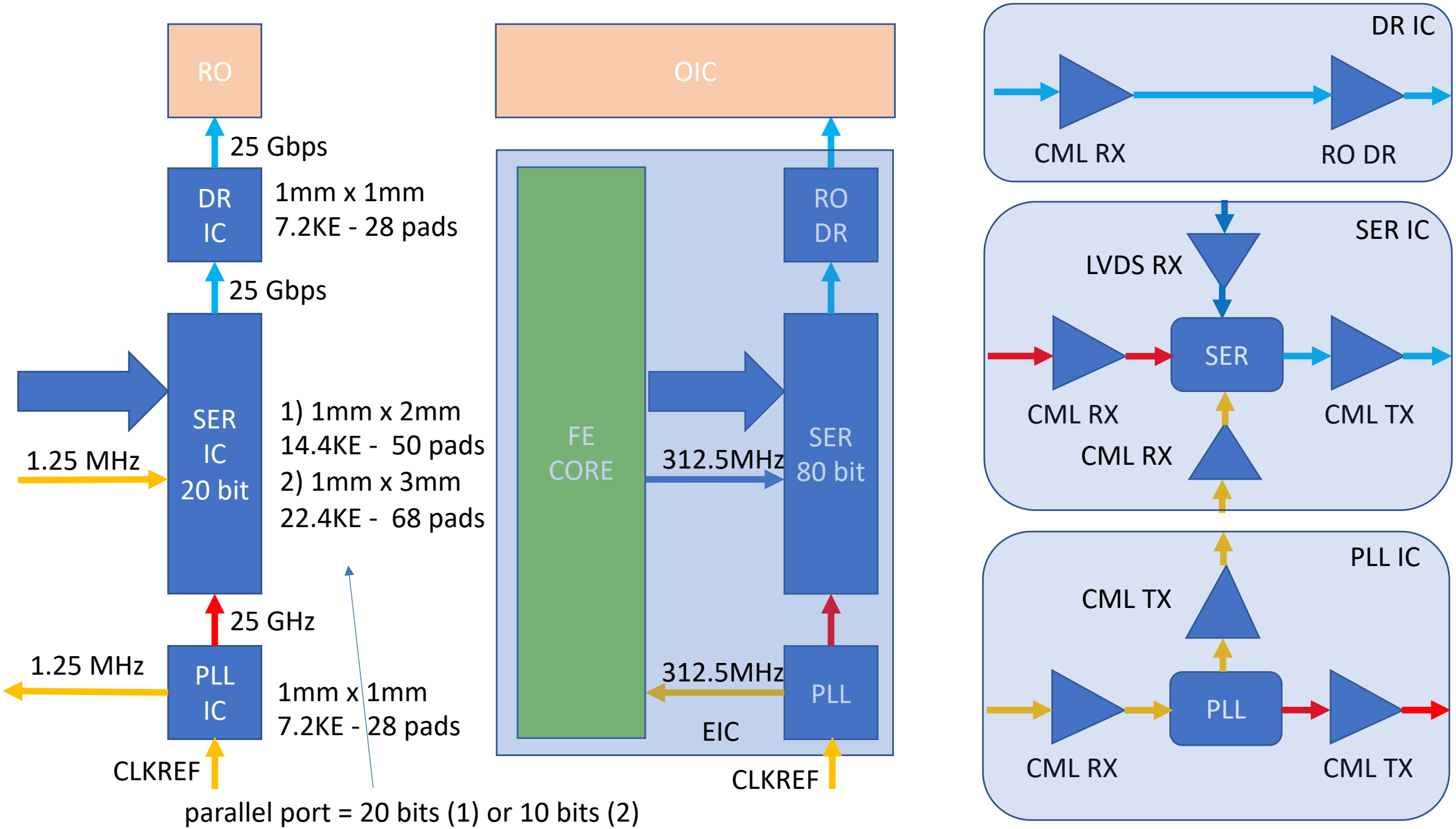
IP-CORES for High Speed Data Links

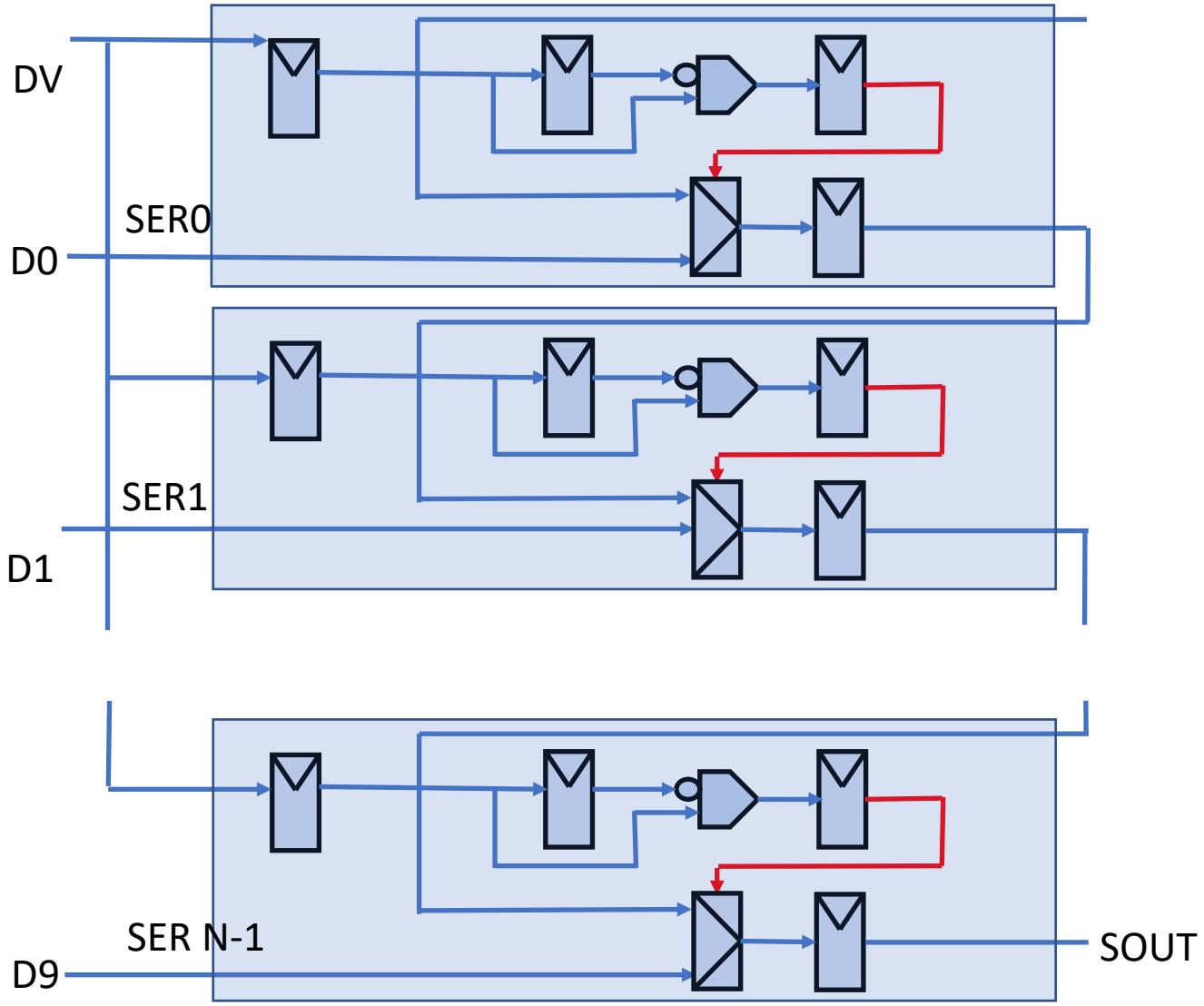
March 10th, 2021

IP-CORES for High Speed Links

- Development of a library of radiation tolerant IP-cores for the implementation of the high speed serial links for the data readout in FE ASICs
  - TID => 1 Grad
  - Data Rate => 25 Gbps
  - Compatibility with Off-The-Shelf Components (FPGA Transceivers)
- IP-Cores
  - PLL => OUT0 = 25GHz, OUT1 = 1.25GHz, OUT2 = 325MHz
  - SERDES => Nb = 80 (4x20), Data Rate = 25 Gbps
  - DRIVERS
    - CML (25 Gbps) – Compatible with Xilinx GTY Transceivers
    - Ring Oscillator Driver (25 Gbps)
  - RECEIVERS
    - CML(1.25GHz)

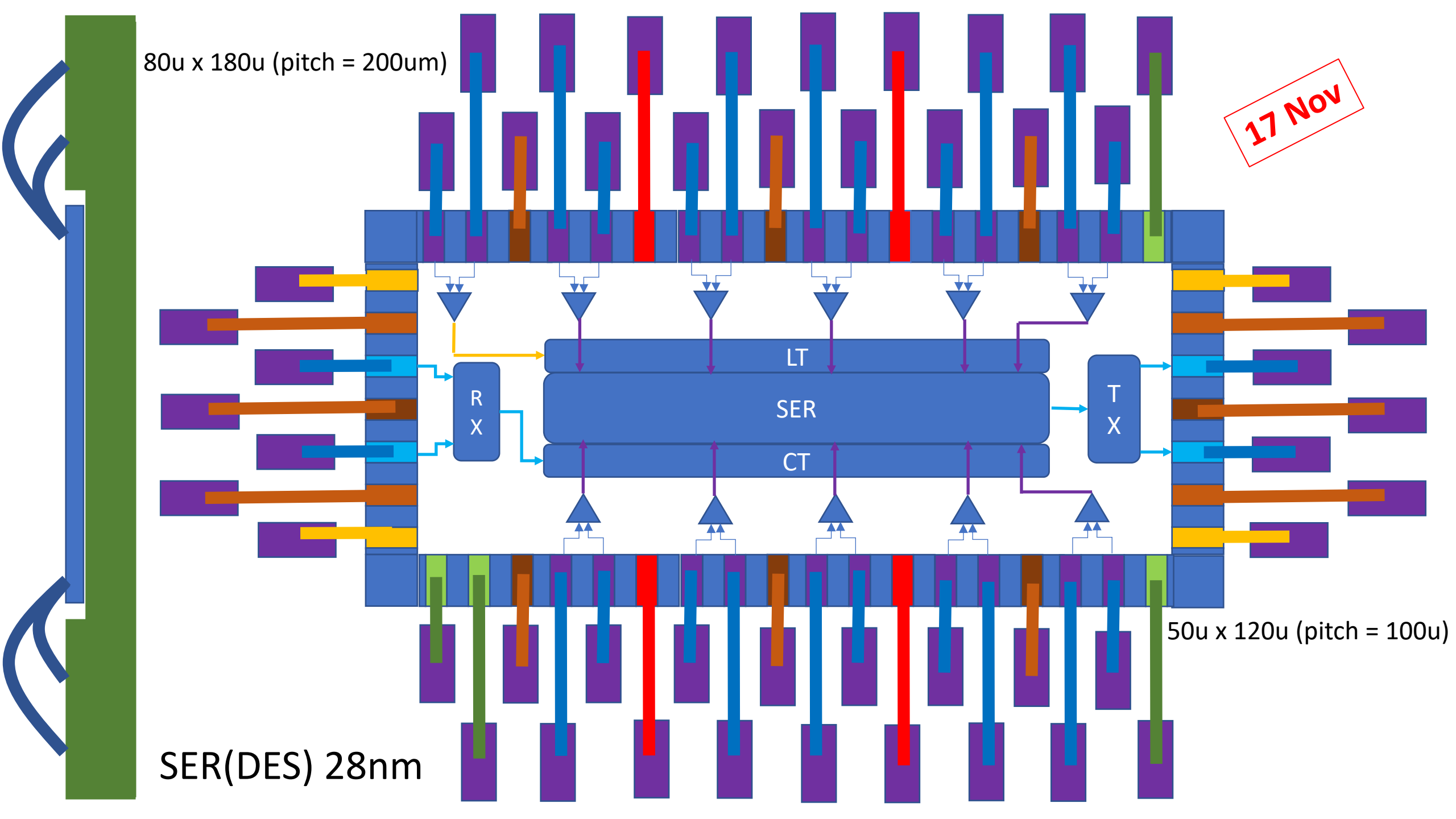

RO
25 Gbps
DR
IC
1mm x 1mm
7.2KE - 28 pads
25 Gbps
SER
IC
20 bit
1.25 MHz
1) 1mm x 2mm
14.4KE - 50 pads
2) 1mm x 3mm
22.4KE - 68 pads
25 GHz
1.25 MHz
PLL
IC
1mm x 1mm
7.2KE - 28 pads
CLKREF
parallel port = 20 bits (1) or 10 bits (2)
OIC
RO
DR
FE
CORE
312.5MHz
SER
80 bit
312.5MHz
PLL
EIC
CLKREF
DR IC
CML RX
RO DR
SER IC
LVDS RX
SER
CML RX
CML TX
CML RX
PLL IC
CML TX
PLL
CML RX
CML TX

SER(DES) 28nm

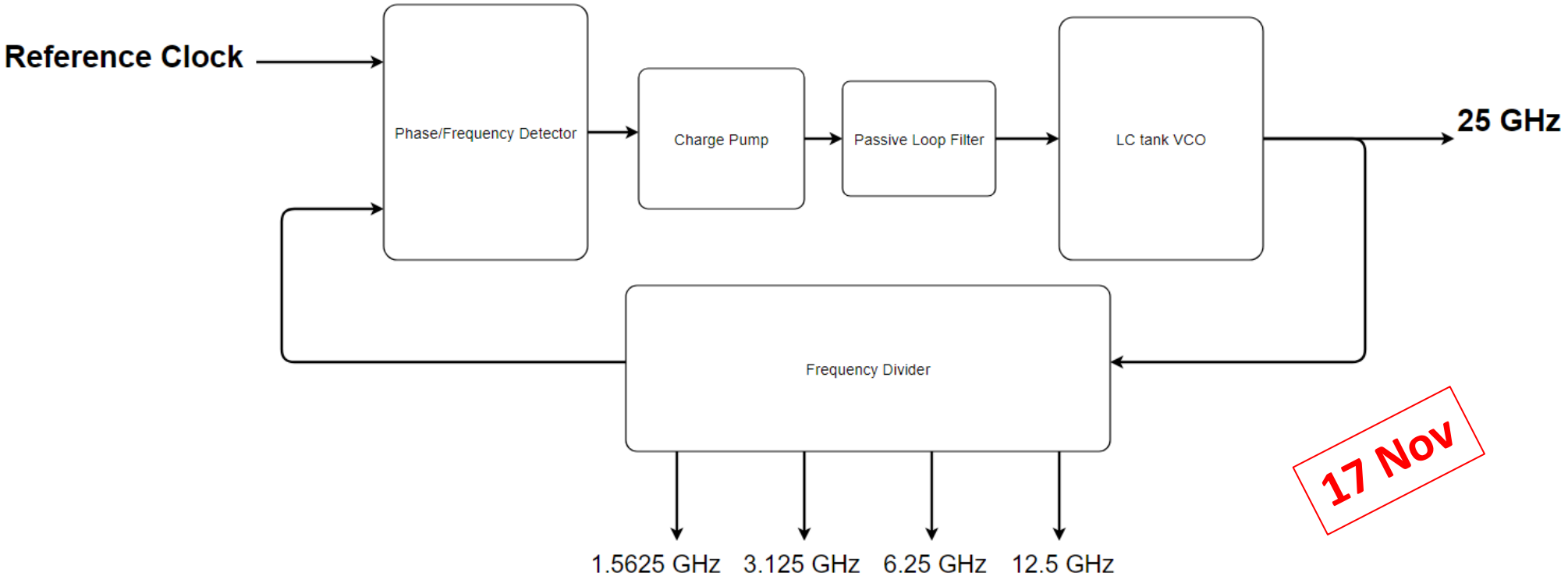


SERDES28

- Architecture:
  - Daisy chain of identical cells with LOAD internally generated at the rising edge of the Data Valid
- Size
  - SERDES65(10 bit) =>
    - 300um x 400um
  - SERDES28(20 bit) =>
    - < 0.25mm2 (SER)
    - < 0.20mm2 (CML TX)
- Power
  - SERDES65(10 bit) =>
    - 400mA
  - SERDES28(20 bit) =>
    - < 1W


80u x 180u (pitch = 200um)
17 Nov
LT
SER
CT
R
X
T
X
50u x 120u (pitch = 100u)
SER(DES) 28nm

25 GHz Phase-Locked Loop in 28 nm CMOS technology



Output Frequencies:

→ 25 GHz

→ 12.5 GHz

→ 6.25 GHz

→ 3.125 GHz

→ 1.5625 GHz

17 Nov

Specs:

- Area < 0.1 mm^2
- Phase Noise @ 1 MHz < -90 dBc/Hz
- Power Consumption < 50 mW

Blocks to be submitted in November:

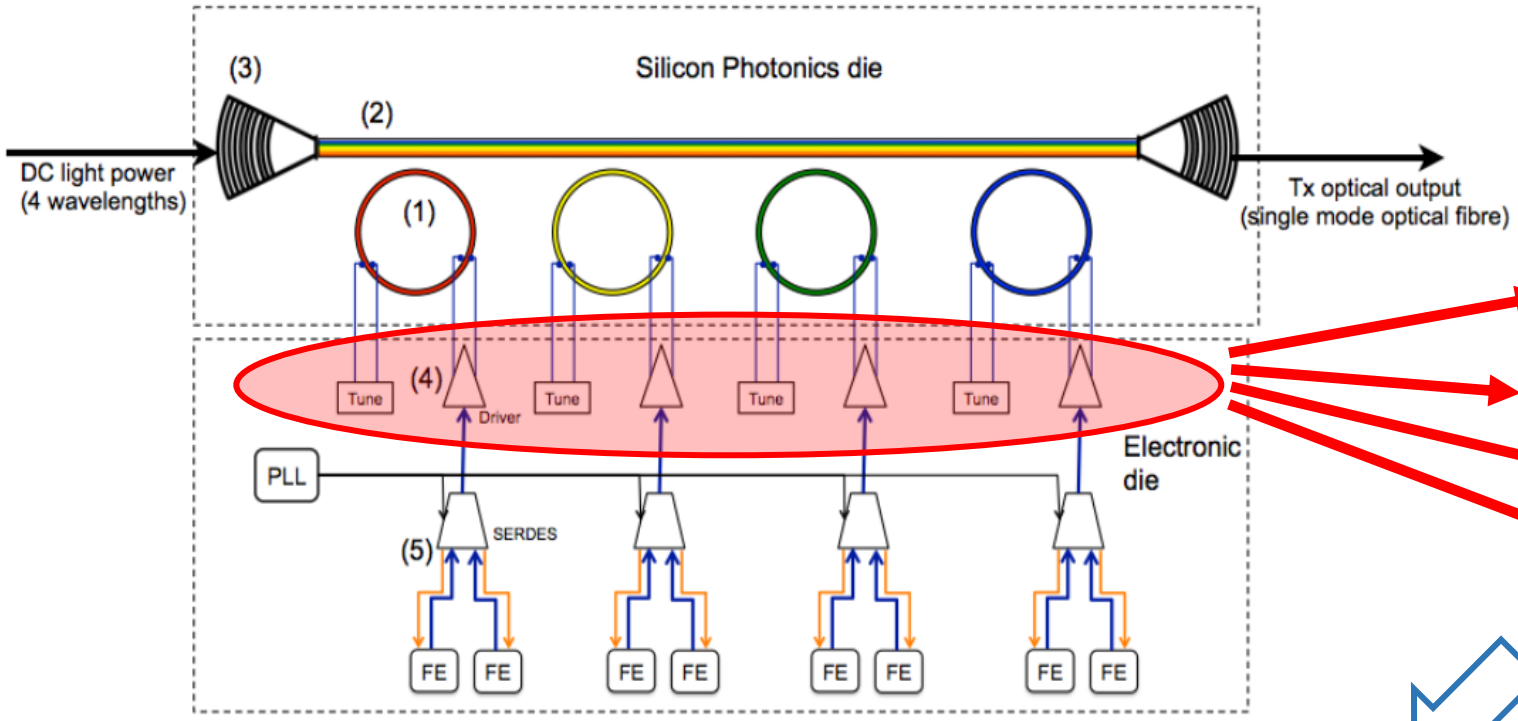
- Phase/Frequency Detector
- Charge Pump
- Passive Loop Filter

A 25 GHz VCO has been already submitted

- 1.25 MHz
- 312.5 MHz

Slide from Marco Mestice

25 Gb/s Drivers for RR



High-Speed ESD Protections + Pads

Chips bonding: Al/Au wires (& flip-chip)

4 Drivers at 25 Gb/s

Ring Resonator Thermal Tuning

EIC-1 Pisa submission:

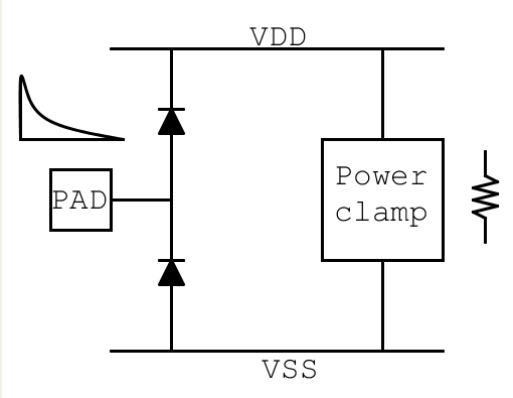
- **1 RR Driver**
- **1 RR thermal control**
- **High-speed ESD & pads**
- **Other low pad dev (pad limited)**

17 Nov

Slides from Gabriele Ciarpi

PADs and ESD protections

Starting Point:



- 1 kV and 2 kV HBM ESD with low capacitance (100-200 fF)
- Low resistance Power clamps

28nm-HPC

Not tested

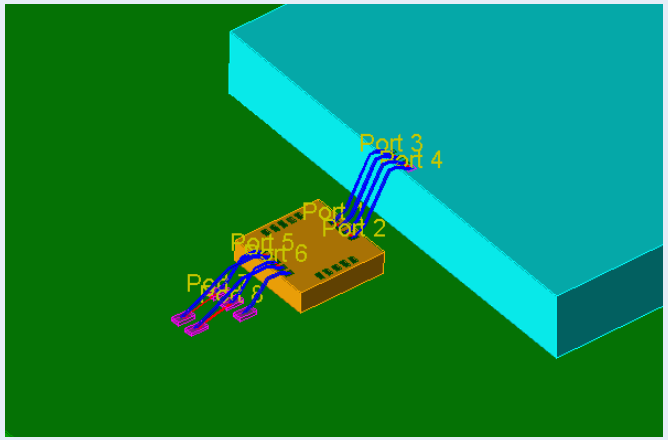
Targetting:

- 500 V Machine Model with low capacitance
- Custom inductors for loading reduction (em simulator)
- Standardization of pads and ring

30 June

Chip Coupling

Starting Point:



- Simulation results (low accurancy)

Targetting:

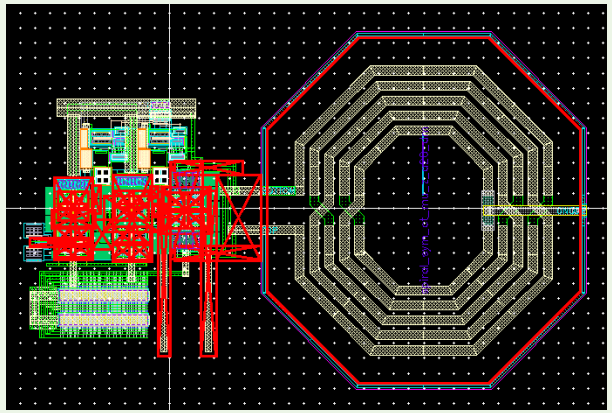
- Improve chip-chip coupling
- Testing board for coupling enancement
- High frequency COTS (connectors, cables…)

Work in progress

31 July

25 Gb/s drivers

Starting Point:



- 25 Gb/s ±500mV RR driver
- Passive and active bandwidth enhancement

28nm-HPC

Not tested

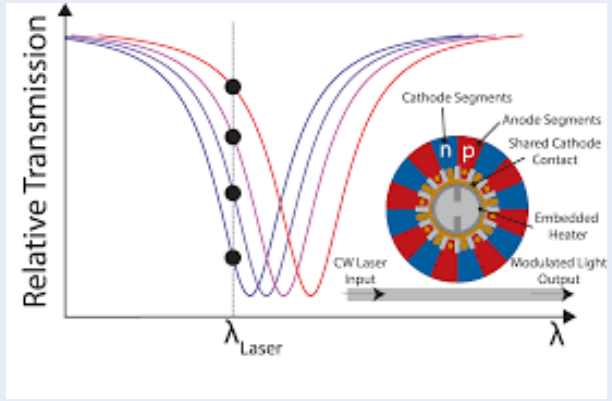
Targetting:

- 25 Gb/s ±500mV RR driver in 28 nm HPC+
- Improving high-frequency performances
- Group delay improvement

30 Sept

Thermal feedback

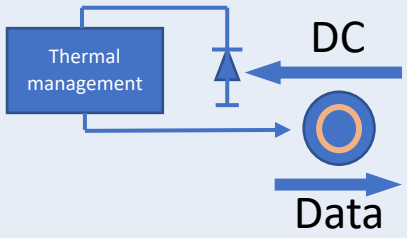
Starting Point:



- External tuning

Targetting:

- Integrated temperature tuning



31 Oct