TF7
Electronics and On-Detector Processing

Conveners: Dave Newbold, Francois Vasey

Members: Niko Neufeld, Valerio Re, Christophe de la Taille, Marc Weber

Mandate

- The development of electronics in general and ASICs in particular will continue to play a very important role for all future experiments in HEP.
- These HEP developments will have to follow the microelectronics industry to smaller feature sizes in order to benefit from the increasing transistor density, the intrinsic high speed and the lower power consumption.
- In addition, the need to follow industry to newer technologies is also mandatory as production lines for older technologies are discontinued.
- Infrastructures at the HEP institutes for the design of complex mixed-mode CMOS ASICs have to be built up to match future challenges and emerging design and verification methods need to be explored.

Mandate

- To process the data generated by the detectors' high speed optical links, chips for data aggregation and filtering as well as FPGAs need to be brought to the level required for future experiments.
- If integrated photonic nodes become available, new avenues of development might open.
- The low operation voltages of present and future chip technologies will make the development of on-chip DC-DC converters and power management blocks essential for future low mass detectors.
- The scope of this task force should also include developments exploring more sophisticated interactions between on-detector and off-detector electronics, keeping in mind and profiting from the rapid evolution of commodity electronics.

Mandate

- The radiation tolerance for the electronics required by future experiments, in particular those at hadron machines, is unique to applications in HEP and needs to be addressed in a common international effort

Mandate

- Interconnection technologies, post processing and packaging will become essential for future high-density detectors.
- In hybrid pixel detectors for example the high cost of flip-chip bonding is a limiting factor, and alternative methods are already in use in industry and may also be explored by HEP.
- Access to these sophisticated technologies is often restricted to large size projects, and will benefit from a community-wide approach.
- The format and packaging of on-detector electronics will be driven partly by integration, material, and power/cooling concerns, and will thus need to be covered across task forces TF7 and TF8.

Symposium TF7 on March 25

09:00 → 09:15 **Introduction and background** 15m

Speakers: Prof. Dave Newbold (STFC Rutherford Appleton Laboratory (GB)) , Francois Vasey (CERN)

09:15 → 09:30 **Part A Introduction: ASICs and front-end electronics** 15m

Covering scope and summary of inputs

Speakers: Christophe De La Taille (OMEGA (FR)) , Valerio Re (Universita and INFN (IT))

09:30 → 10:00 **Keynote talk: Future trends, challenges and opportunities in ASICs for HEP: a birds-eye view** 30m

Speaker: Angelo Rivetti (INFN - National Institute for Nuclear Physics)

10:00 → 10:10 **Topical invited talk: Moving to leading-edge technology nodes** 10m

10:10 → 10:20 **Topical invited talk: 3D integration** 10m

Speaker: Christophe Wyon (CEA French Alternative Energies and Atomic Energy Com)

10:20 → 10:30 **Topical invited talk: Perspectives on future development (TBC)** 10m

Speaker: Erik Heijne (Czech Technical University in Prague (CZ))

10:30 → 11:00 **Comments and brief discussion** 30m

Identifying points to take to afternoon discussion

Symposium TF7 on March 25

11:15 → 11:30 **Part B Introduction: Links, powering and integration** 15m

Speakers: Francois Vasey (CERN) , Marc Weber (KIT - Karlsruhe Institute of Technology (DE))

11:30 → 12:00 **Keynote talk: Front-End Power and Links: Trends and Expected Needs** 30m

Speaker: Philippe Farthouat (CERN)

12:00 → 12:10 **Topical invited talk: Future rad-hard optical links** 10m

Speaker: Jan Troska (CERN)

12:10 → 12:20 **Topical invited talk: Wireless link technologies on the detector** 10m

Speaker: Richard Brenner (Uppsala University (SE))

12:20 → 12:30 **Topical invited talk: Powering and data communications challenges at FCChh** 10m

Speaker: Werner Riegler (CERN)

12:30 → 13:00 **Comments and brief discussion** 30m

Identifying points to take to afternoon discussion

Symposium TF7 on March 25

14:00 → 14:15 **Part C Introduction: Off-detector systems** 15m

Speakers: Prof. Dave Newbold (STFC Rutherford Appleton Laboratory (GB)) , Niko Neufeld (CERN)

14:15 → 14:45 **Keynote talk: DAQ and Trigger Beyond HL-LHC** 30m

Speaker: Dr Emilio Meschi (CERN)

14:45 → 14:55 **Topical invited talk: Challenges of large software-oriented TDAQ systems** 10m

Speaker: Dr Alessandro Thea (Rutherford Appleton Laboratory (GB))

14:55 → 15:05 **Topical invited talk: Using COTS processing technologies effectively** 10m

Speaker: Conor Fitzpatrick (University of Manchester (GB))

15:05 → 15:15 **Topical invited talk: Moving intelligence onto the detector** 10m

Speaker: Farah Fahim (Fermilab)

15:15 → 15:45 **Comments and brief discussion** 30m

Identifying points to take to afternoon discussion

Symposium TF7 on March 25

16:00 → 17:30 **Open discussion** 1h 30m

To cover the following themes:

- Synthesis of priority questions / topics from themes
- Learning from LHC and other projects
- The process of choosing R&D priorities
- Organisation, training and sociology
- The rest of the roadmap process

- Are requirements of future experiments reasonably achievable for electronics?

- Design of electronics systems should be an integral part of the design of detectors and experiments

- Next slides: a selection of outcomes from the input session on Future Facilities (Feb.19)

FCC-hh

Challenges for Read-Out Electronics & Trigger (TF7)

- **Huge amounts of data produced** (e.g. O(1000TByte/s) = O(10Pbps) for zero-suppressed tracker)
  - **Streaming:**
    - Read-out everything → need fast low power radiation hard optical links
    - Alternative: summarize received data by higher-level quantities and only transmit and store those
  - **Triggered:** Read-out interesting events → challenge to achieve a data reduction of factor O(10) (HL-LHC aims for factor 40) with much higher pile-up
    - → need efficient triggering – intelligent decision as close to the sensor as possible (ML or AI on front-end, programmable ASICs, FPGAs?)
    - → radiation hard buffering/storage
- **→ High bandwidth, low power, radiation hard data links**
  - Industry at link speeds of 400Gbps, need to be adapted to radiation hardness, low power, low material and distributed data sources
  - Rad. hard link R&D targeting 25Gbps has started at CERN, but will need 50-100Gbps links to fulfil FCC-hh requirements
  - Low-power: 10Pbps = 1 million lpGBTs (~500mW) → 500kW for the links alone!
    - Cooling needs cause large amounts of dead material → minimize cooling needs
  - New technologies: CMOS with integrated photonics (Silicon Photonics)
    - DOE Instrumentation BRN: “The presently used data link architecture in which front-end ASICs communicate electrically to optical converters does not scale to arbitrary data rates…. New architectures will need to be explored to solve this problem. In terms of ASIC technology, industry predicts that photonics will be integrated with CMOS processes within 5 to 10 years.”

FCC-hh

- **Wireless read-out systems:**
  - Potential to reduce material – interesting if wireless transmission can fulfil the low-power requirement
  - But main material contribution coming from power and cooling needs (and not from optical fibers)
- **Analogue to digital conversion** will be located at the front-end
  - Already the case for all HL-LHC upgrades, e.g. analogue calorimeter trigger Run1 and Run2 → digitization at the front-end for HL-LHC
  - Advantages: low noise, standardised and efficient digital transmission
  - But needs radiation hard and low-power ADCs and ASICs (300MGy, 10^{18}neutrons/cm^2)
    - For comparison: HL-LHC factor 30 less, 65nm ok up to O(3MGy)
- Develop **radiation hard power management blocks** (DC/DC converters, regulators)
- Develop **precision clock and timing circuits** (PLL, DLL, Timing Discriminators, Delay Lines, Picosecond TDCs)
  - Timing distribution with pico-second synchronization

Linear high-energy e+e- machines

- Highly integrated electronics crucial for LC detectors, to enable required compactness and hermeticity
- ***ASICs*** central for all subsystems - ***ultra-low power consumption*** a central theme
  - Optimised for ***power-pulsing*** - however, suitability of such ASICs for beam tests, pre-installation calibration and cosmics data taking is a challenge.
  - Maximal integration requires modern technologies, ***small feature size***: costly development, increasing demand on ***verification***
- ***Compact interfaces*** - high-density boards for services and communication between VFE and off-detector electronics
- ***Large-area multi-layer*** electronics boards with high mechanical precision, far beyond industry standards - in particular for highly granular calorimeters
- DAQ requirements relatively benign - ~100 MB of zero-suppressed data per bunch-train, up to ***~5 GB/s***
  - Significantly higher for calibration runs without or with reduced zero suppression

- CMOS technologies are becoming more and more complex, making it impossible to effectively support too many variants
- 65 nm, 28 nm, next?
- Radiation tolerance, cryogenic temperatures
- Design of integrated electronics in CMOS sensors (65 nm, 28 nm imaging processes)
- Will 3D integration become available?

INFN

- **CHIPIX65** (call gruppo V, P.I. Lino Demaria)

28 nm CMOS ASIC for pixel detectors with high time resolution

- **Timespot** (call gruppo V, P.I. Adriano Lai)

28 nm CMOS ASIC for pixel detectors with high time resolution

- **Falaphel** (call gruppo V, P.I. Fabrizio Palla)

28 nm CMOS for CMOS ASICs interfacing with silicon photonics devices for high rate data transmission

- **AIDAINNOVA**

WP with network on 28 nm CMOS, 130nm/65nm chips for detectors in the project

TF7 outlook

- At this point TF7 is open to suggestions from the community (I solicit inputs from INFN)

- Development of new electronics systems with advanced technologies (nanometer CMOS, 3D integration) requires a community of fully trained designers; in my opinion, it is crucial that INFN supports this community