Timespot1

A CMOS 28-nm ASIC for tracking applications

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On behalf of the TimeSPOT team

F/E solutions 1: Si-Ge

*Improved discrete components **Si-Ge BJT** allows almost reaching the theoretical performance…*

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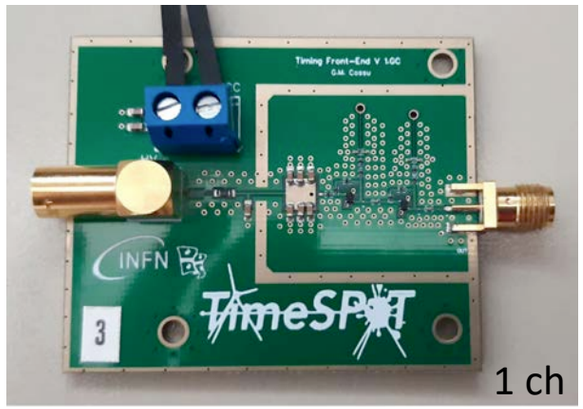

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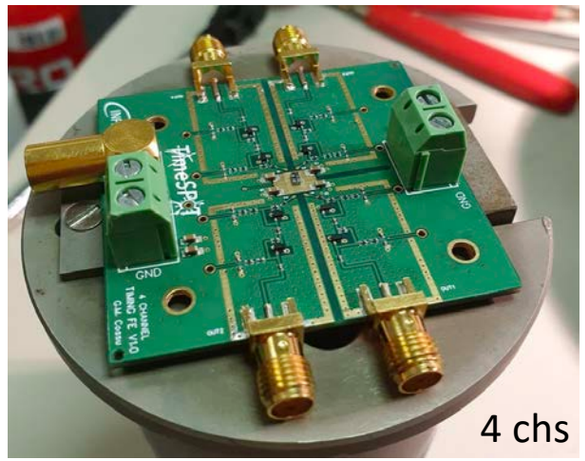


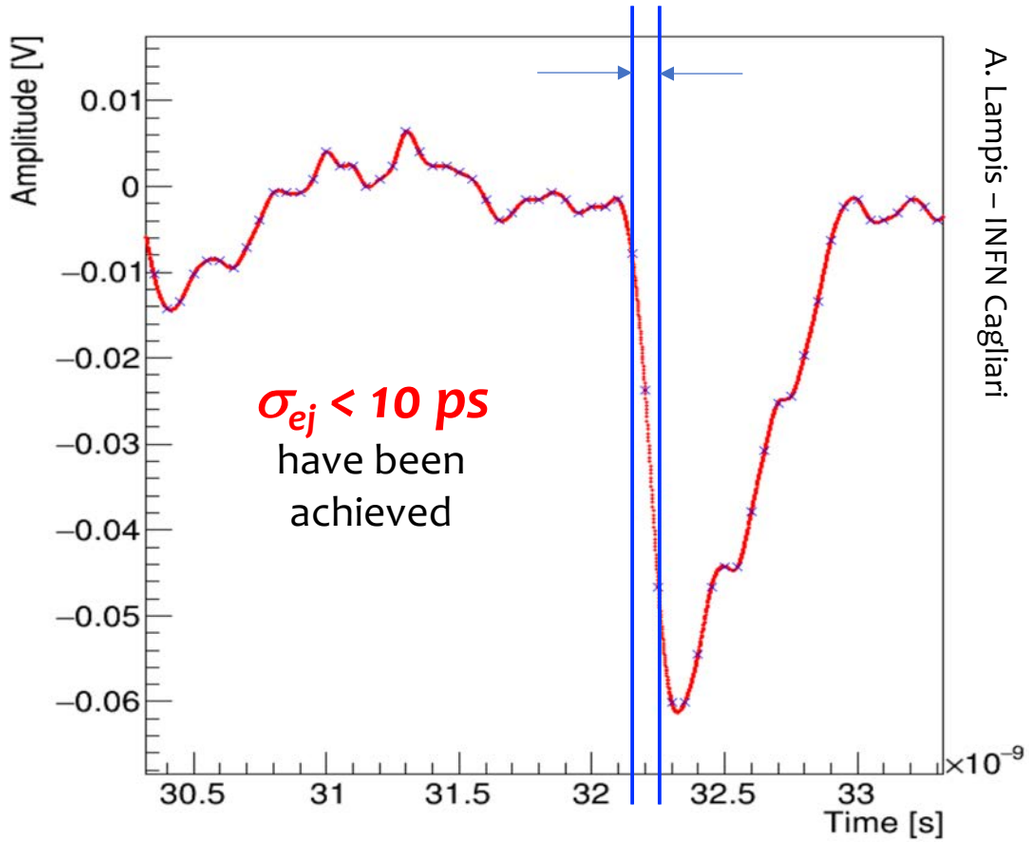
4 chs

…Drawbacks:

1. High consumption (mW/channel)
2. No integration (few wire-bonded channels)

Integrated 130 nm BiCMOS (Si-Ge):
best performance in speed, relatively scarce integration capabilities, not duly characterized against radiation

rise time t_r = 100 ps



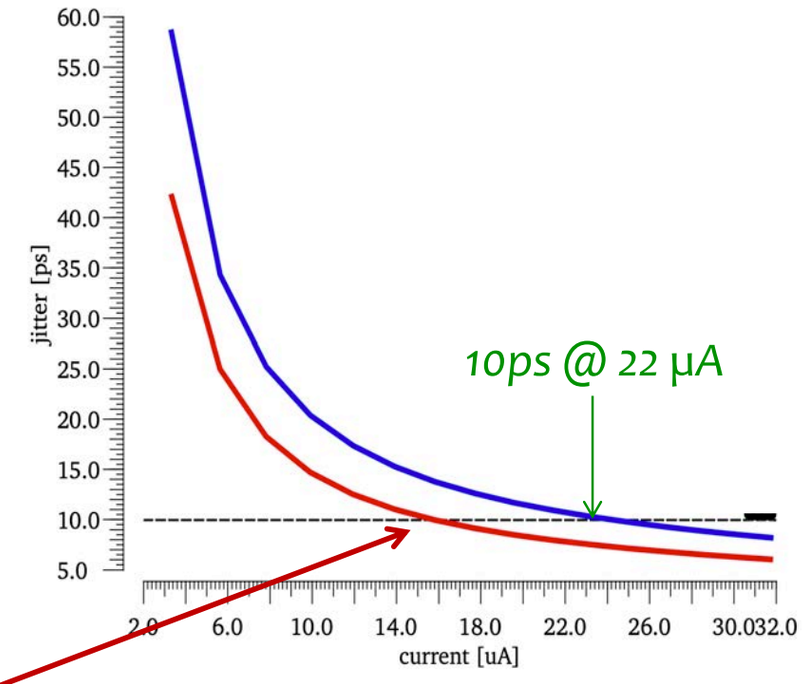
F/E solution 2: CMOS

and our TimeSPOT ASIC

- Integrated CMOS as important limitations: smaller g_m of the input stages (smaller gain and BW wrt Si-Ge BJT): difficult to reach t_r < 1-2 ns
- Integration is expensive in time and money: analogue designers tend to be conservative in implementing front-end solutions

Present pixel front-end designs are based on a traditional scheme: CSA with telescopic cascode input stage and Krummenacher feedback (e.g. RD53 ASIC, CMOS 65-nm, ATLAS-CMS).
In **Charge Sensitive** approaches this is an optimal solution (compact, stable, **low consumption**)
In high time resolution applications this is not the ideal solution for timing performance: sensor speed is not fully exploited

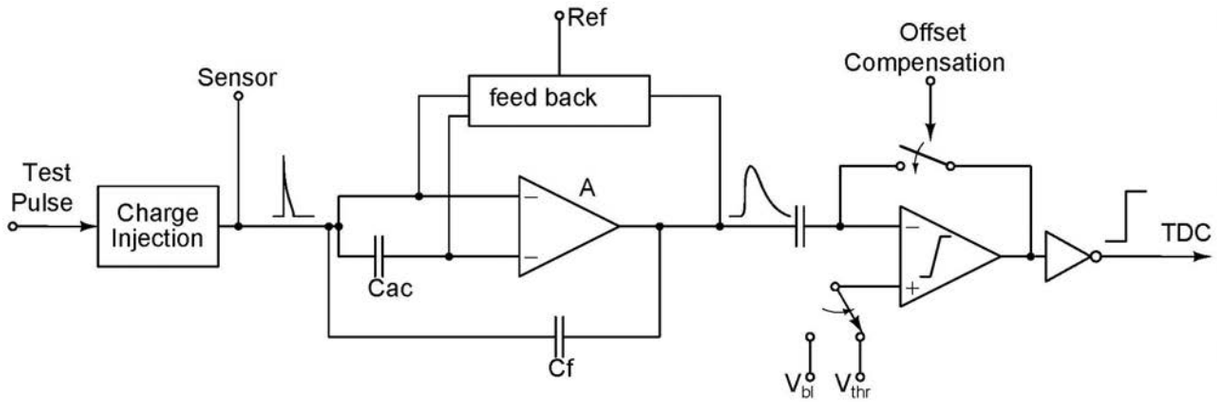
A new scheme (TimeSPOT, CMOS 28-nm): CSA inverter input stage, which sums–up the g_m's of 2 input (N and P) MOS
→ t_r reduction (<2 ns wrt ≈ 10 ns of previous solution)
→ BW increase + negligible Gain reduction by GBWP effect
→ Time jitter reduces by increasing power and do not saturates as in previous (cascode) version

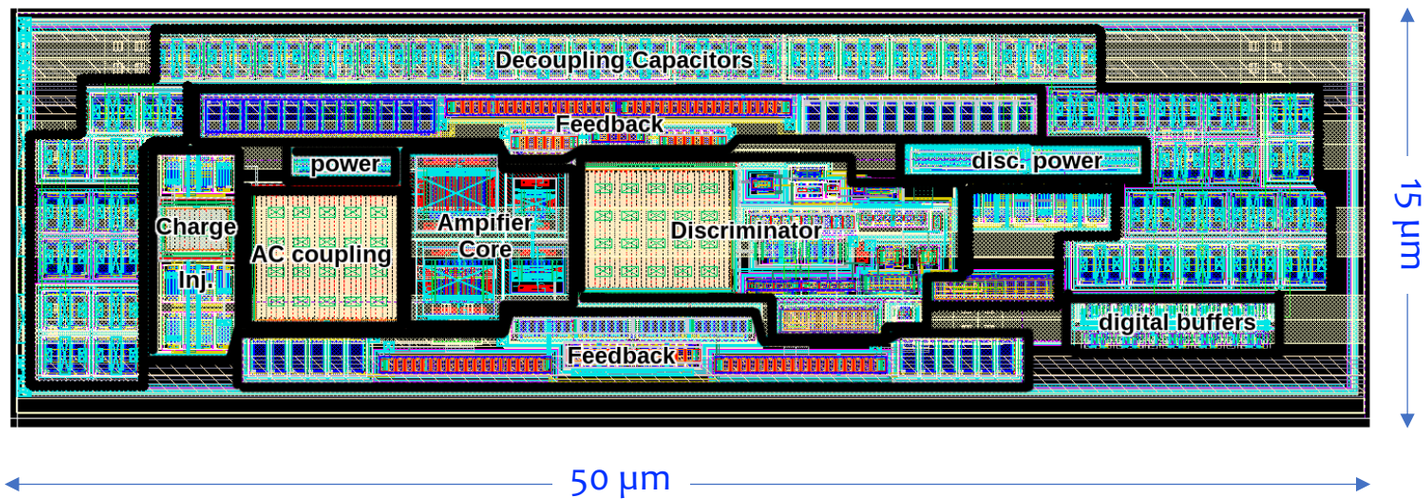


Time jitter vs current consumption of the CSA stage (CMOS 28-nm). Red curve: schematic simulation. Blue curve: post-layout simulation after parasitics extraction.

Timespot1: Analog Front End - 1

Inverter core amplifier with double Krummenacher FB



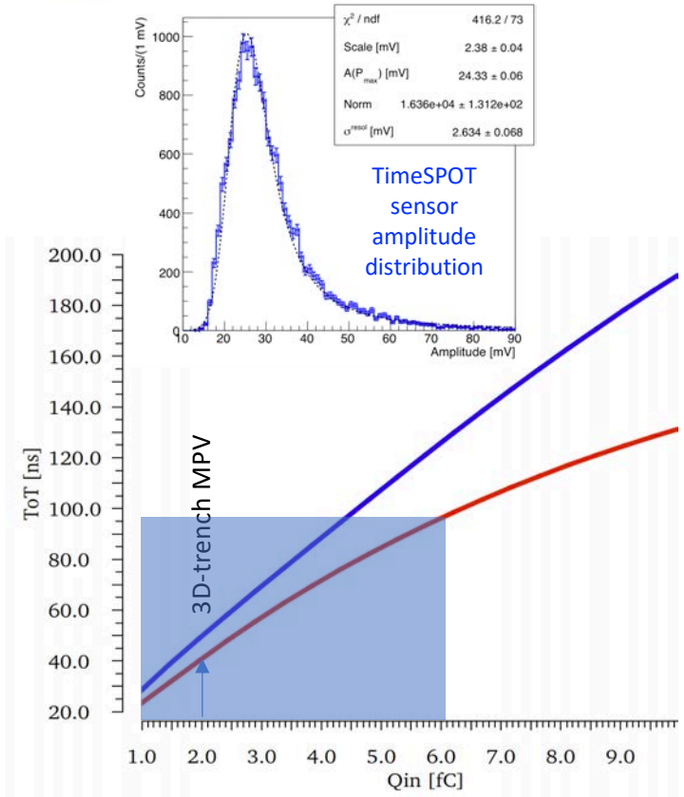


Post-layout simulation results

Pwr regime	nominal	high
Pwr/channel [µW]	18.6	32.9
Slew rate [mV/ns]	250	360
Z_{in} [Ω] in BW	23k	23k
Gain [dB]	93	93
RMS noise [mV]	3.9	3.8
BW [MHz]	311	455
Jitter [ps]	15.6	10.5

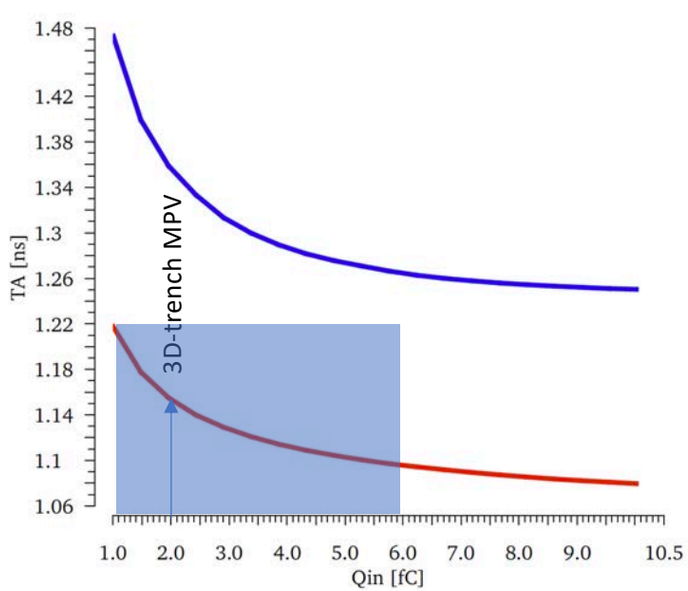
Analog Front End - 2

Comparison with "classic" CSA with KFB ("old version")

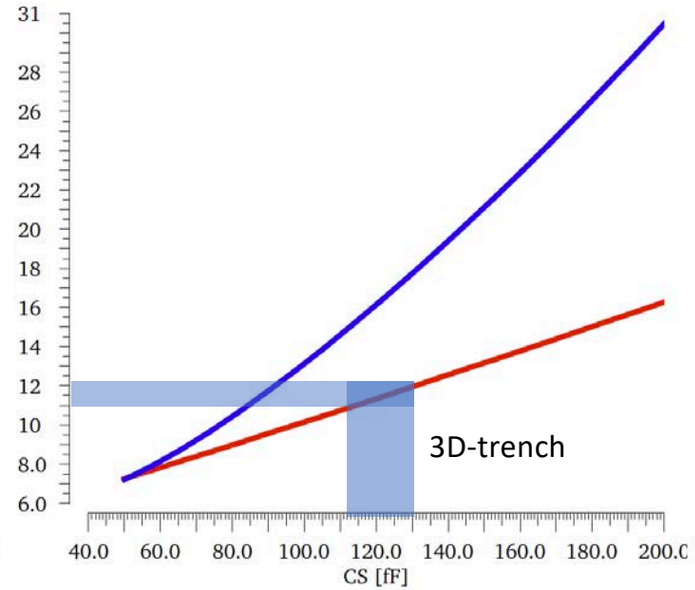


Time over Threshold
vs input charge
MPV ≈ 2fC (ToT ≈ 40 ns)
Corrections beyond 6 fC (≈90 ns)
are not worth considering

Old version
This version



Time walk
Corrections beyond 6 fC (≈90 ns)
are not applied
ToT bits are minimized to 8
(LSB ≈ 1 ns)



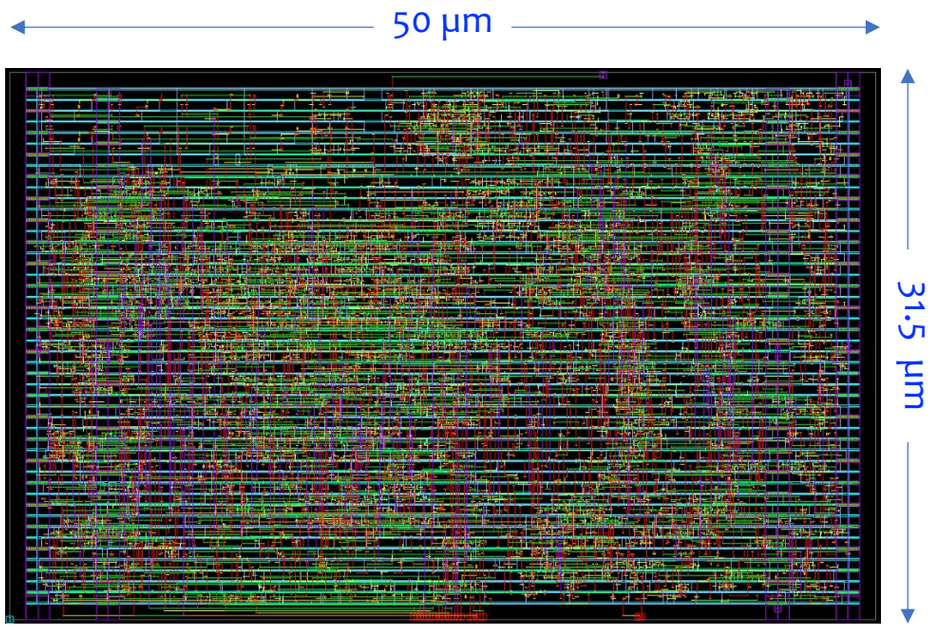
σ_{ej} vs sensor capacitance

High resolution – "low" consumption TDC

based on DCO and a Vernier architecture

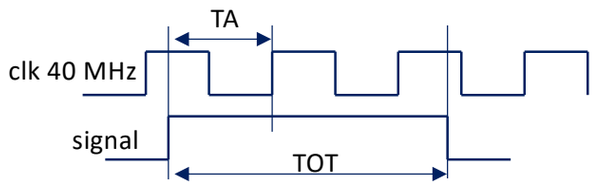
To maximize sustainable rate, **1 TDC per pixel channel** has been integrated

Maximum input signal TDC rate = 3 MHz
24 bits output word (ToA + ToT) serial @160 MHz



Time of Arrival

ToA	LSB [ps]	σ [ps]
MIN	6	2
TYP	12	3,74
MAX	12	4



Time over Threshold

TOT	LSB [ns]	Bits
MIN	0.75	8
TYP	1.10	8
MAX	1,18	8

The TDC gives the phase of the signal wrt the master 40MHz clock
The TDC and the counter use the same DCO-generated Clk (~1 GHz)

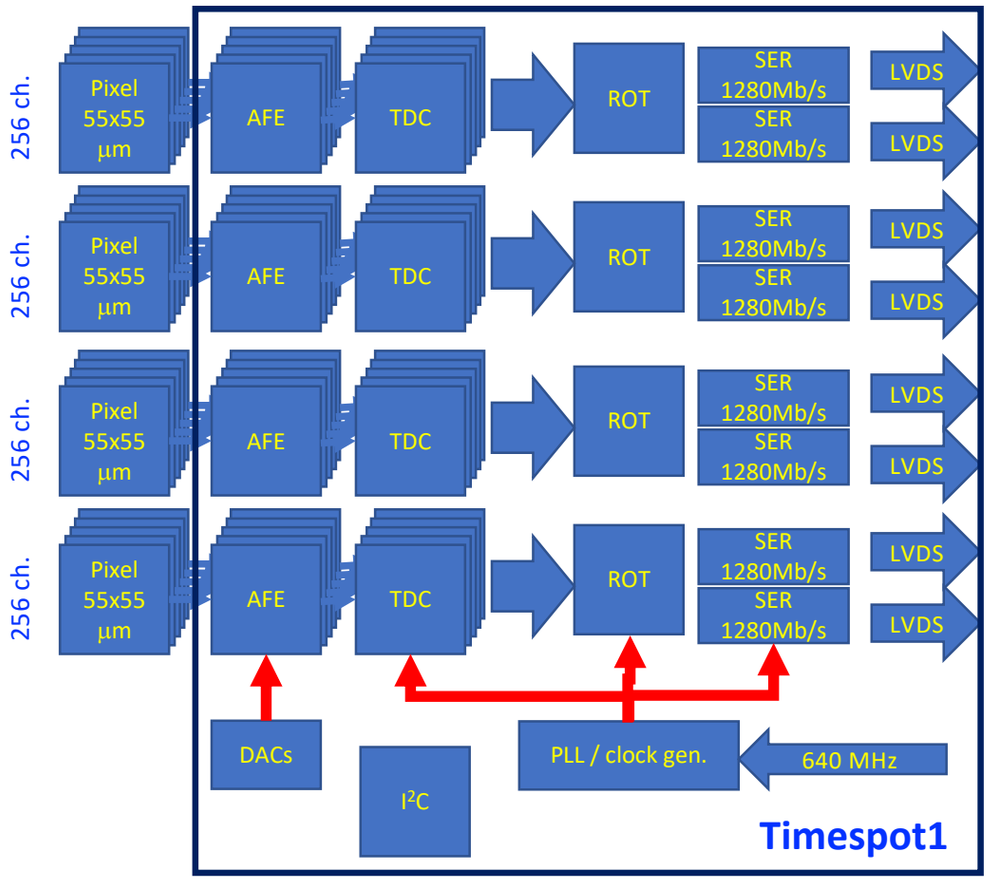
Power consumption

	Internal Pwr [µW]	Switch Pwr [µW]	Leak Pwr [µW]	Tot Pwr [µW]
IDLE	12.2	4.8	3.7	20.7
Calibration	338	211	3.7	552
DAQ 3MHz	101	69.5	3.6	175
DAQ 1MHz	40.4	25.3	3.7	69.3
DAQ 500kHz	26.6	15.2	3.7	45.5
DAQ 100kHz	15.1	6.9	3.7	25.7

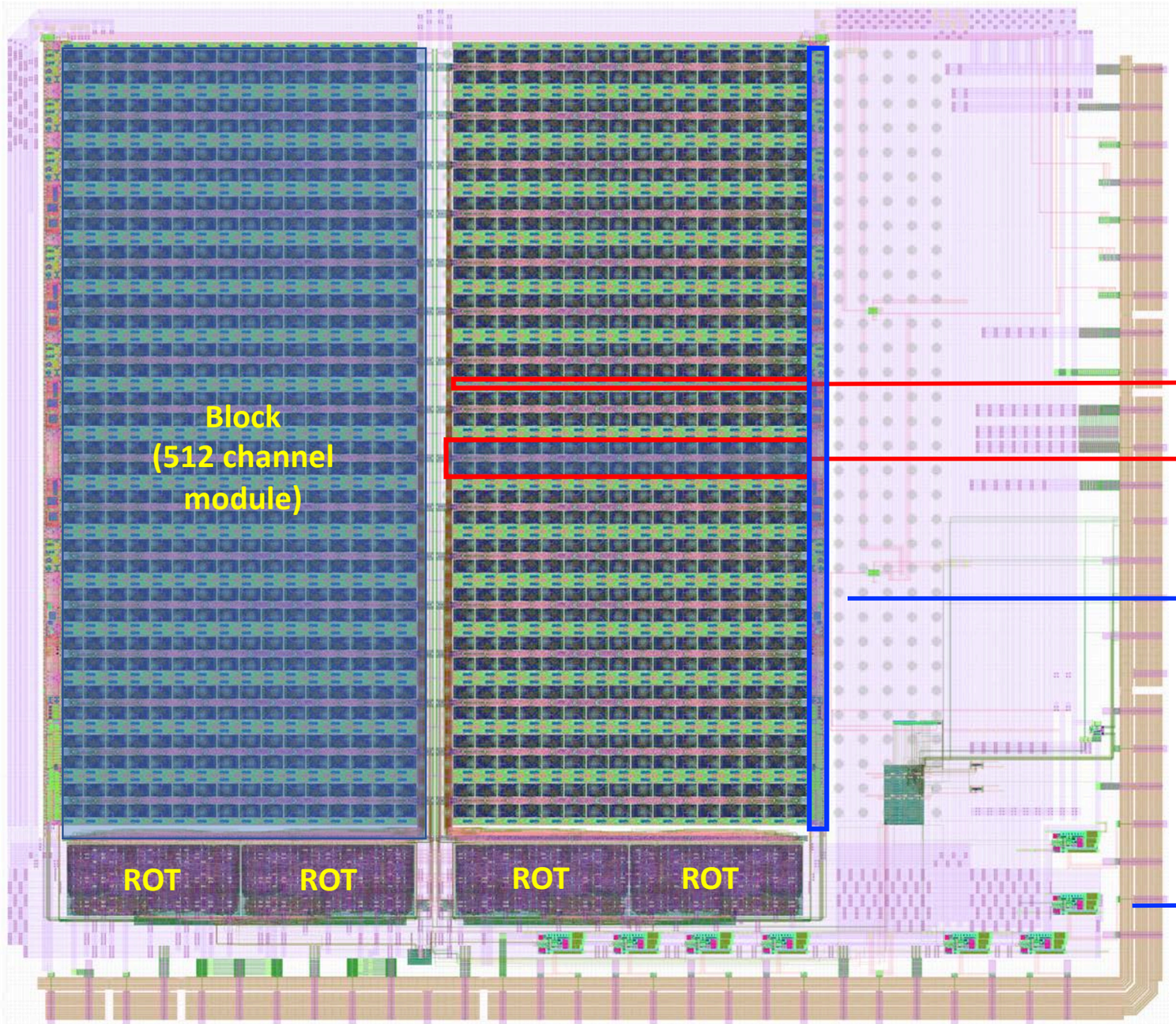
Timespot1 ASIC architecture

A prototype 28-nm CMOS ASIC

Reduced size with a full set of functionalities



- **1024 channels**, each equipped with Analog Front End and TDC
- A group of 256 channels is readout by a **ROT** (Read Out Tree) that addresses incoming data to 2 serializers that drive a LVDS driver each, sending data out **@1280Mb/s**
- There are 10 DACs giving Voltage references to the Front-End cells
- Different clock generator (**PLL and DCOs**) are implemented to give different clock sources for the circuit, with different jitter performances, to study the jitter influence on the time resolution
- All the chip is controlled/configured through **I²C** interfaces



Timespot1 ASIC
28-nm CMOS

Submitted mid October 2020,
Tests starting

INFN Cagliari, Milano, Torino
(Bergamo: LVDS drivers)

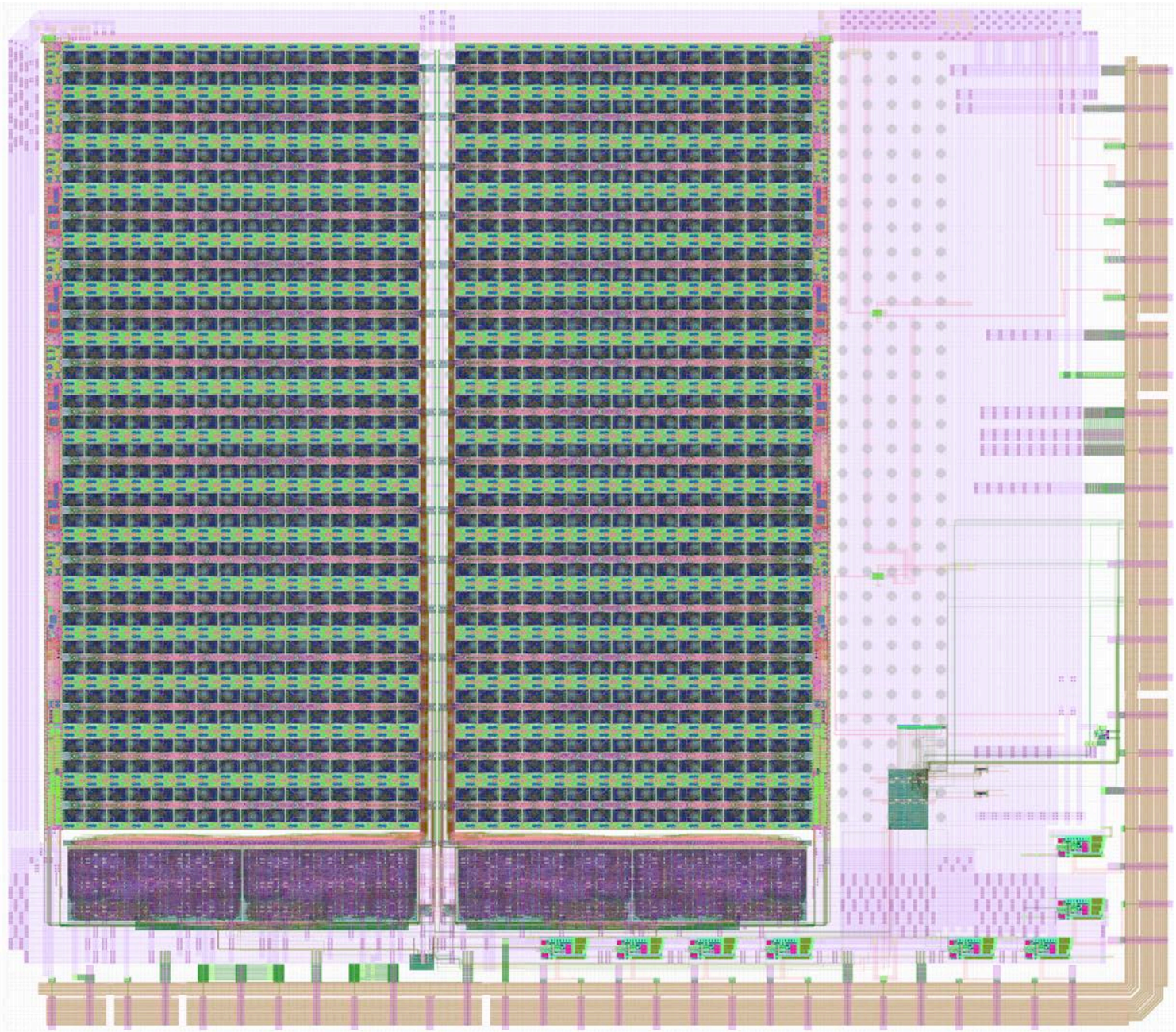
Analog row (16x2 AFE)

Digital row: 16x2 TDC + Controls, Conf. registers, I²C I/F)

Analog (service) column:

- 1 BandGap
- 5 DAC sigma-delta (producing analog levels used by pixels)
- Programmable bias cell (for power consumption)
- bias replicas with source followers.

LVDS driver



Timespot1 ASIC
Main characteristics

6 mm² – MPW run. Sensing area ~3 mm². 52 pins (staggered)

32x32 pixels. Pitch 55 µm (Timepix compatible). **Modular extendable architecture**

Each pixel integrates the Analog F/E (50x15 µm²) and 1 TDC (50x31.5 µm²)

Full chain σ_t **< 15 ps** (after layout)

The core matrix is TSV-ready and 4-side buttable thanks to a RDL

Max pixel rate is 3 MHz

Max ASIC readout rate is 200 kHz @ 10.24 Gbps (strongly output pad limited)

Power ≈ 45 µW/channel (<1.5 W/cm²)

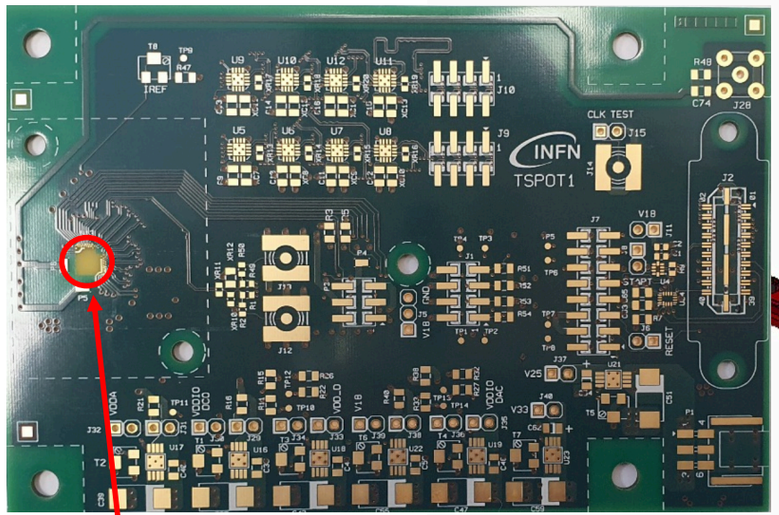
Towards the Timespotter®

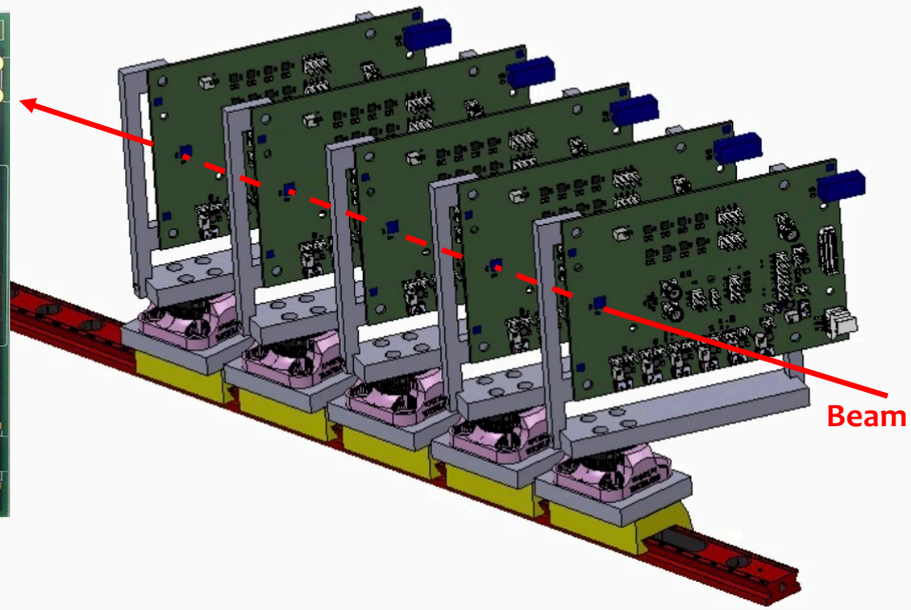
The final demonstrator

TS1-PCB characteristics

- 120x80 mm^2 size
- 640 MHz Clk. 4 options: external, internally generated x3 (useful for internal jitter measurements)
- 5 Separated supplies (D, A, IO, DCO, DAC)
- Hybrid supply up to 200 V
- Slow control by I^{2}C
- 8 buffered LVDS serial outputs
- Simplified readout protocol and data format:
  - IDLE byte (AB = 10101011)
  - START byte (E5 = 11100101) +
  - 5 DATA bytes

Conceived for both ASIC tests and the demonstrator setup with the hybrid on-top





1. **In our case the mechanics will be largely simplified, mainly using COTS components (e.g. Thorlabs).**
2. **Under evaluation: *a*) inclusion of an external time reference; *b*) cooling box.**
3. **Foreseen also (backup/complementary solutions): Timepix4* readout, 8x80 strips (see slide 31).**

**ready for bonding @IZM*