Novel silicon detectors: monolithic and 3D vertically integrated pixel sensors

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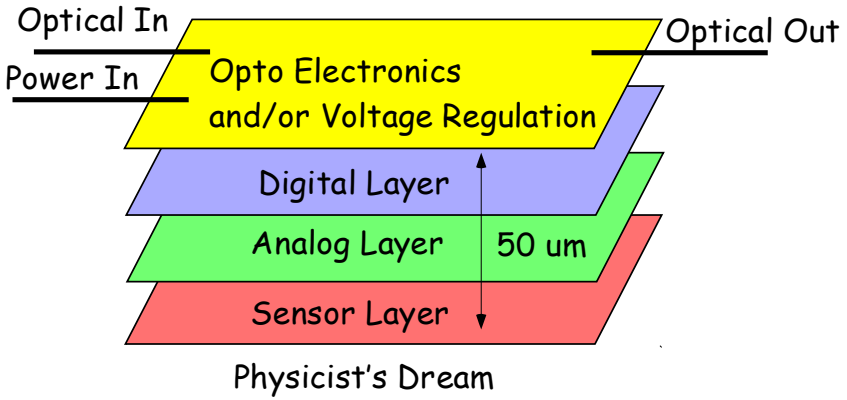
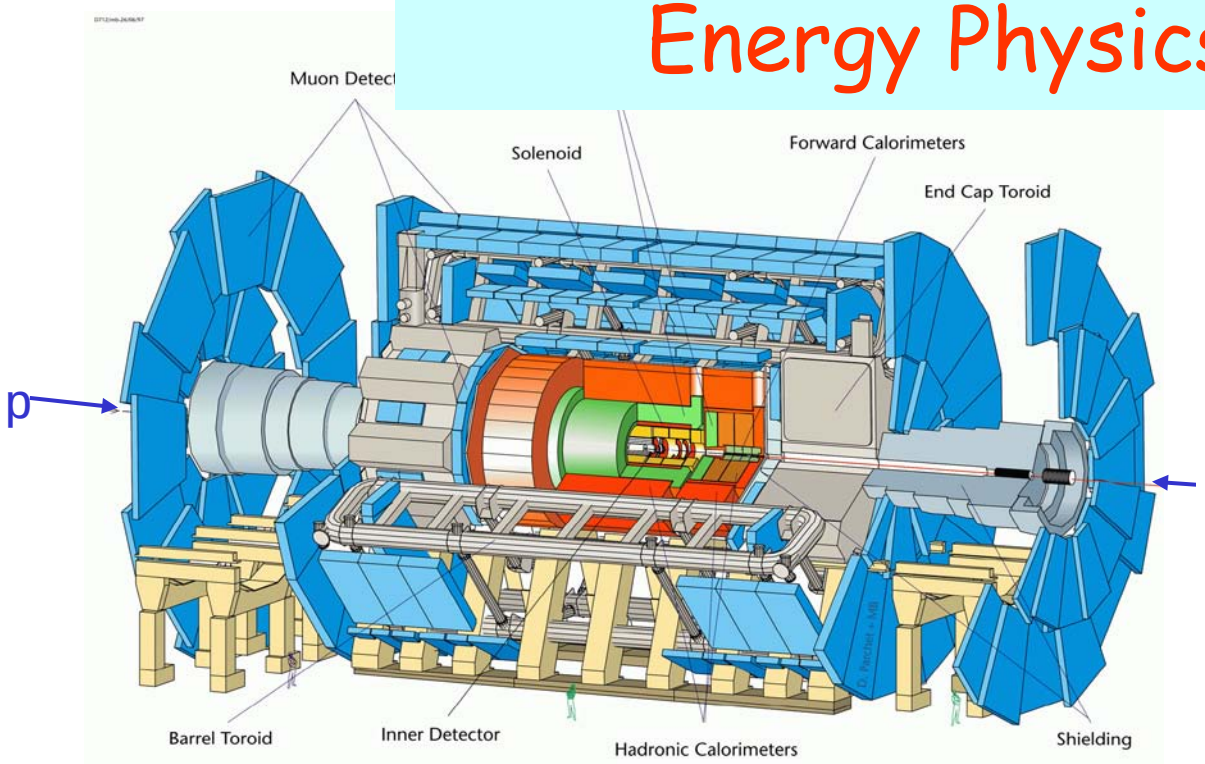
Outline

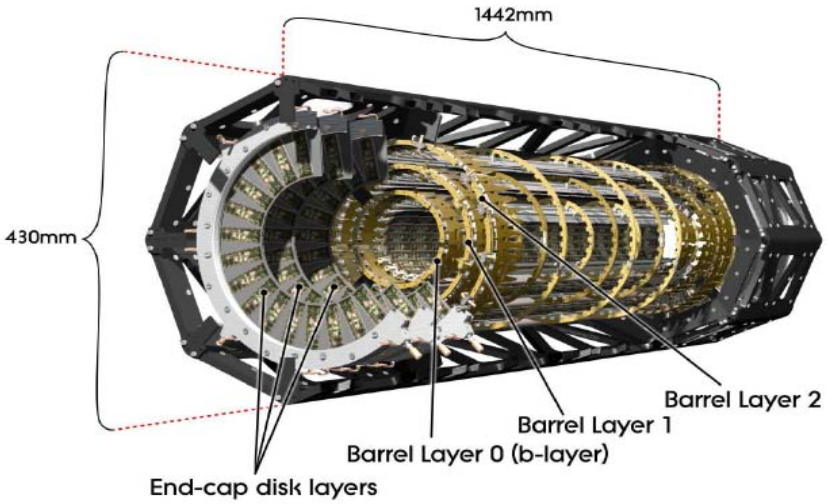
- **Pixel sensors in modern experimental applications:**
  - silicon vertex trackers in high energy physics experiments
  - high resolution imagers at advanced X-ray sources
  - …
- **Exploiting the most recent advances in microelectronics and interconnection techniques:**

  meet demanding specifications (low material budget, high resolution, high data rate capabilities and the generation of a track trigger with low latency)



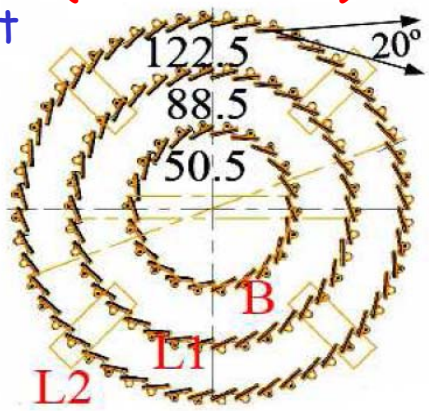
Silicon pixel detectors in High Energy Physics (HEP)



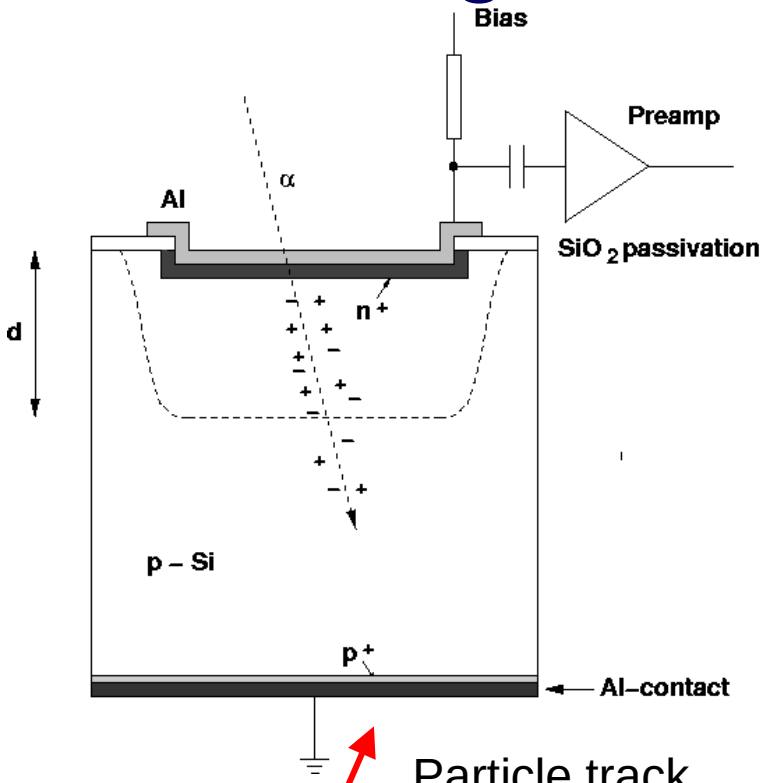


- Detection of charged particles generated in high energy collisions of accelerated proton beams (e.g. LHC - Large Hadron Collider facility at CERN, Geneva)
- Measurement of particle tracks as close as possible to the beam interaction point
- High granularity (80 Mpixels) and high data rate capability (hit rate ~ 50 MHz/cm^2) are necessary to detect multiple tracks with good space and time resolution
- Radiation hardness is also necessary to operate close to beams

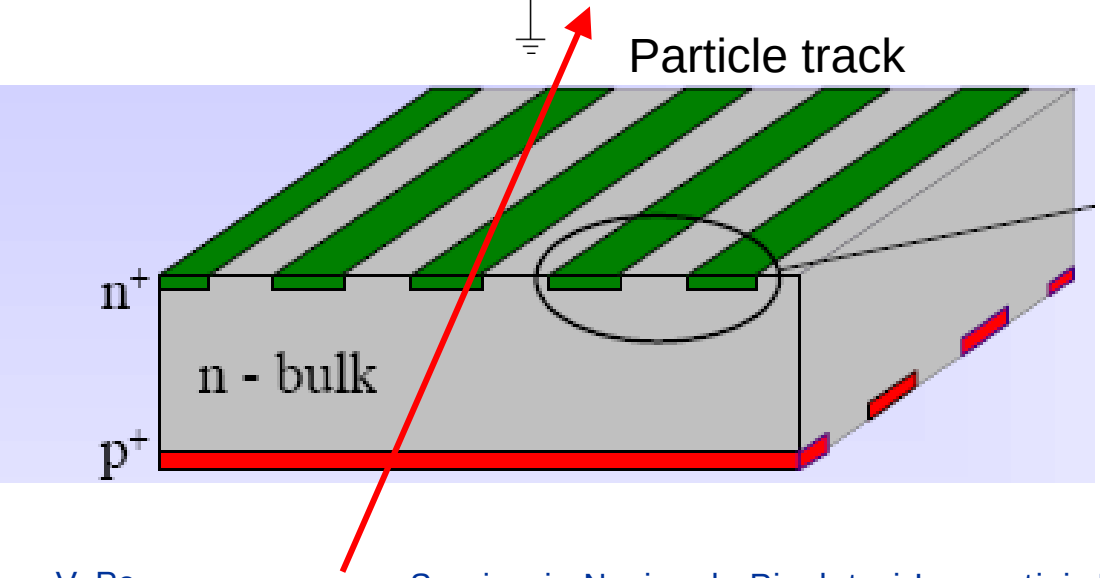
Barrel layers cross section (radii in mm)



From a single semiconductor sensor…



Ionization sensor converts the energy deposited by a particle to an electrical signal. In a fully-depleted semiconductor sensor, electron-hole pairs are swept to electrodes by an electric field, inducing an electrical current.



Position-sensitive detector:

Information about the coordinates of the interaction point in a segmented region (presence of a hit, amplitude measurement, timing)

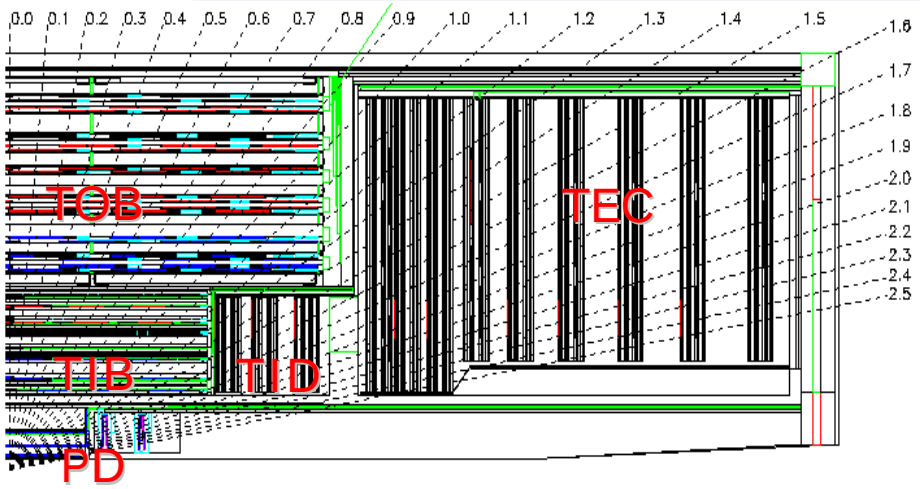
(single-sided or double-sided strip detector, pixel sensors)

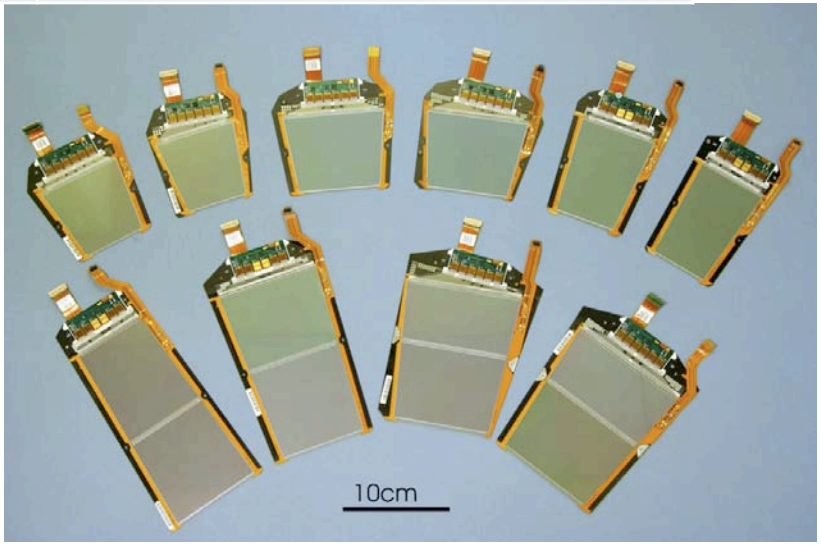
…to a full Tracker system (e.g., CMS)

- Two main sub-systems: Silicon Strip Tracker and Pixels
  - pixels quickly removable for beam-pipe bake-out or replacement

Microstrip tracker	Pixels
~210 m^2 of silicon, 9.3M channels	~1 m^2 of silicon, 66M channels
73k APV25s, 38k optical links, 440 FEDs	16k ROCs, 2k olinks, 40 FEDs
27 module types	8 module types
~34kW	~3.6kW (post-rad)

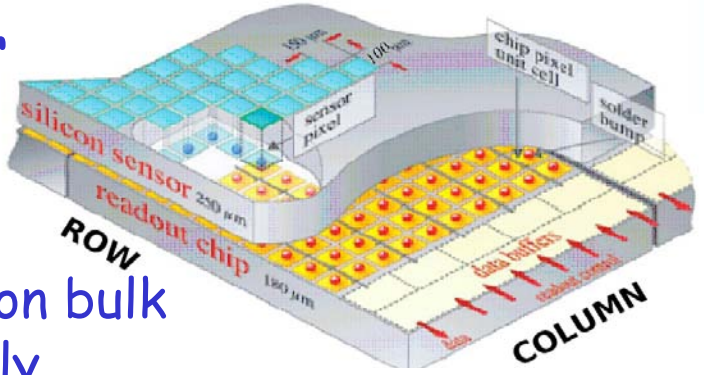
Geoff Hall, TIPP09

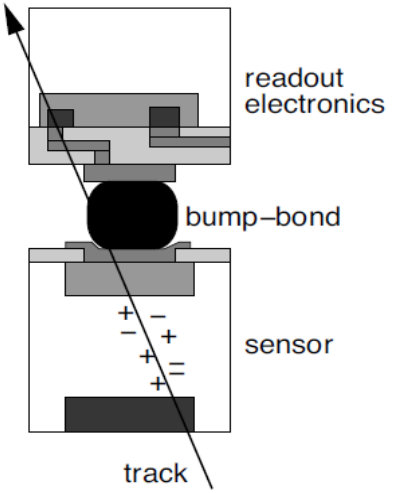


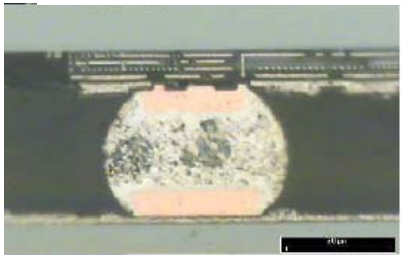


A mature technology: hybrid pixel sensors

- A pixellated sensor chip is connected to a matching readout chip by an array of solder bumps
- Sensors
  - Particle sensitive volume is a high resistivity silicon bulk (1-10 kΩcm, 250 μm typical thickness), can be fully depleted for fast charge collection by drift
  - Typical pixel dimensions: 50 μm × 400 μm
  - Radiation-hard to 50 MRad
- Front-end chips (Deep submicron CMOS)
  - For any event (particle hit in the sensor) provide pixel position, timing, pulse amplitude
  - Only a small number of pixels are hit in any event
  - Analog pre-amplification, discrimination, time stamping, digitization, zero suppression (sparsification)…





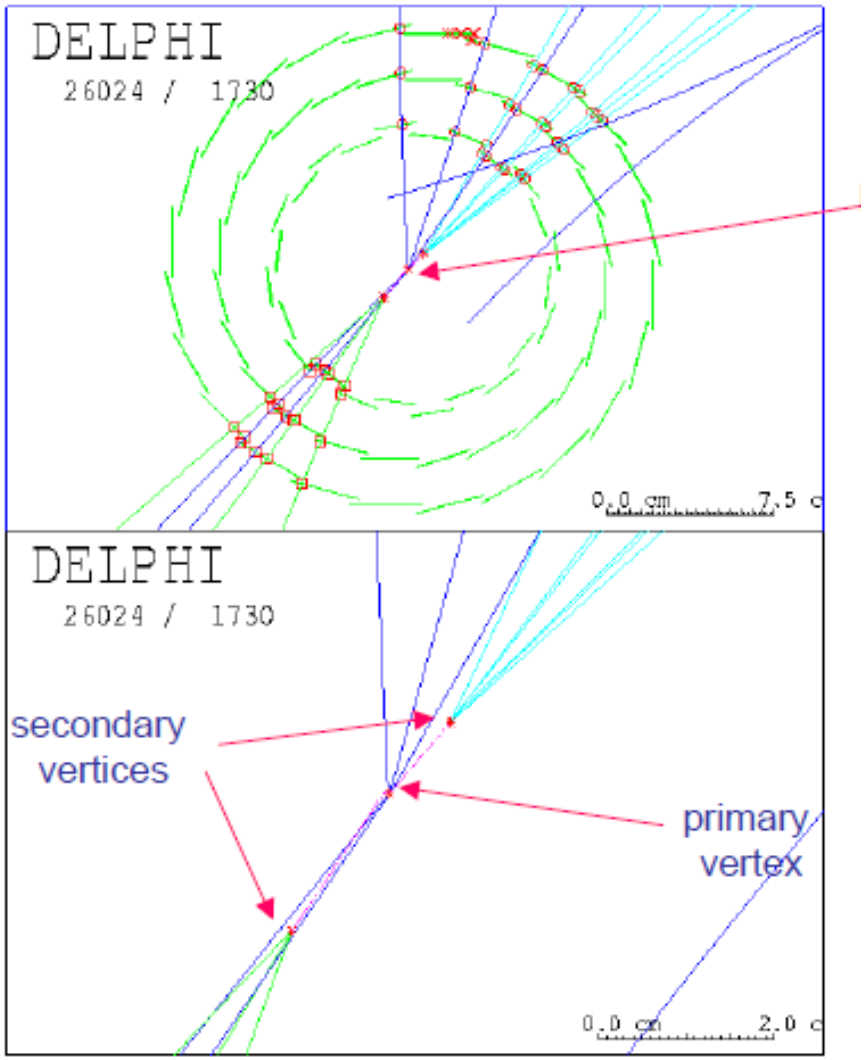


Physics defines the detectors: e.g., LHC

- High luminosity is required of the LHC to have sufficient statistical power in studying terascale physics
- This means that the detectors will be exposed to high particle rates.
- LHC experiments required fast, radiation-hard and finely segmented detectors.
- The detectors can be operated at a speed which can resolve the time between two successive r.f. bunches, which is 25 ns

The Vertex Detector in collider experiments

- Measures secondary decay vertices, has to be as near to the beam pipe as possible
- Silicon pixels for an unambiguous two-dimensional information , low occupation probability (ideal location to start finding track patterns) at the cost of the independent readout of many pixels
- Trade off in radius between number and size of pixels and the radiation field.

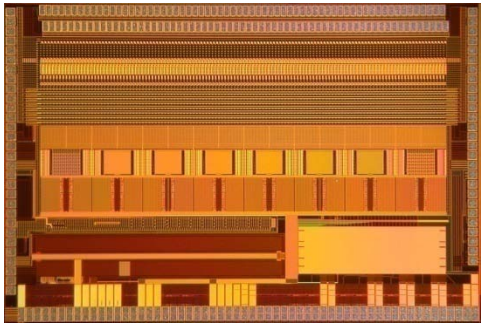


Pixel Detectors for Vertexing

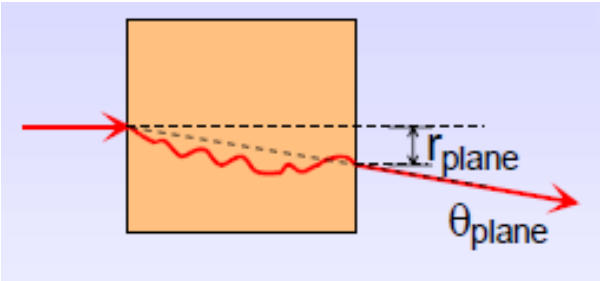
- Sensor electrodes are connected to a matching array of readout electronics via an array of contacts
- Pixel size can be limited by the area required by each electronic readout cell
- Detector segmentation reduces the rate per readout channel and aids distinguishing multiple tracks emitted simulatneously in a small solid angle (jets)
- Improves radiation resistance: less shot noise from detector leakage current (proportional to electrode area), less series noise because of smaller electrode capacitance allows a greater signal degradation from detector damage
- Power is roughly independent of segmentation (scales with the square of capacitance)

Not only the sensor but the whole system matters

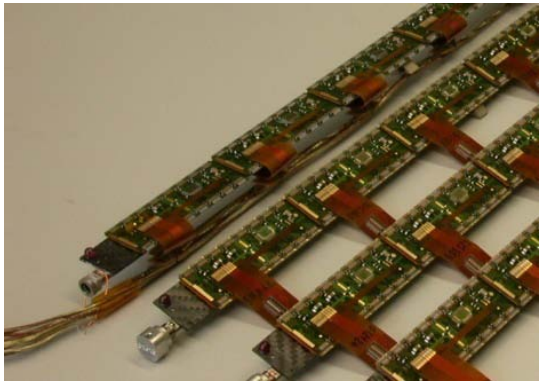
- A high resolution detector implies a high density readout electronics



- Vertex resolution is affected by angular deflection due to multiple scattering from material in the detector volume

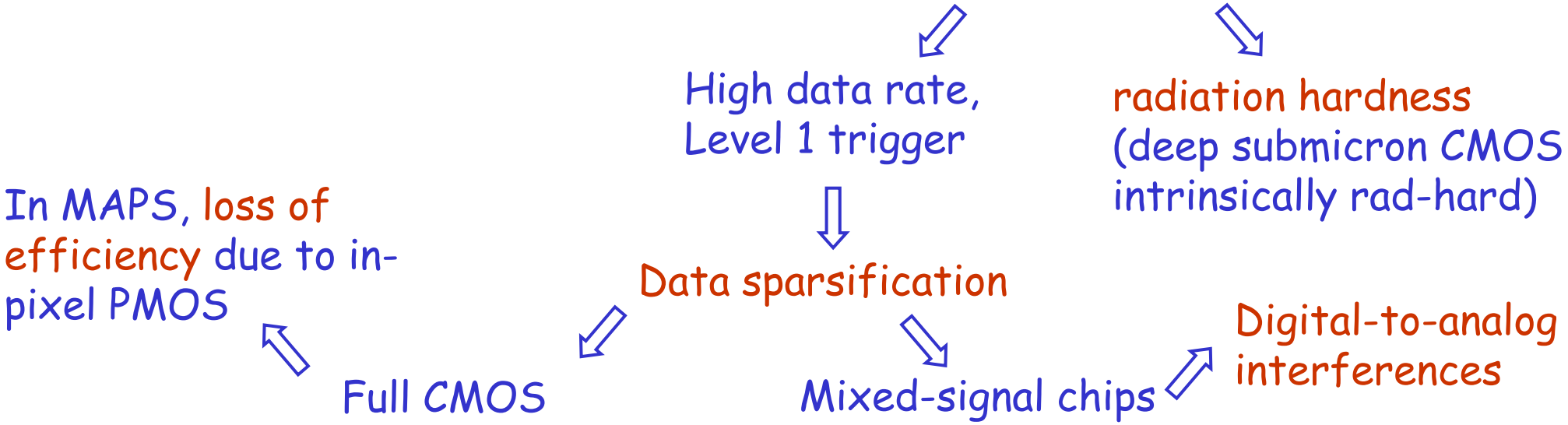


- Material constraints on sensor, electronics, support structures, cooling system, power cabling

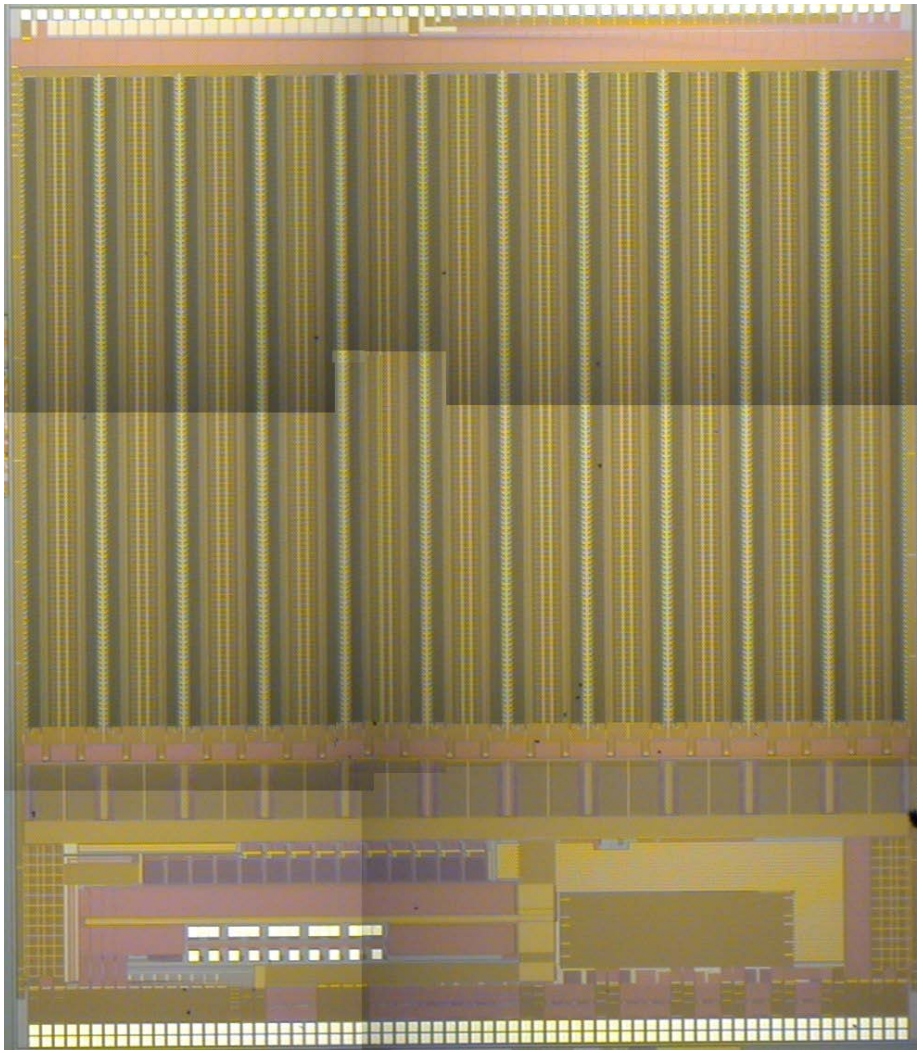


A wild bunch of requirements (often fighting each other…)

- High efficiency, low noise occupancy ⇒ high signal-to-noise ratio
- High granularity ⇒ small pixel pitch
- Low material budget ⇒ low mass cooling, thin silicon wafers, small amount of material for support and interconnections
- Small distance to interaction point ⇒ large background



FPIX2 Layout (Pixel readout chip)

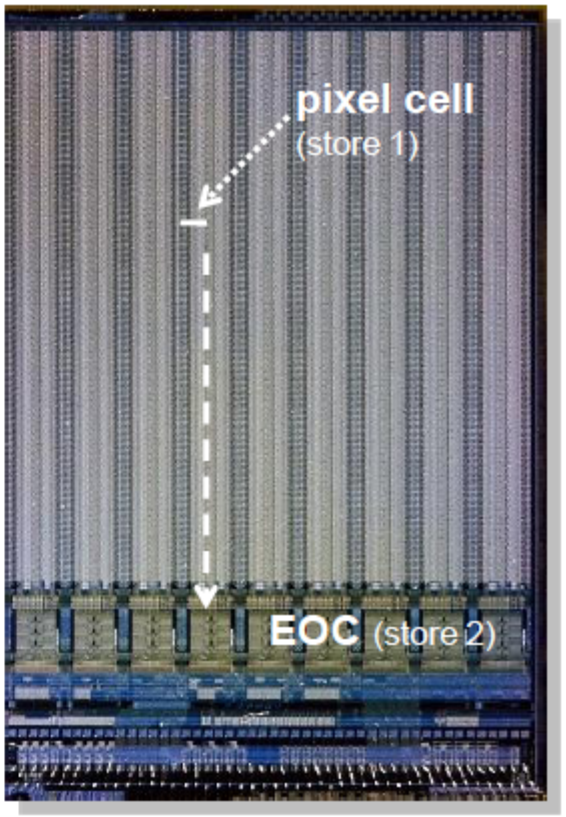


Principle of hybrid pixel detector readout

charge generation in sensor, integration in FE-chip

temporary on chip storage (digital or analog)
trigger driven readout of individual hits

- pn-diode → Q_{signal}
- amplification and filtering → V_{out}
- pixel-wise storage: address, charge, time (BX)
- column-wise R/O
- transfer information to End of Column (wait for trigger)

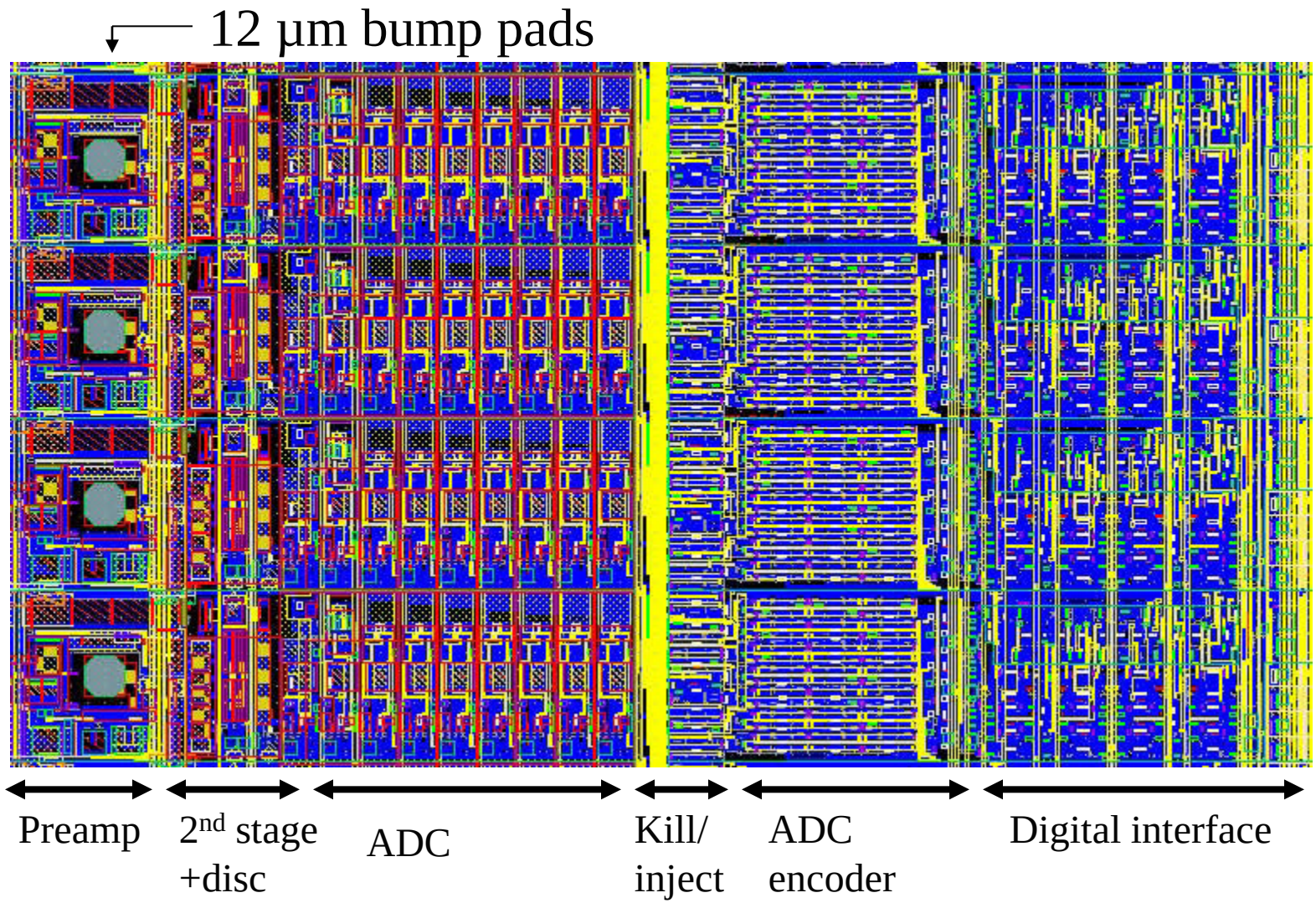


✓ high rate capability
✓ radiation hard to 10^{15} n_{eq}/cm^2
✓ mature technology

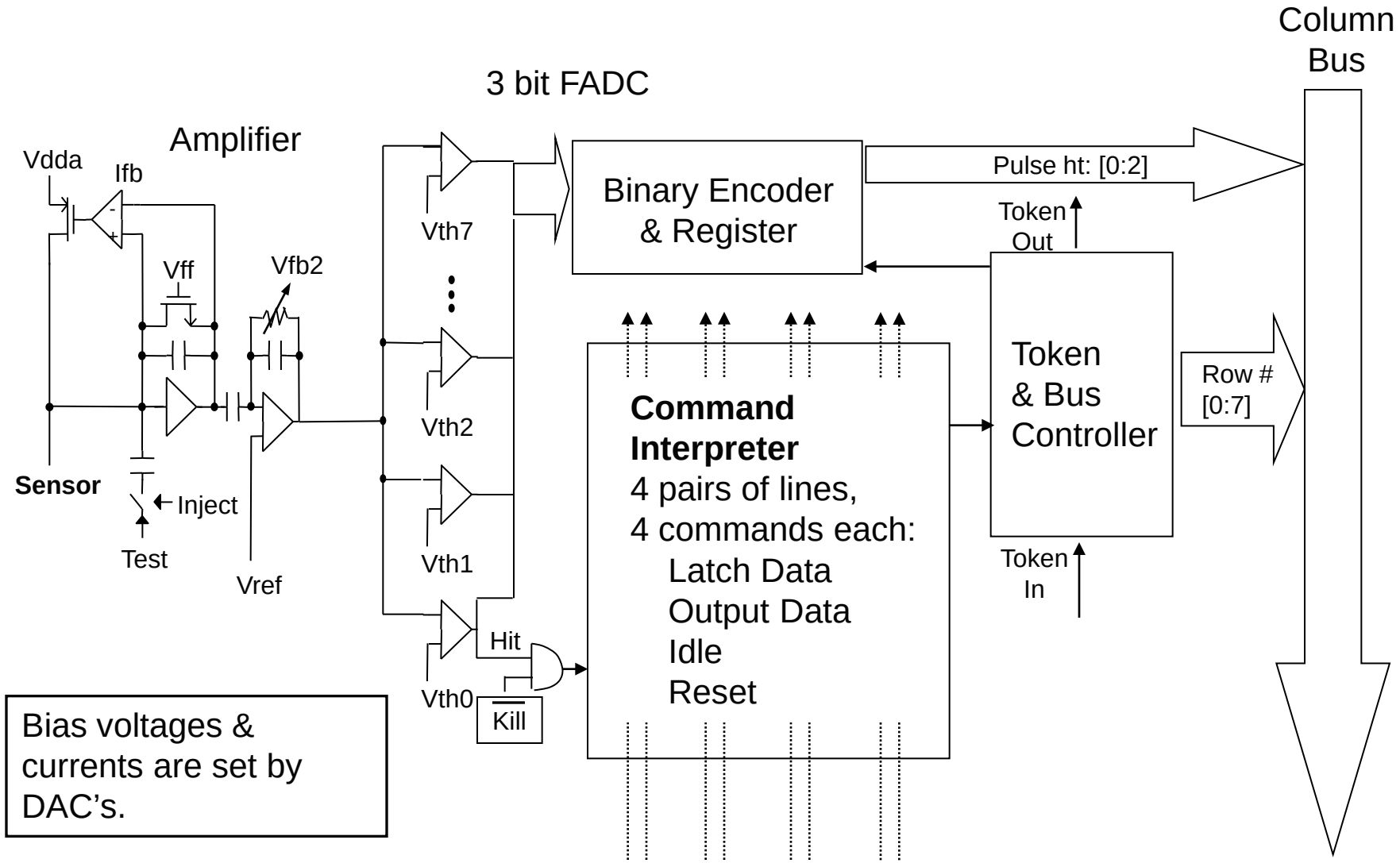
❖ comparatively massive (>3% X_0, mostly due to power and "overall size")
❖ resolution ~10 µm (pixels sizes 50x400 µm² or 100x150 µm²)

→ improve

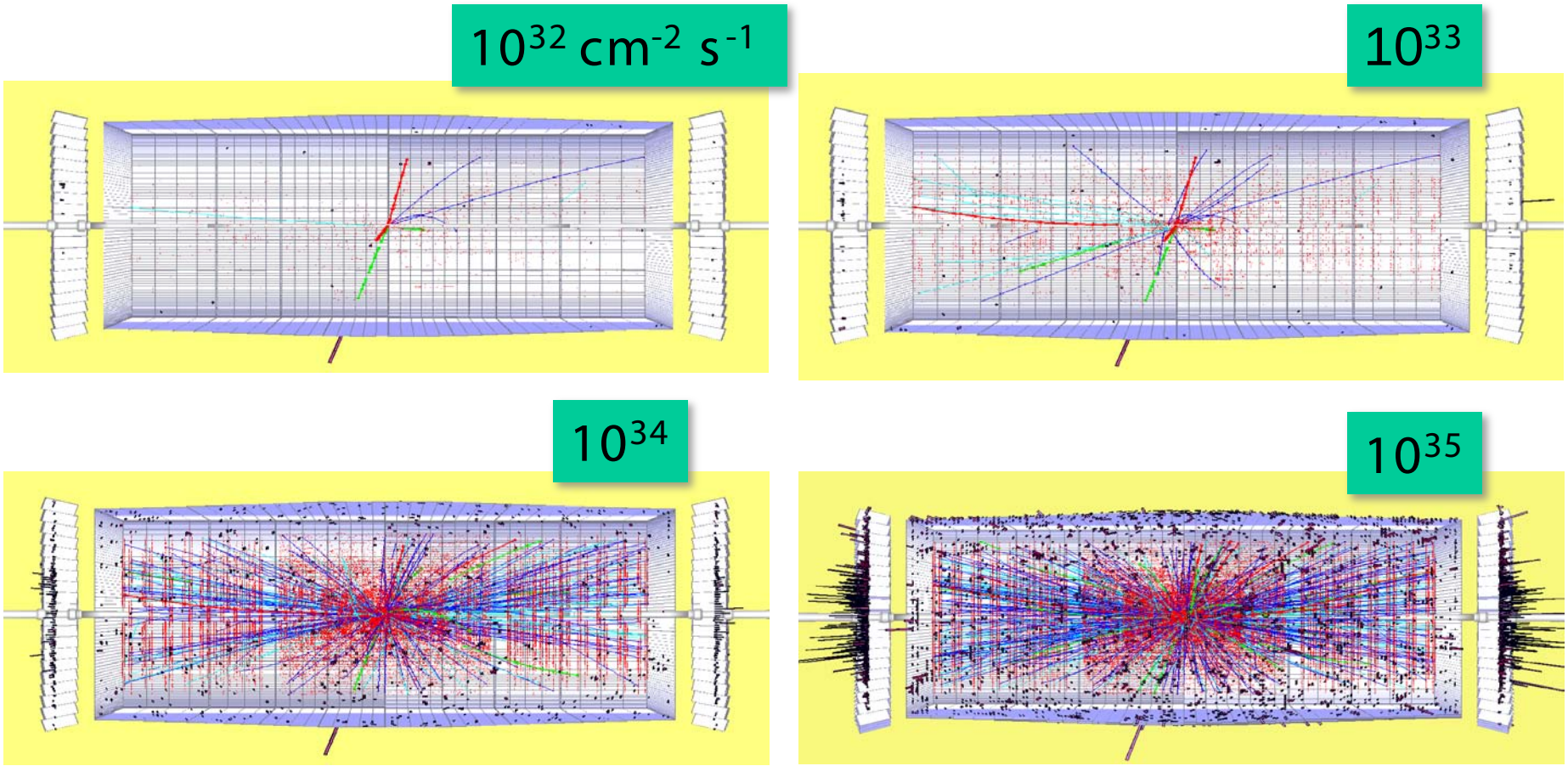
Pixel Cells (four 50 x 400 μm cells)



Pixel Unit Cell



From LHC to SLHC



Advancing the state of the art of pixel sensors for a next generation of HEP experiments

New demanding specifications for experiments at new machines (Super LHC, International Linear Collider, Super B-Factories)

- **Improve resolution ⇒ shrink pixel size and pitch**, down to 20 μm or even less

  presently limited to 50 μm by bump bonding technology

- **Preserve or even increase pixel-level electronic functions**

  handling of high data rates (hit rates > 10 MHz/mm^2), analog-to digital conversion, sparsification,…: presently this also contributes to limiting the minimum size of pixel readout cells

- **Decrease amount of material ⇒ thin sensor and electronics** chips, "zero mass" cooling

  Necessary to reduce errors in track reconstruction due to multiple scatterings of particles in the detector system

  50 -100 μm total thickness

Requirements of pixel sensors in future High Energy Physics experiments

Depending on the application, some (or all!) of the following requirements must be taken into account:

- **Pixel pitch < 20 μm**
- **Timing resolution ~ 25 ns**
- **High radiation tolerance**: total ionizing dose > 100 Mrad, 10^{16} neutrons/cm^2
- **Sensor thickness < 50 μm** (0.1% X_0 per layer at ILC)
- **Noise: 10 – 100 electrons rms**

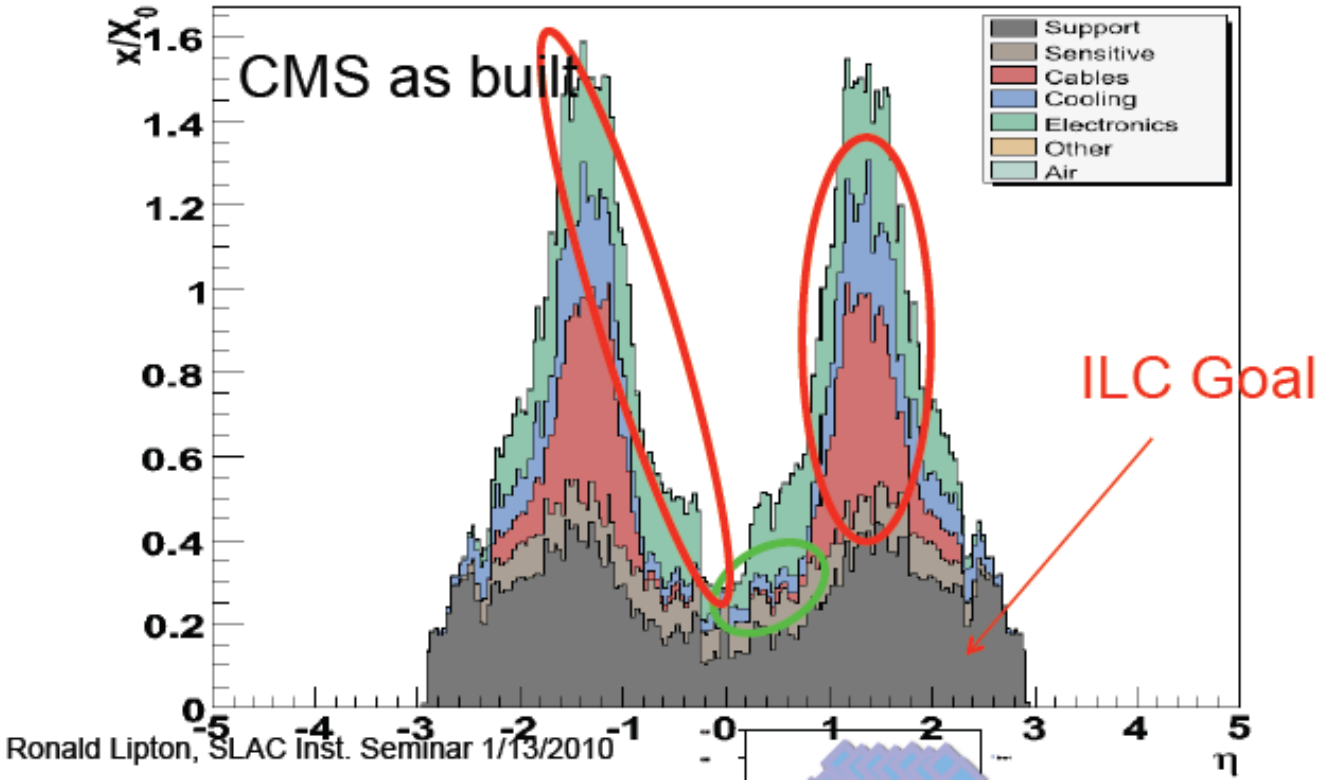
  S/N adequate to detection of small signals (few hundreds – few thousands electrons); signal ÷ thickness of active sensing layer; depends also on radiation-induced damage
- **Low power dissipation** (~ 100 μW/cm^2 average, may require power cycling)
- **Processing of events with very high rate**

  even with zero suppression, chip architectures with output data rates of 320 MHz; detector modules require data links with rate capability ~ 5 Gbps

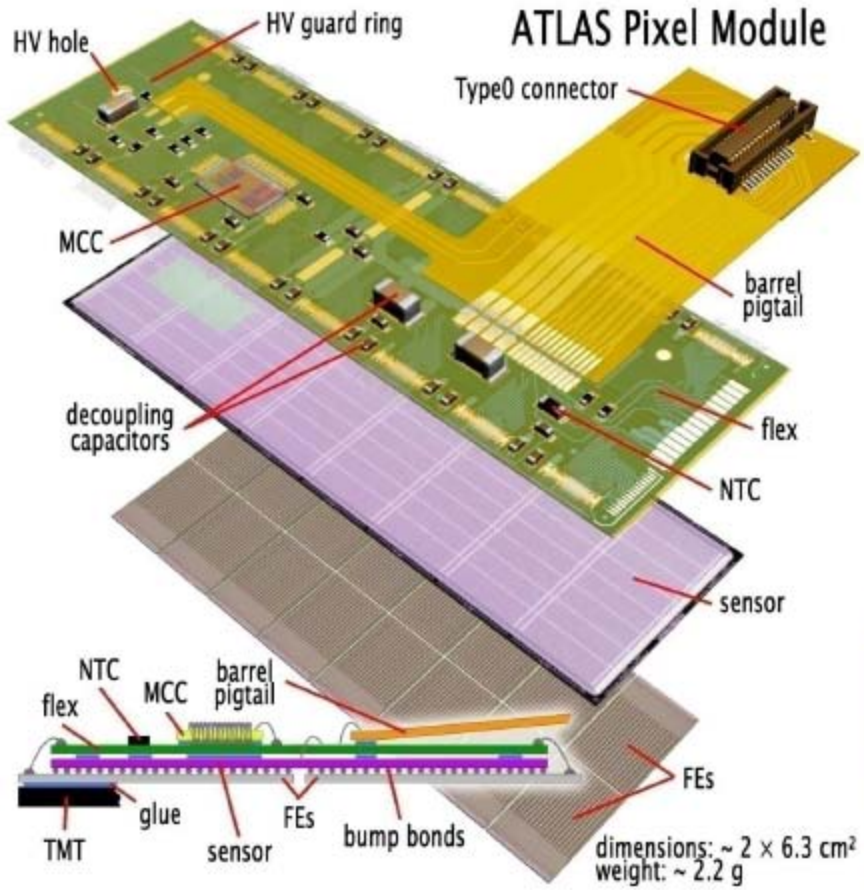
Detector Mass

Mass Drivers:

- Cooling and associated infrastructure – directly related to power dissipation and radiation damage which forces low temperature operation
- Supports
- Cables, interconnects and electronics

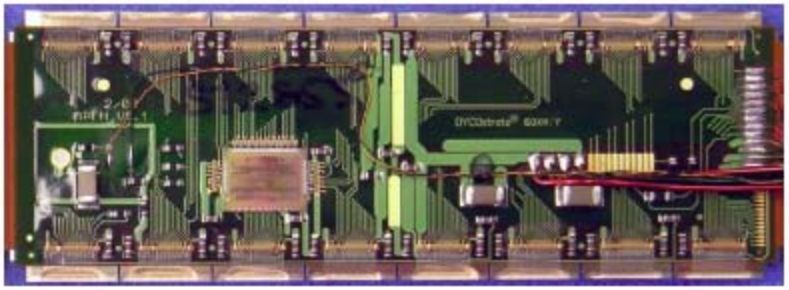


A Hybrid Pixel Detector Module



- module (1.1% X_0)
- supports & cables (2.4% X_0)

per layer



Rate and radiation challenges at the innermost pixel layer

High resistivity Pixels

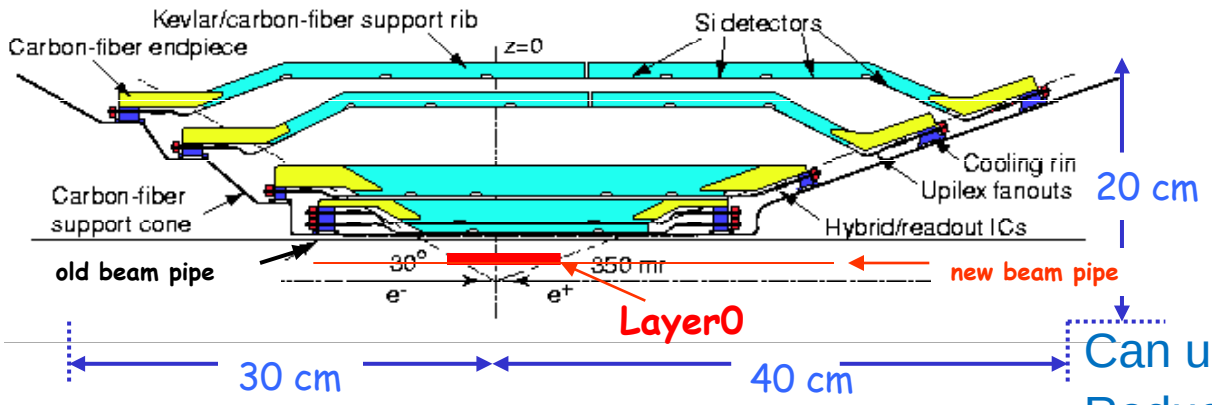
	BX time	Particle Rate	Fluence	Ion. Dose
	ns	kHz/mm^2	n_{eq}/cm^2 per lifetime*	kGy per lifetime*
LHC (10^{34} cm^{-2}s^{-1})	25	1000	1.0 x 10^{15}	790
sLHC (10^{35} cm^{-2}s^{-1})	25	10000	10^{16}	5000
SuperKEKB (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	50
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	4
RHIC (8x10^{27} cm^{-2}s^{-1})	110	3,8	1.5 x 10^{13}	8

Monolithic Pixels

lower rates
smaller pixels
less material

assumed lifetimes:
LHC, sLHC: 7 years
ILC: 10 years
others: 5 years

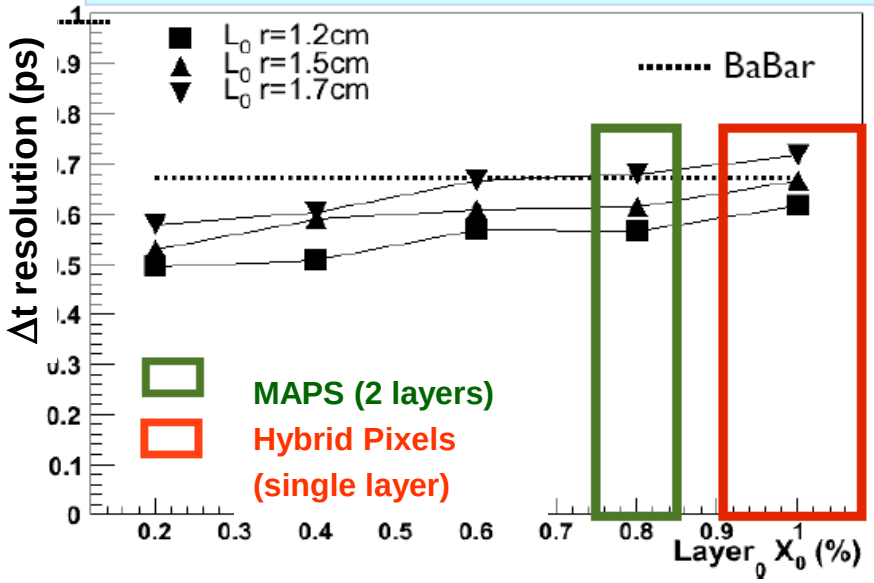
The SuperB Silicon Vertex Tracker



BaBar SVT

- 5 Layers of double-sided Si strip sensor
- Low-mass design. (P_t < 2.7 GeV)
- Stand-alone tracking for slow particles.
- 97% reconstruction efficiency
- Resolution ~15μm at normal incidence

B→π π decay mode, βγ=0.28, beam pipe X/X0=0.42%, hit resolution =10 μm



Can use Babar SVT design for R>3cm

Reduced beam energy asymmetry (7x4 GeV vs. 9x3.1 GeV) requires improved vertex resolution

- **Layer0 very close to the IP (R~ 1.5 cm) with low material budget**

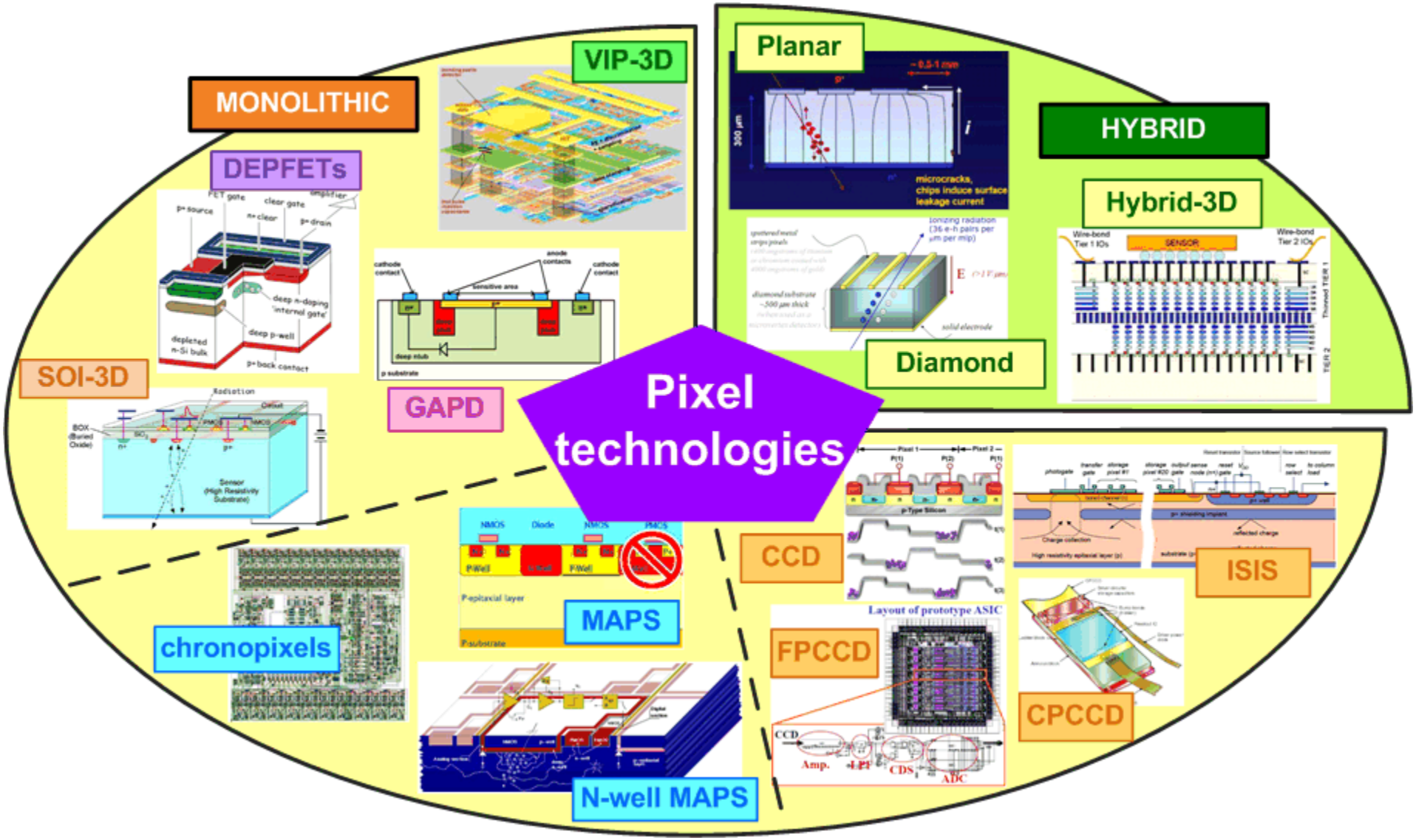
Background levels depends steeply on radius

- **Layer0 needs to have fine granularity and radiation tolerance**

- Layer0 subject to large background and needs to be extremely thin:

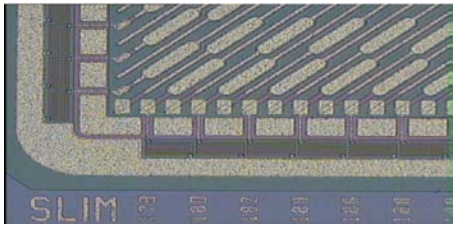
> 5MHz/cm², > 1MRad/yr, < 1 %X_0

The variety of pixel technologies

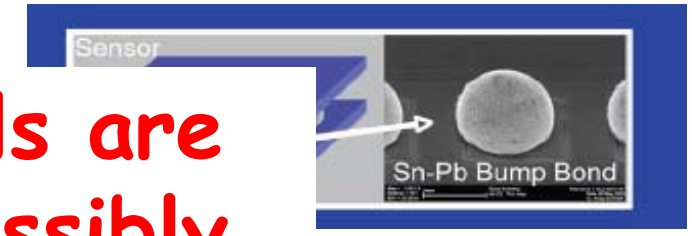


SuperB SVT Layer 0 technology options

- **Striplets option**: mature technology, not so robust against background.
  - Marginal with background rate higher than ~ 5 MHz/cm^2
  - Moderate R&D needed on module interconnection/mechanics/FE chip (FSSR2)

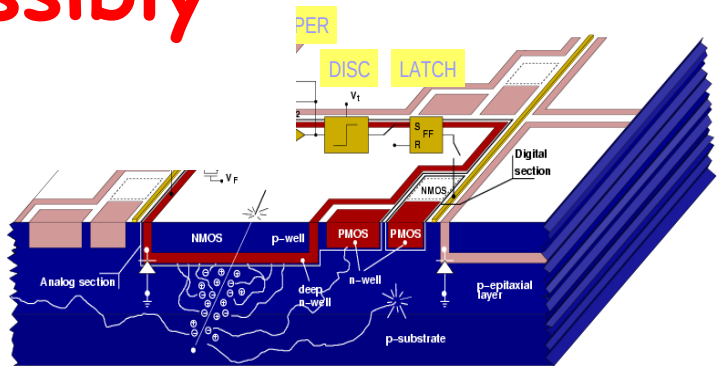


- **Hybrid Pixel Option**: viable, although marginal.

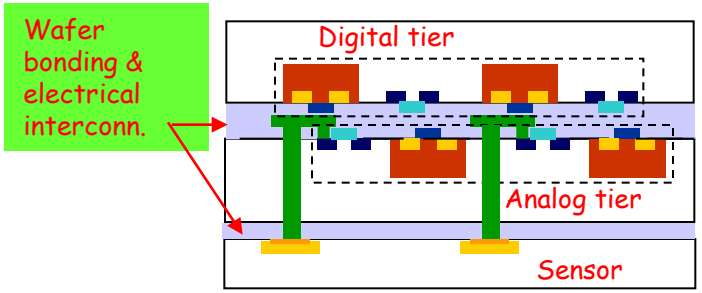


3D vertically integrated pixels are the most advanced option (possibly for an SVT upgrade):

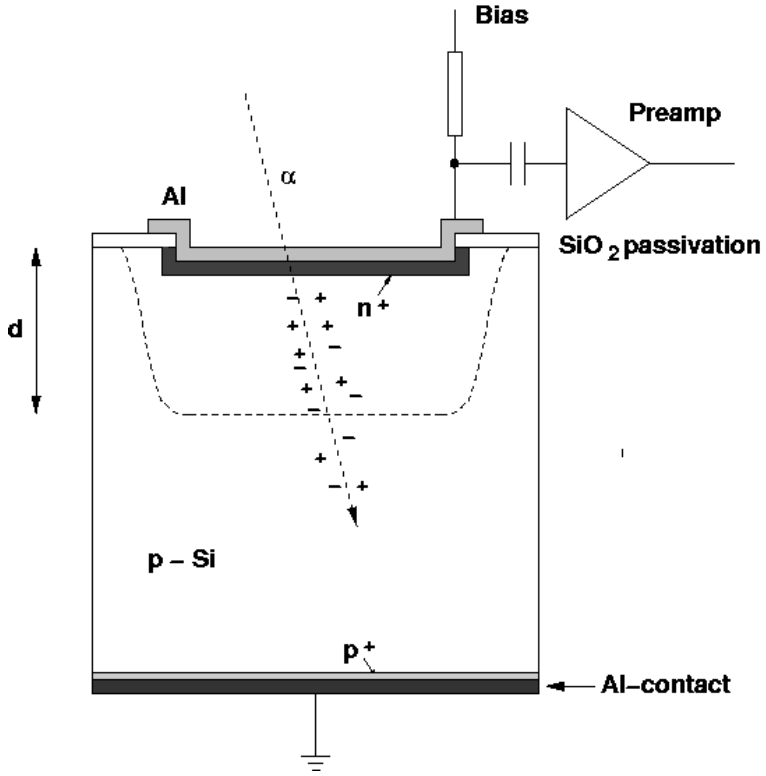
  - Extensive R&D (SLIM5 collaboration) on
    - Deep N-well devices 50x50μm^2 with in-pixel sp ification.
    - Fast readout architecture implemented
  - CMOS MAPS with 4k pixels successfully te ed with beams.



- **Thin pixels with Vertical Integration**:
  - Reduction of material and improved performance possible with the technology leap offered by vertical integration.
  - DNW MAPS with 2 tiers (Chartered/Tezzaron 130 nm) submitted in August 2009.



Combining semiconductor sensor technology with microelectronics

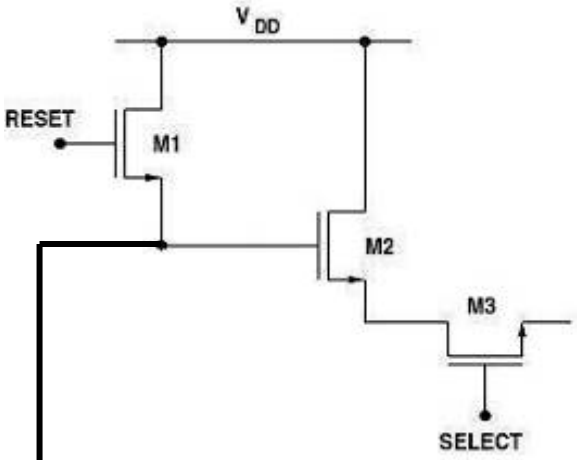


Ionization sensor converts the energy deposited by a particle to an electrical signal. In a fully-depleted semiconductor sensor, electron-hole pairs are swept to electrodes by an electric field, inducing an electrical current.

Charge collection by drift in high-resistivity silicon is much faster and less sensitive to radiation induced defects in the bulk as compared to the diffusion process that takes places in the low resistivity substrate of a CMOS chip

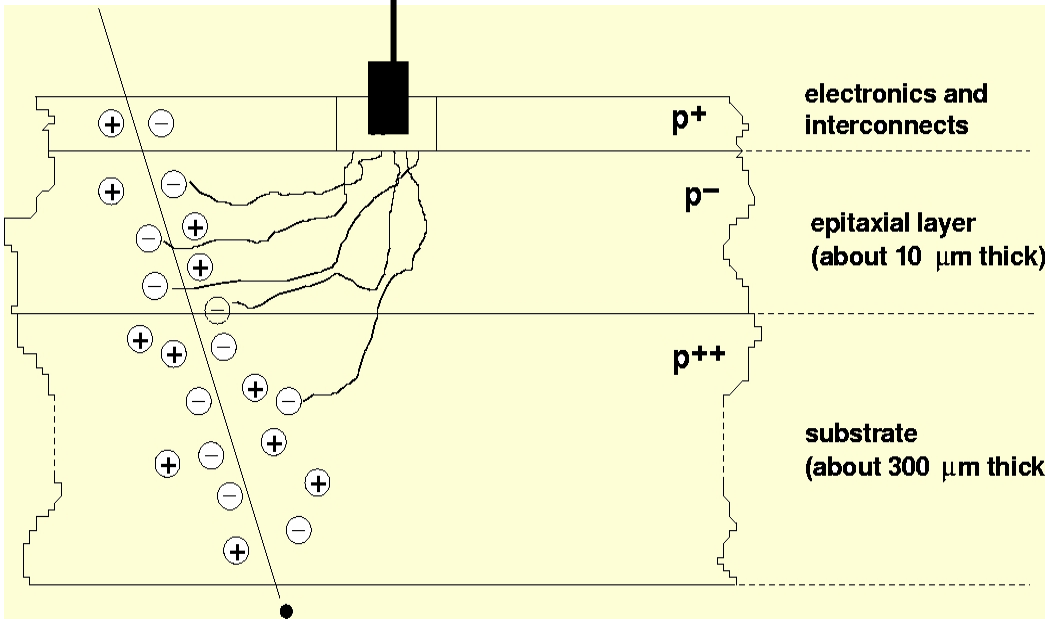
Using the substrate of a CMOS device as a sensing layer for ionizing particles

- Developed for imaging applications
- Several reasons make them very appealing as tracking devices :
  - detector & readout on the same substrate
  - wafer can be thinned down to few tens of μm
  - high functional density and versatility
  - low power consumption and fabrication costs



Principle of operation

- The undepleted epitaxial layer (or a non-epi substrate) acts as a potential well for electrons
- Signal (~1000 e-) collected through diffusion by the n-well contact
- Charge-to-voltage conversion provided by the sensor capacitance
  → small collecting electrode
- Simple in-pixel readout (PMOS not allowed)
  → sequential readout



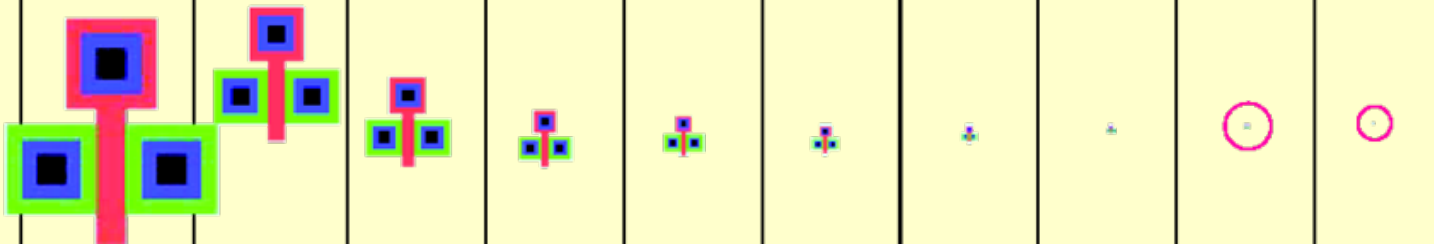
Exploiting advances in microelectronic technologies

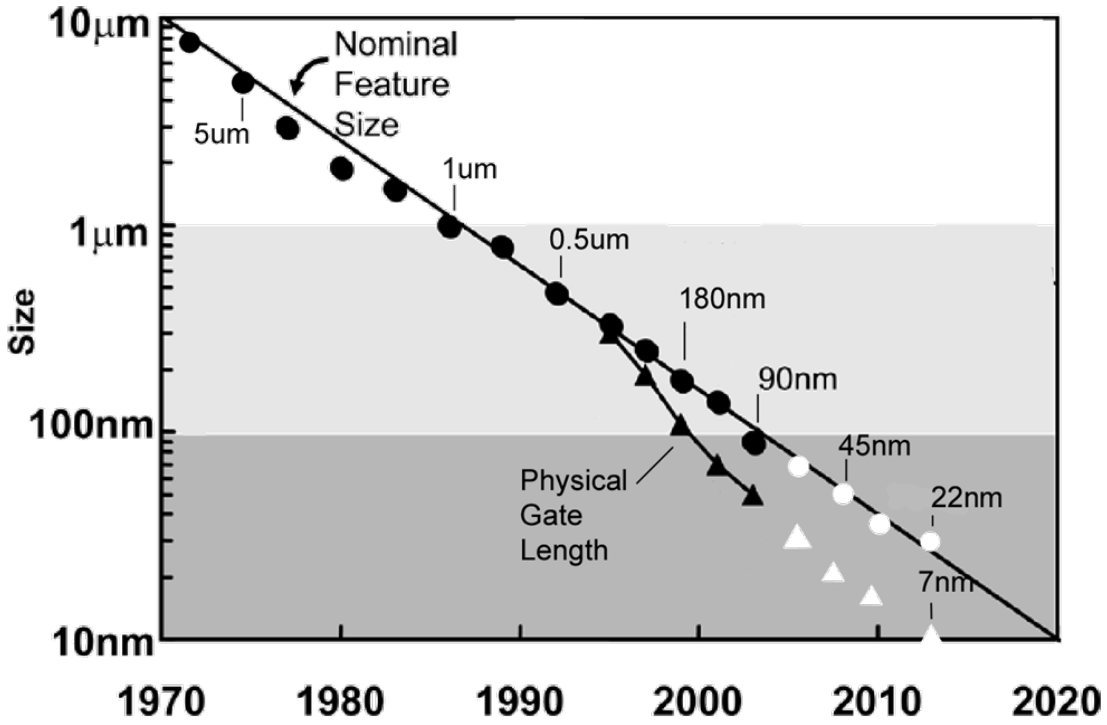
The big market of semiconductor industries is consumer electronics.

This has pushed towards very aggressive technology developments in both CMOS devices and interconnections.

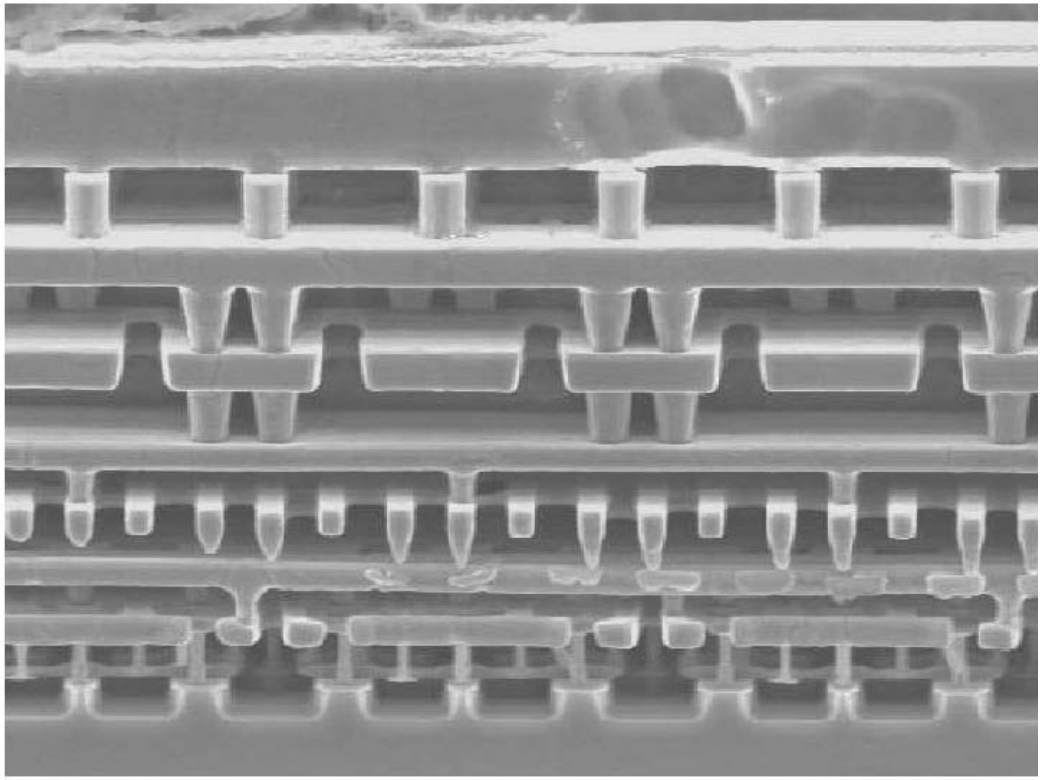
How advanced silicon vertex detectors can profit from this?

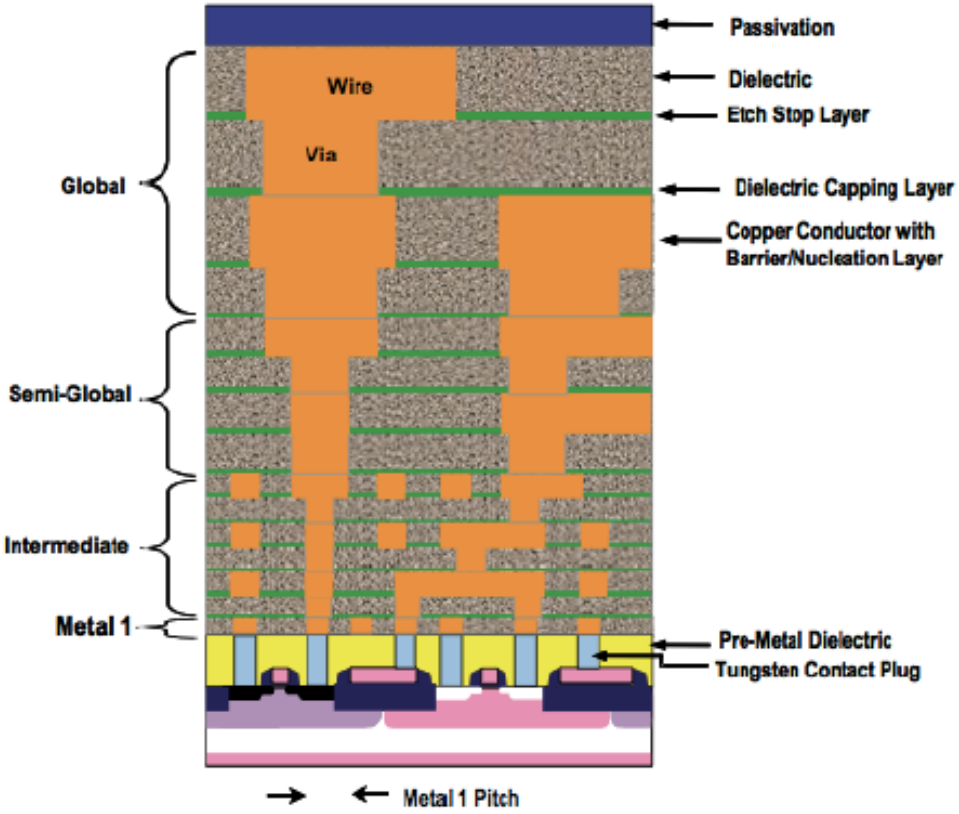
Industry Scaling Roadmap

Feature Size [nm]	2000	1200	800	500	350	250	130	65	35	20
Minimum NMOS										



Industry Scaling Roadmap: interconnections

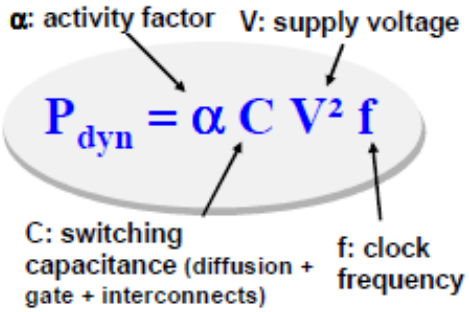




Challenges of advanced interconnects

• Today, More than 50% of dynamic power consumption is due to interconnects. This rate is projected to increase.

[Nir Magen et al, Proc. of the 2004 international workshop on System level interconnect prediction, France, pp 7-13, 2004]



• Global Interconnect length doesn't scale with transistors and local wires. Because of functionality increase, chip size remains relatively constant.

[Havemann et al., IEEE, Vol. 89 (5), May 2001]

• RC delay is increasing exponentially. For 65nm node, RC delay in 1mm global wire at minimum pitch is ~100 times higher than NMOSFET intrinsic delay [ITRS07].

[ITRS 2007]

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

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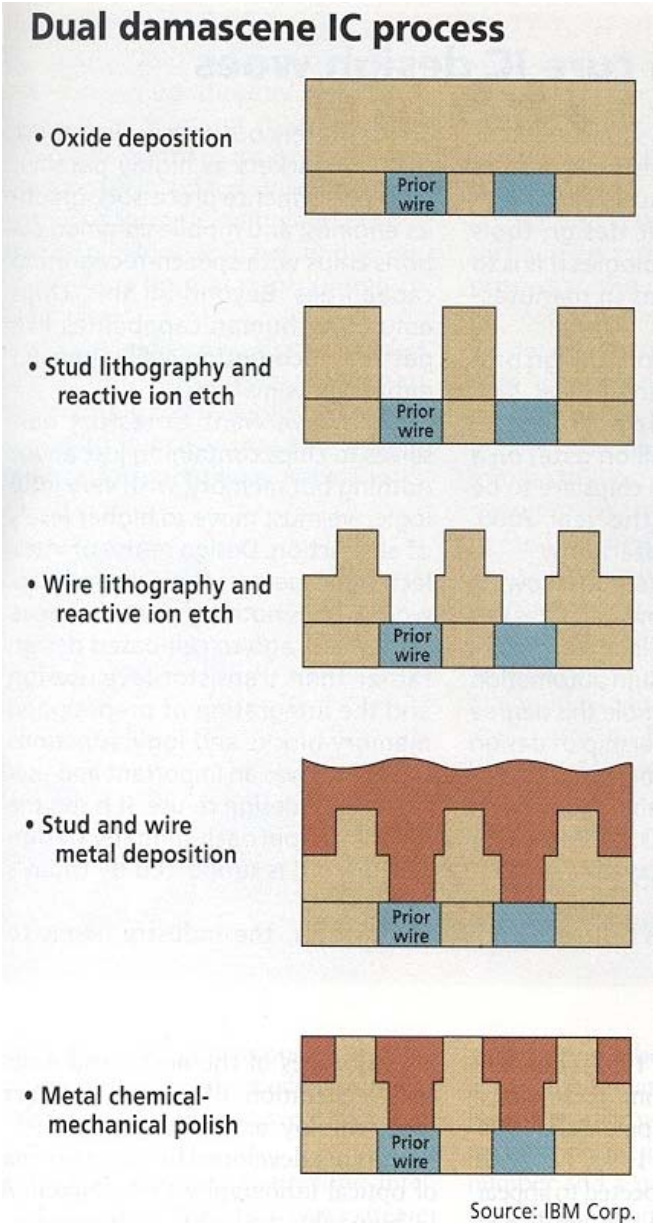
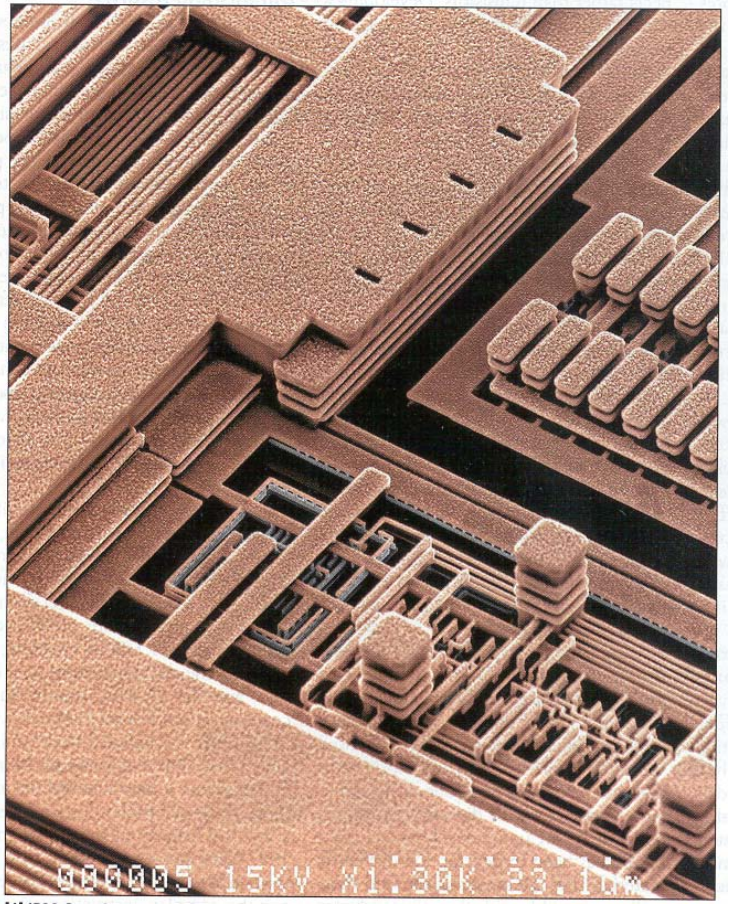
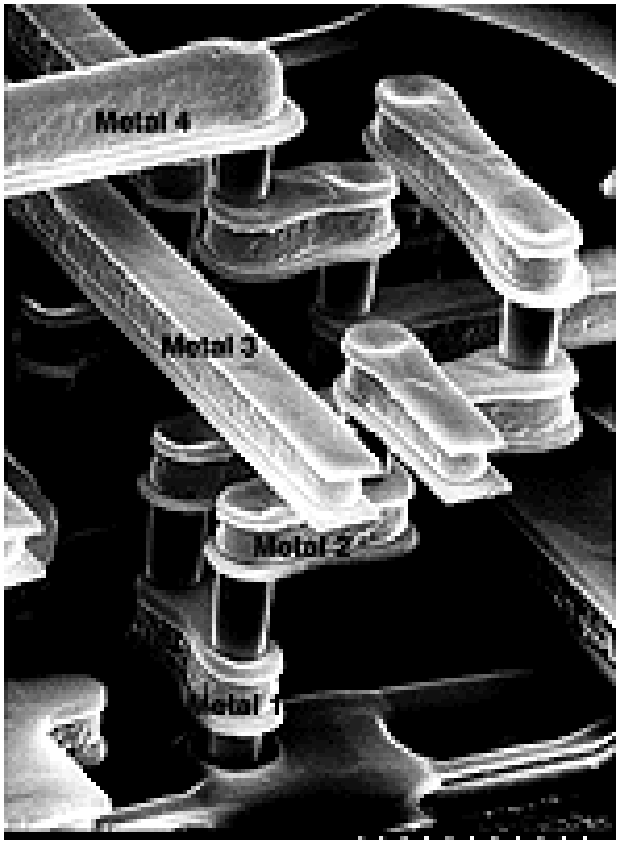
source: cea leti MINATEC

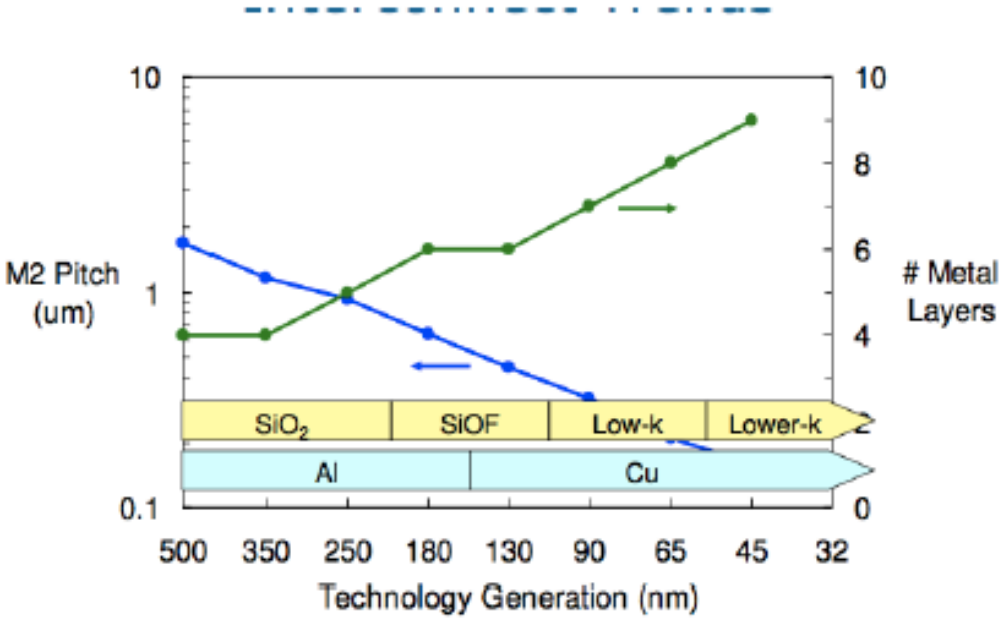
Advanced Metallization

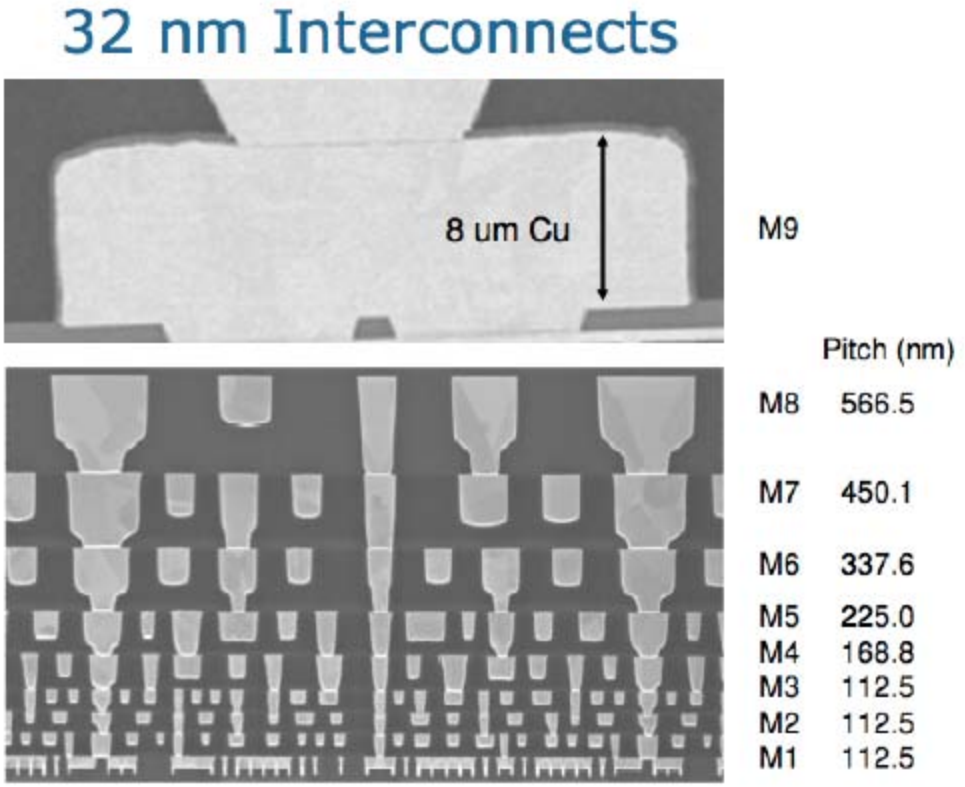






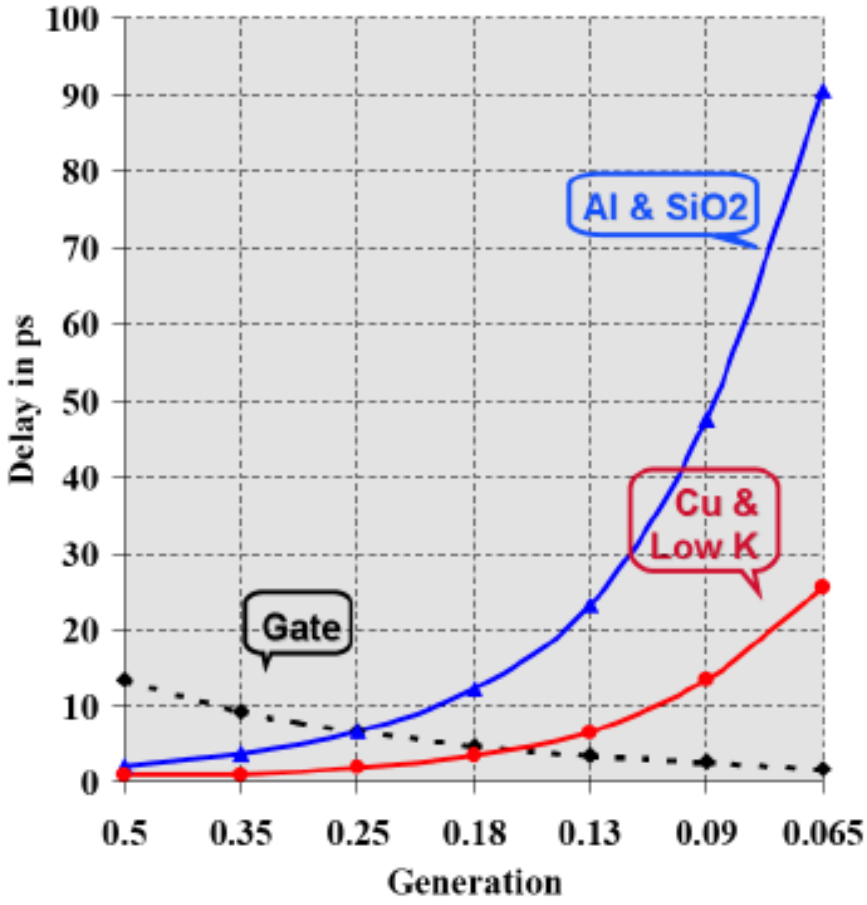
Advanced Metallization





Why are wires important?

Why Cu/Low-k?….R*C Product



Gate Delay

Interconnect Delay, Al & SiO2

Interconnect Delay, Cu & Low K

Interconnect will dominate timing delay.

Cu/Low-k buys 1-2 generations.

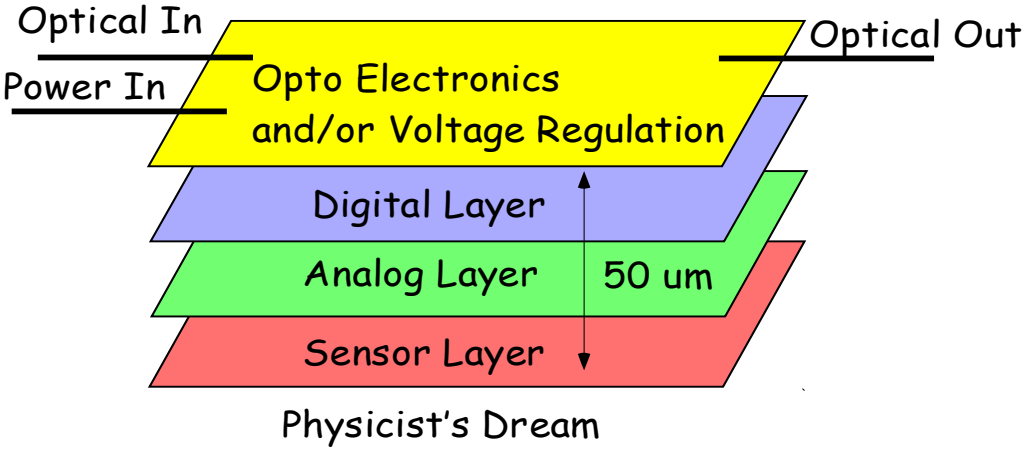
Al	*3.0 uΩ-cm*
Cu	*1.7 uΩ-cm*
SiO2,	*K=4.0*
Low K	*K=2.0*
Al & Cu	*.8um Thick*
Al & Cu Line	*436um Long*

Data From: Bohr, Mark T; "Interconnect Scaling - The Real Limiter to High Performance ULSI"; Proceedings of the 1995, IEEE International Electron Devices Meeting; pp241-242

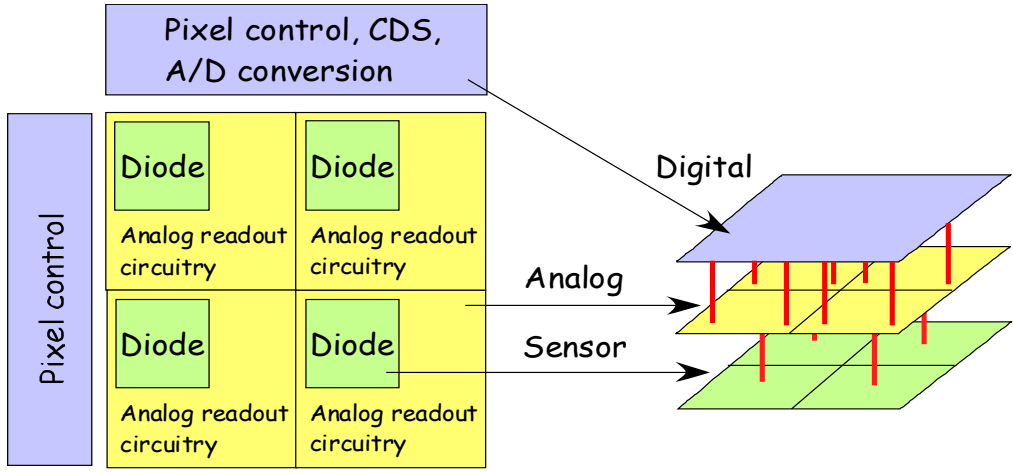
The technology leap: 3D vertical integration

Vertical integration technologies

- A “3D” chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a “monolithic” circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward Vertical Integration to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- This is a major direction for the semiconductor industry.



Physicist’s Dream



Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

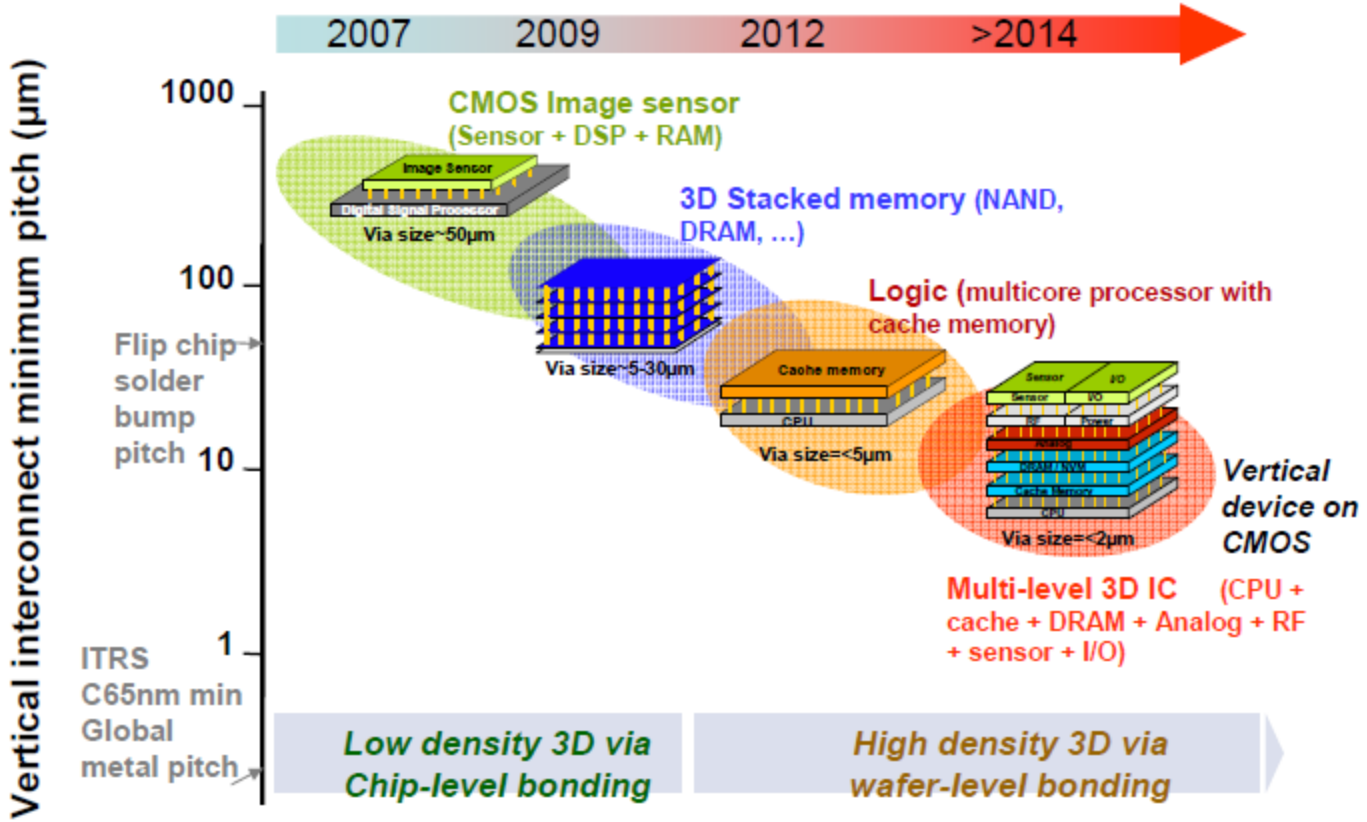
3D Integrated Circuits in Industry

- 3D electronics: "the vertical integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers."[1]

- 3D electronics has the potential of being:
  - Denser (smaller form factor)
  - Faster (reduced delay because of shorter interconnects)
  - Lower power (smaller interconnect capacitance)
  - Lower cost (sizably less expensive than aggressive CMOS scaling)
  - Integration of dissimilar technologies (sensor, analog, digital, optical)

1) Philip Garrou, Christopher Bower, Peter Ramm, Handbook of 3D Integration Technology and Applications of 3D Integrated Circuits,Wiley-VCH, 2008.

Applications of 3D Si integration



source:

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

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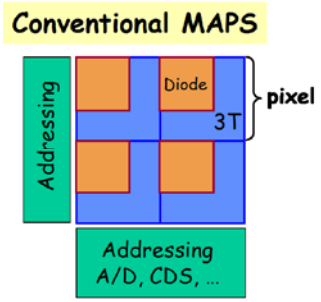
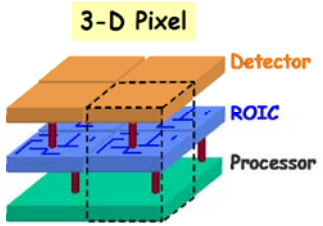
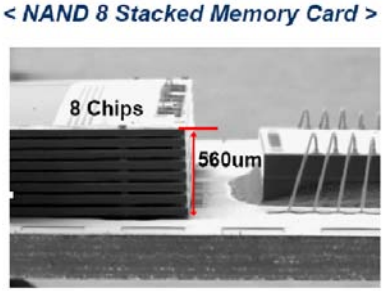
Major Markets being Pursued by Industry for 3D integration

- Pixel arrays for imaging
  - Pixel arrays with sensors and readout are well suited to 3D integration since signal processing can be placed close to the sensor. Current 2D approaches cannot handle the data rate needed for high speed imaging.

- Memory
  - All major memory manufactures are working on 3D memory stacks. Significant cost reductions can be expected for large memory devices. The cost of 3D can be significantly less than going to a deeper technology node.

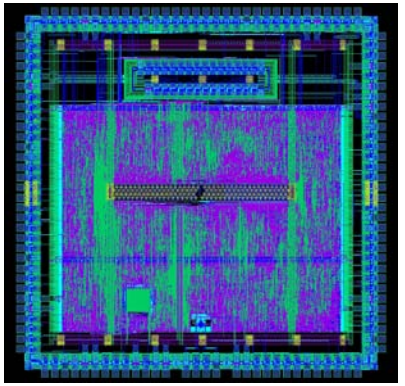






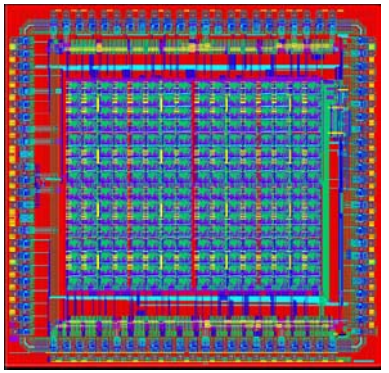
Major Markets being Pursued for 3D

- Microprocessors
  - A major bottleneck is access time between CPU and the memory. Memory caches are used as an interface but the area required is significant. Initial applications for 3D will use Logic to Memory, and Logic to Logic stacking. Intel is claiming terabyte transfer rates between stacked memory and multicore processors is possible.



CPU and 220 MHz memory Stack (Tezzaron)

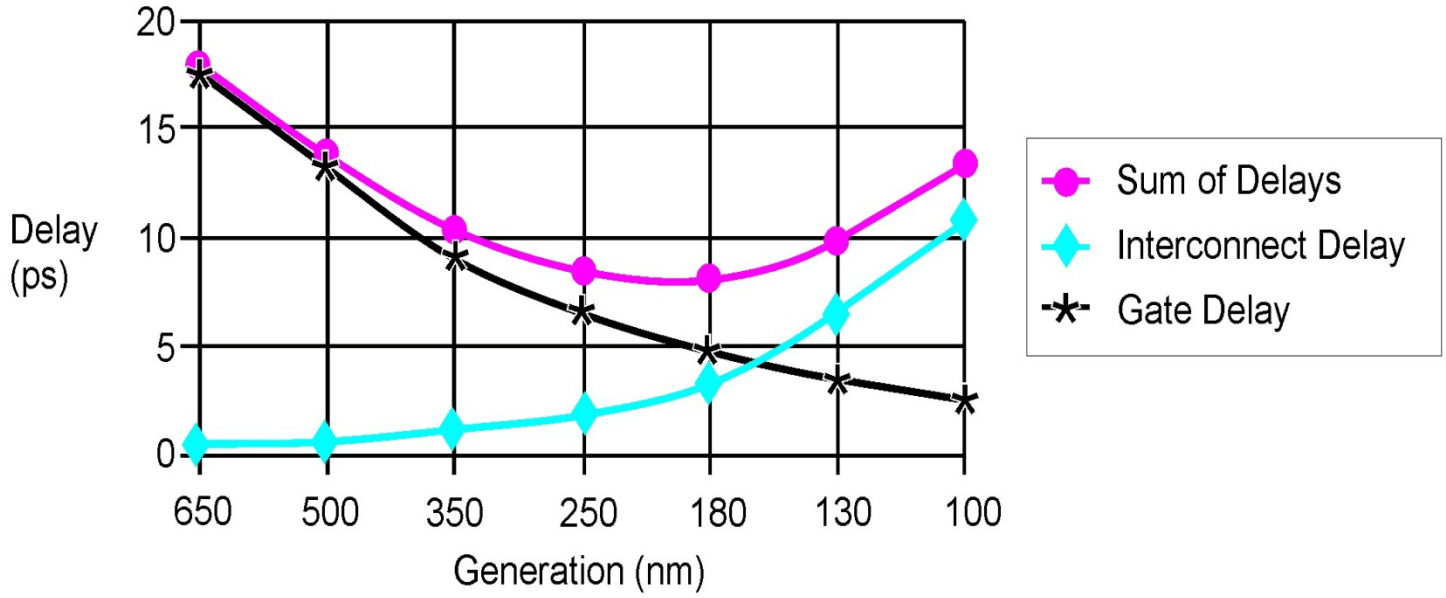
- FPGAs
  - Wire delays are an inherent problem in 2D FPGAs. 3D integration can improve performance by removing the programmable interconnect from the logic block layer and moving it to another tier.



FPGA – 12 vertical interconnects per logic block (Tezzaron)

Speed advantage of 3D

SPEED / PERFORMANCE ISSUE *The Technical Problem*



"It is clearly seen in Figure 1, that without further reductions in interconnect delay, reducing gate dimensions much below 130nm do not result in corresponding chip improvements."

NSA Tech Trends Q3 2003

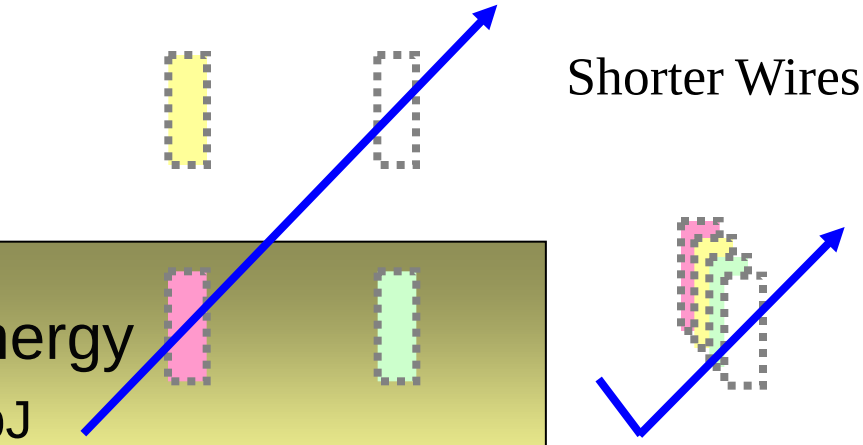
Speed and power advantage of 3D for semiconductor industry

$$t_d \approx 0.35 \times rcl^2$$

$$P_{avg} = VDD \times I_{avg} = C_{tot} \times VDD^2 \times f_{clk}$$

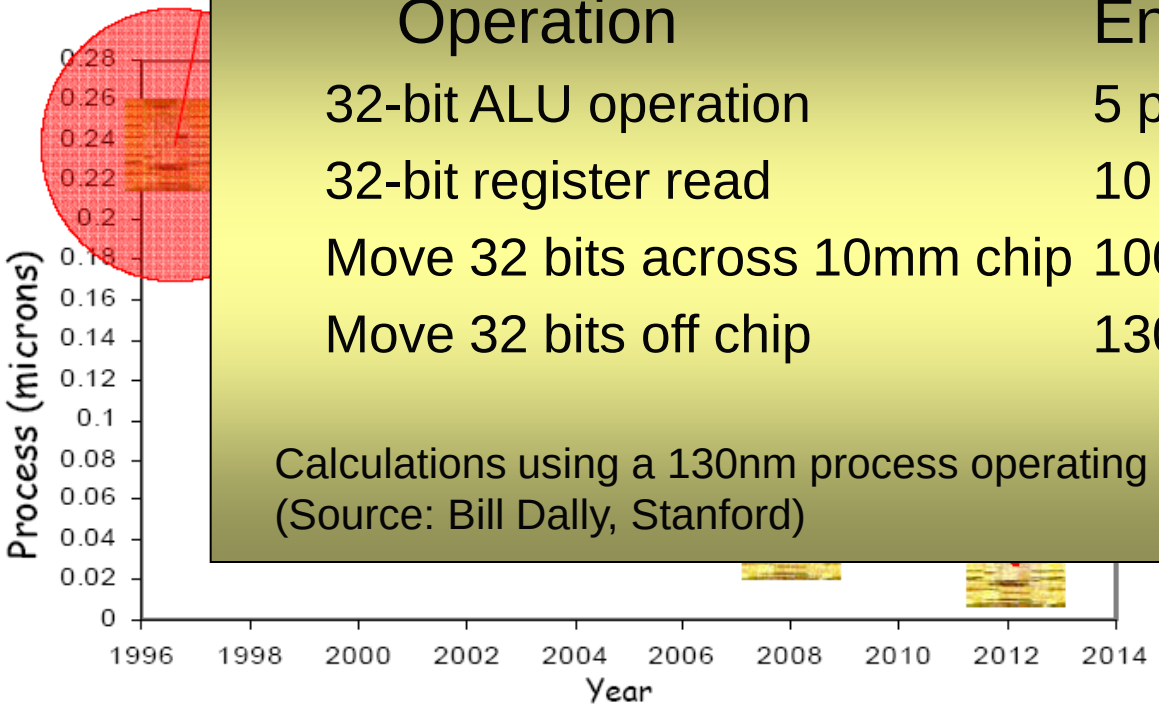
C is mostly due to wiring

Therefore:

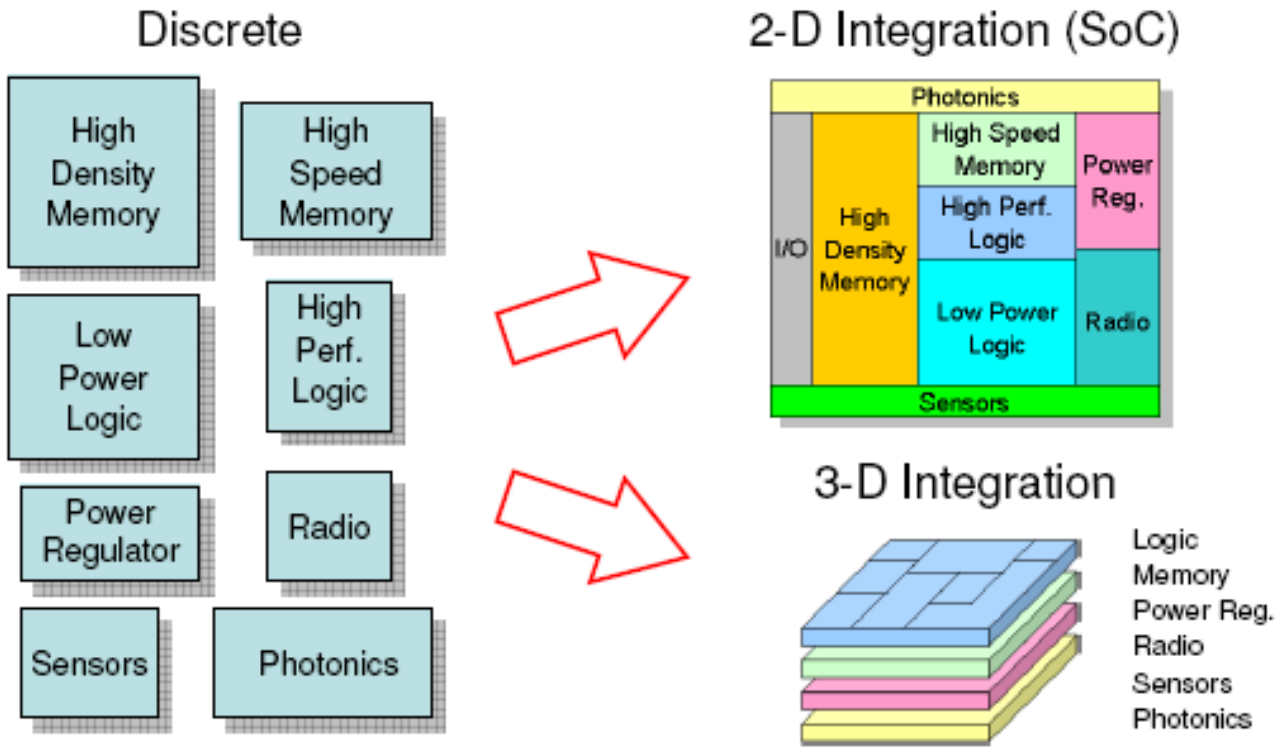


Operation	Energy
32-bit ALU operation	5 pJ
32-bit register read	10 pJ
Move 32 bits across 10mm chip	100 pJ
Move 32 bits off chip	1300 to 1900 pJ

Calculations using a 130nm process operating at a core voltage of 1.2V
(Source: Bill Dally, Stanford)



System Integration



System integration needed for performance, power, form factor

Challenge is to integrate wider range of heterogeneous elements

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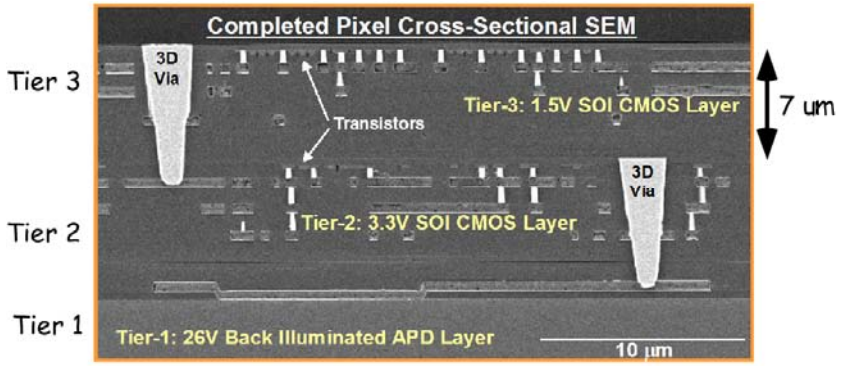
Key Technologies for 3D (I)

1) Via formation and metallization

- Vias typically have an aspect ratio of 5-8:1
- Vias fabricated after the Back End of Line (BEOL) foundry processing are know as "via last". Vias that are fabricated as a part of the IC foundry process are known as "via first" and use less silicon real estate.
- CMOS wafers require passivation of the vias before metallization to avoid shorts
- SOI wafers do not require via passivation



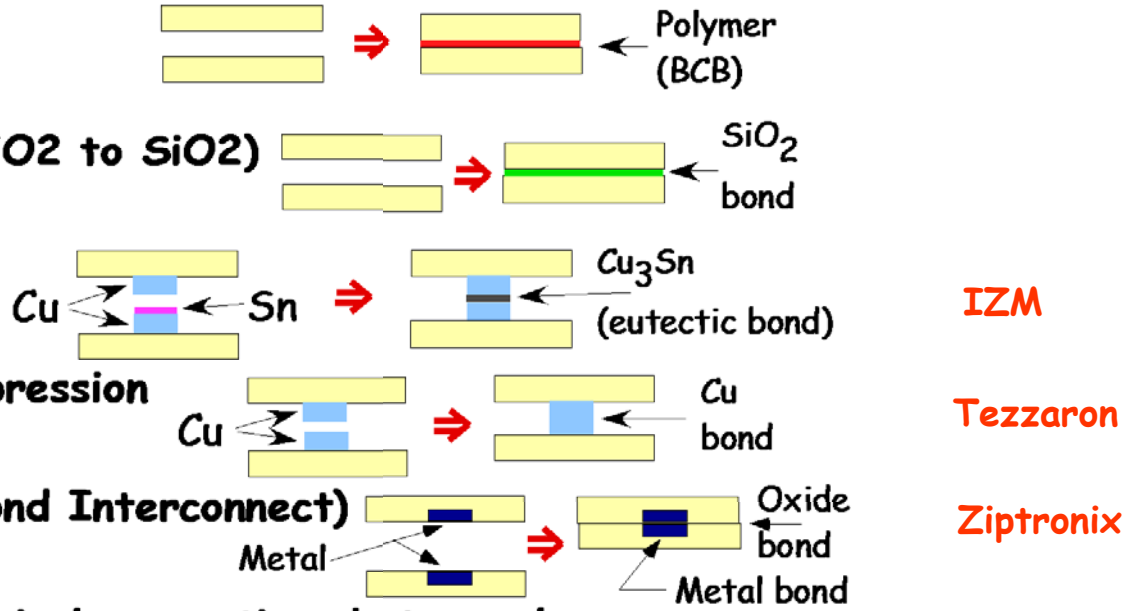
MIT LL via last process in SOI

2) Thinning

- To minimize space for vias in small pixel designs, thin substrate as much as possible

Key Technologies for 3D (II)

3) **Bonding between Die/Wafers**



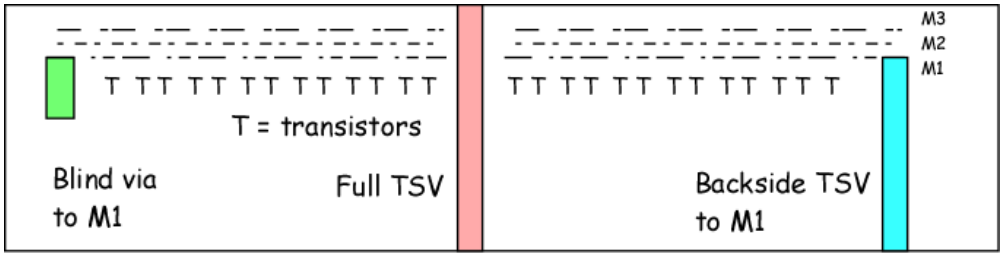
For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

4) Precision alignment

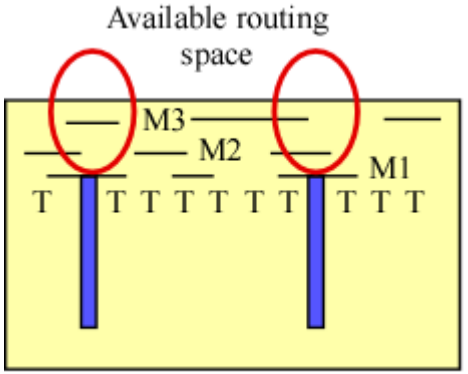
of better than 1 um (3 sigma) is now possible with wafer to wafer bonding.

Vias Used in 3D Integration

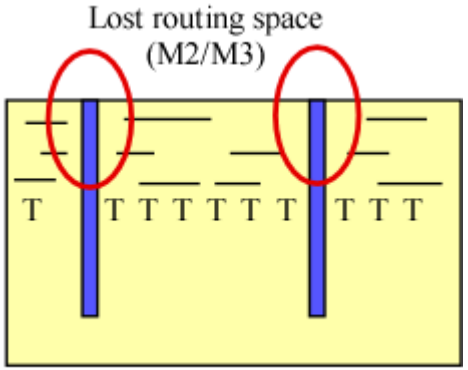
- Three different types of vias are used in 3D integration
  - Blind TSV – (via first or middle)
  - Full TSV – (via last)
  - Backside TSV – (via last)
- TSVs can be implemented at three different stages in the IC fabrication process.
  - Via first – before FEOL (Front end of line/transistor formation) processing
    - Small vias
  - Via middle – After FEOL and before BEOL (Back End Of Line/metalization) processing
    - Small vias
  - Via last – After BEOL processing
    - Generally large vias
    - Via last technique often requires space on all metal layers.
    - Very bad for high density designs



Example of three different types of vias used in 3D integration



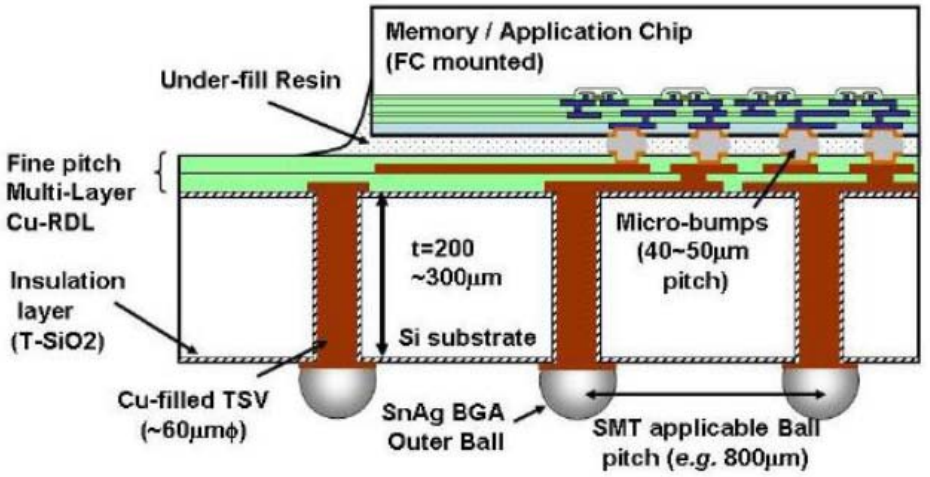
Via First or Via Middle

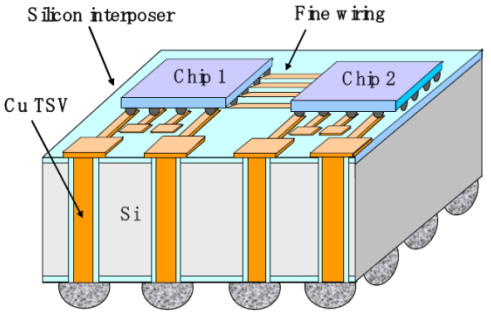


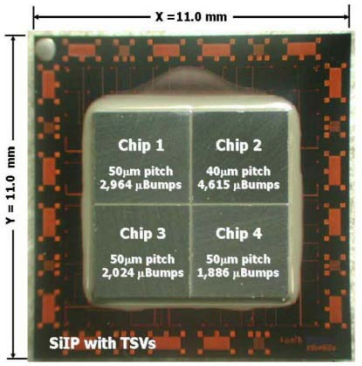
Via Last

3D Interposers

- Silicon interposers have become known as 2.5 D integration because there are TSVs in the silicon interposer.
  - Use full through wafer via
  - Allows fine pitch interconnections between die.
  - Good CTE match between chips and substrate
  - May have multiple levels of interconnection on interposer
- Beginning to become available from different sources

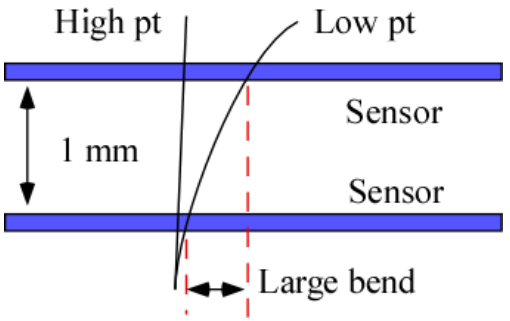




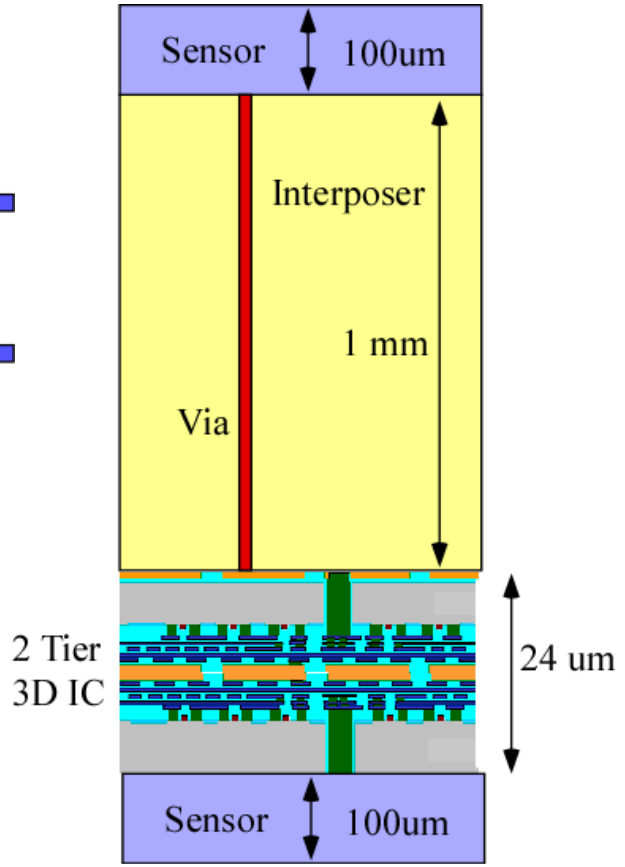


Interposer Application for CMS Track Trigger

- The TSV technology has been proposed for use in CMS to locally identify high pt tracks and thus minimize data transfer
- This can be done by having two layers of sensors separated by an interposer of modest thickness (~1 mm)
- Signals would pass from the top sensor through the interposer to a ROIC which processes signals from the top and bottom sensors to look for steep tracks.
- A 3D track trigger demonstrator chip called VICTR is now at the foundry.



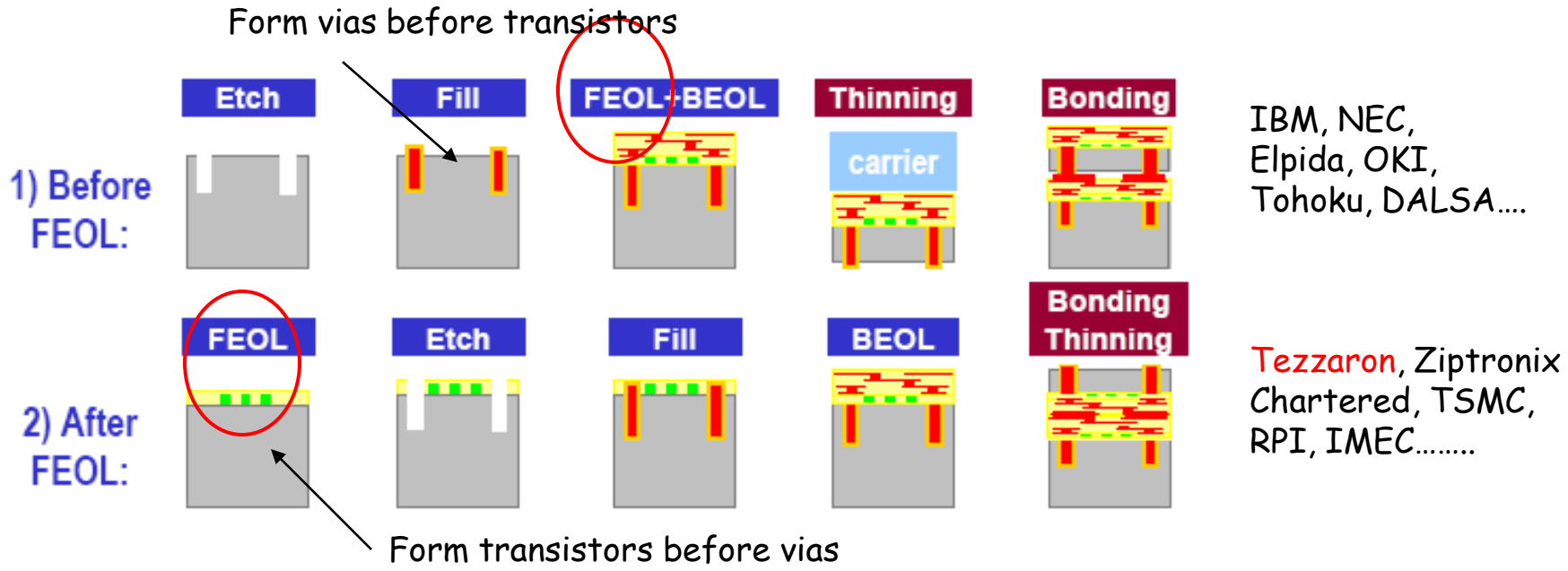
Sensor pair in magnetic field



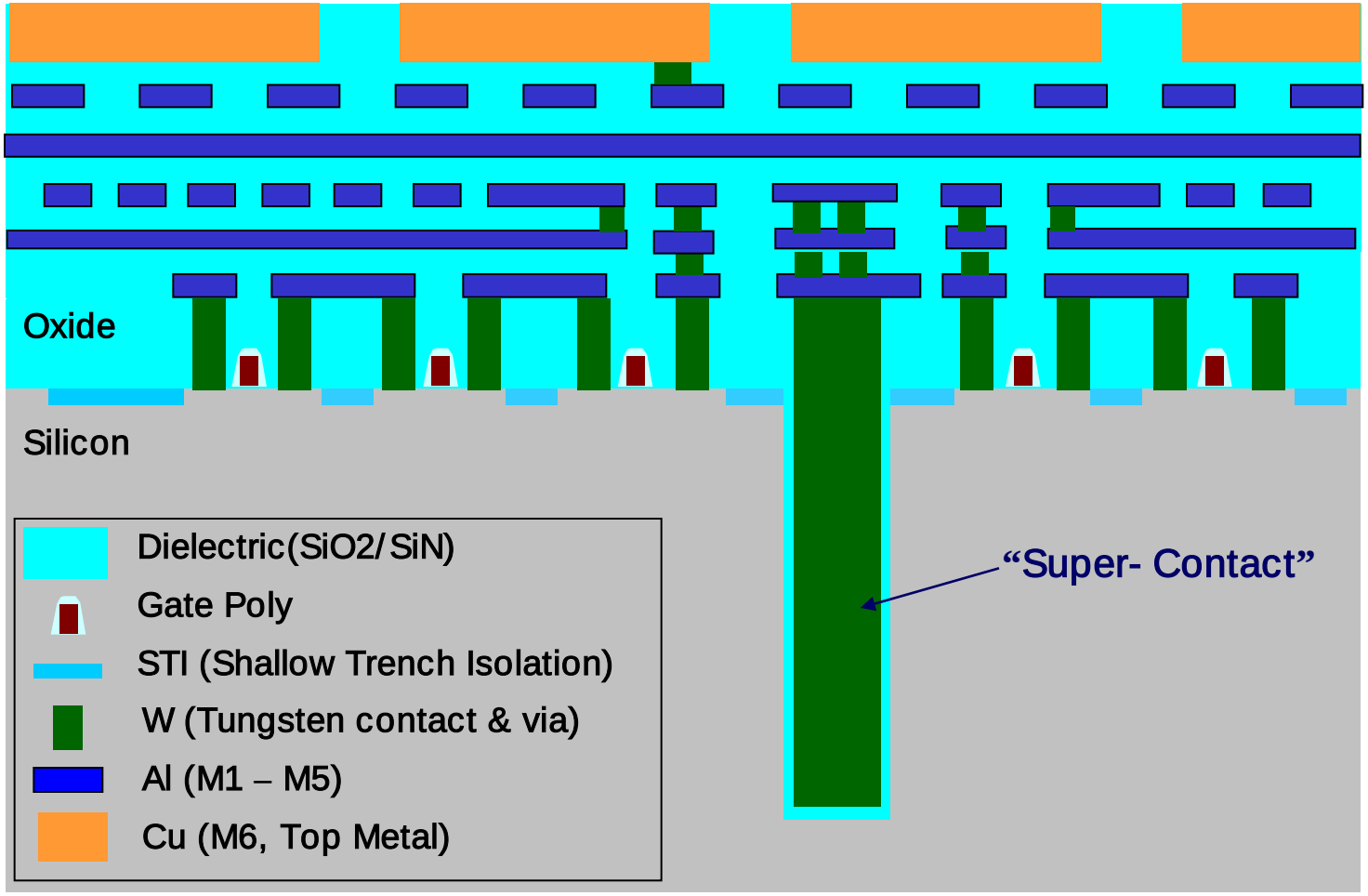
Assembly Cross section

Via First Approach

- Through silicon Via formation is done either before or after CMOS devices (Front End of Line) processing



Example of Via First Approach: Tezzaron/Chartered process (I)

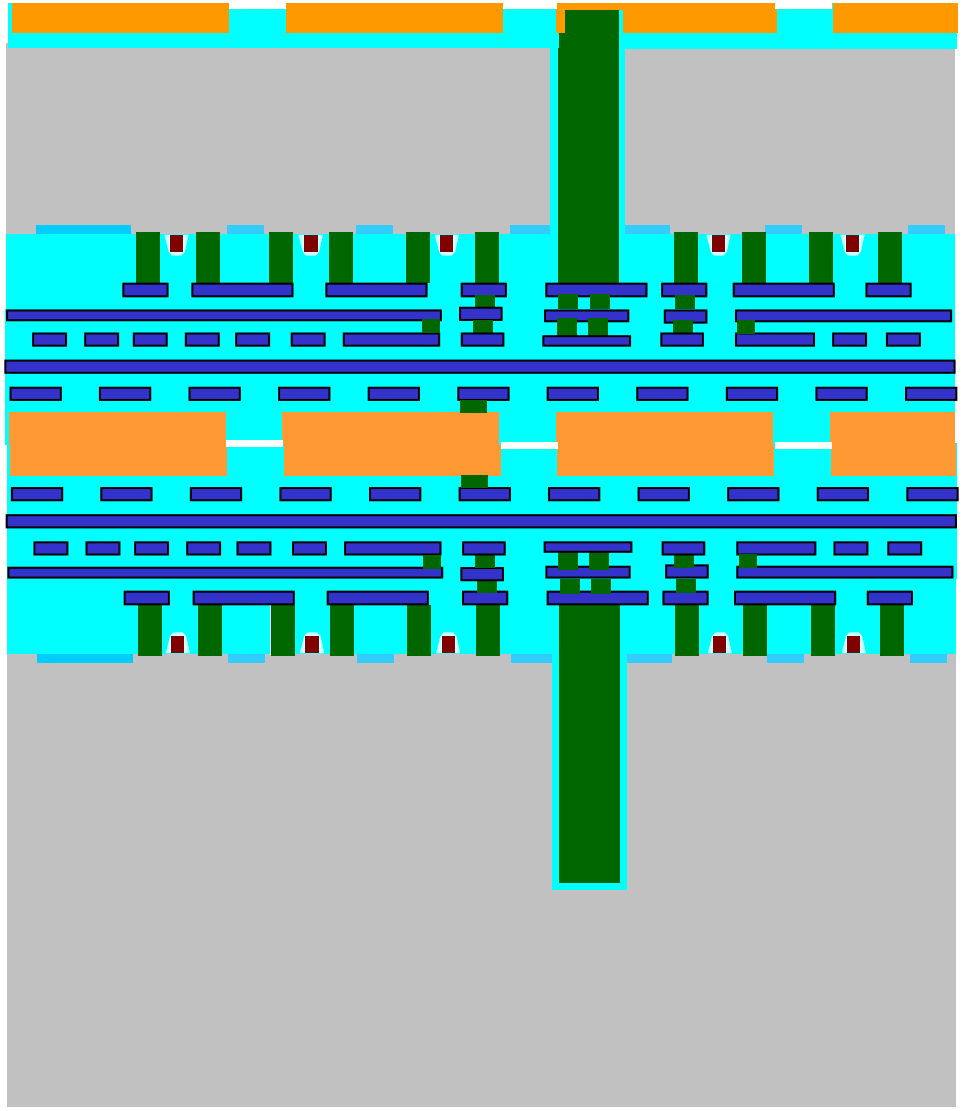


Step2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7 μm)

Step 1: Fabricate individual tiers; on all wafers to be stacked: complete transistor fabrication, form super via. Fill super via at same time connections are made to transistors

Based on 130 nm bulk CMOS process by Chartered

ɔroach:
:ess (II)

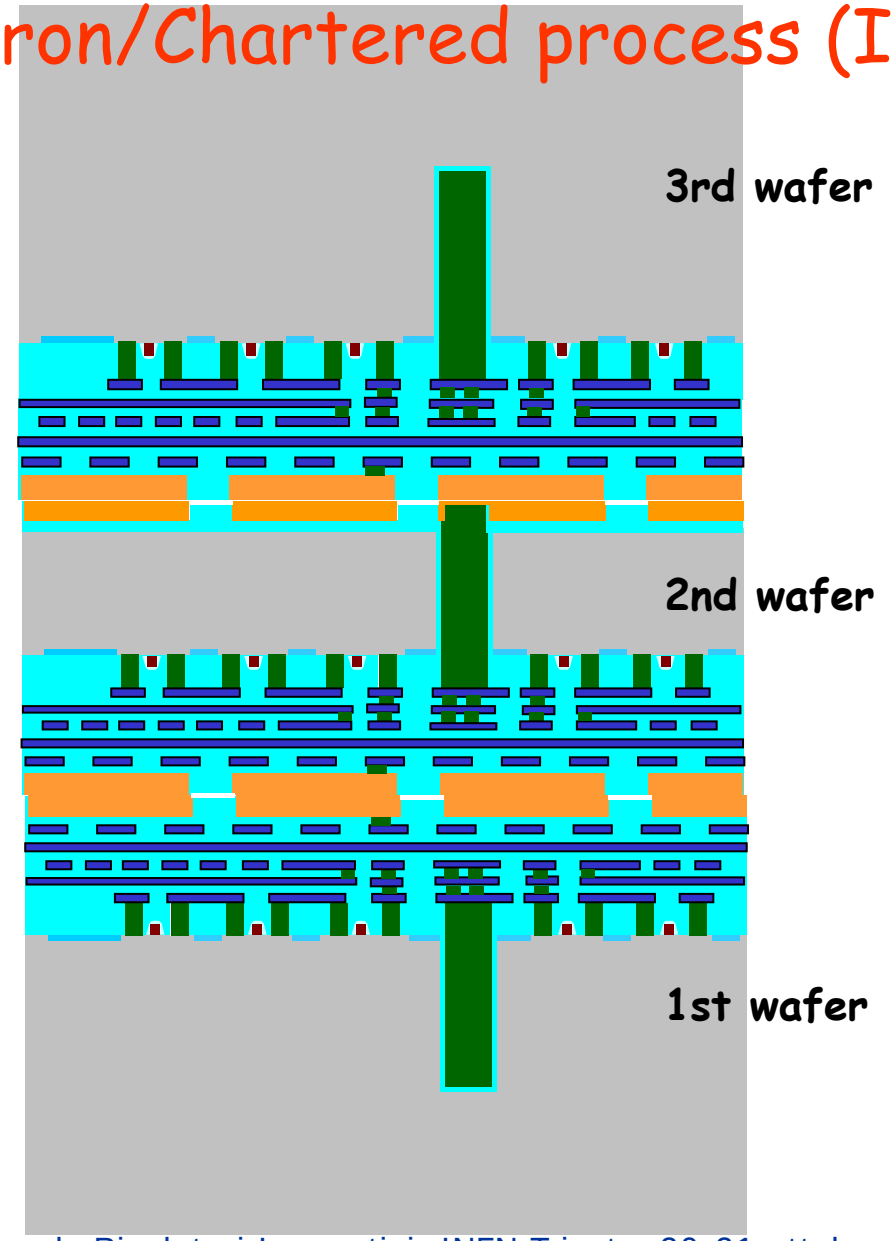


Step 3: Bond wafer-2 to first wafer-1 by a Cu-Cu thermo-compression bond

Step 4: Thin wafer-2 to about 12 um to expose super via. Add Cu to back of wafer-2 to bond wafer-2 to wafer-3 OR stop stacking now! add metallization on back of wafer-2 for bump bond or wire bond

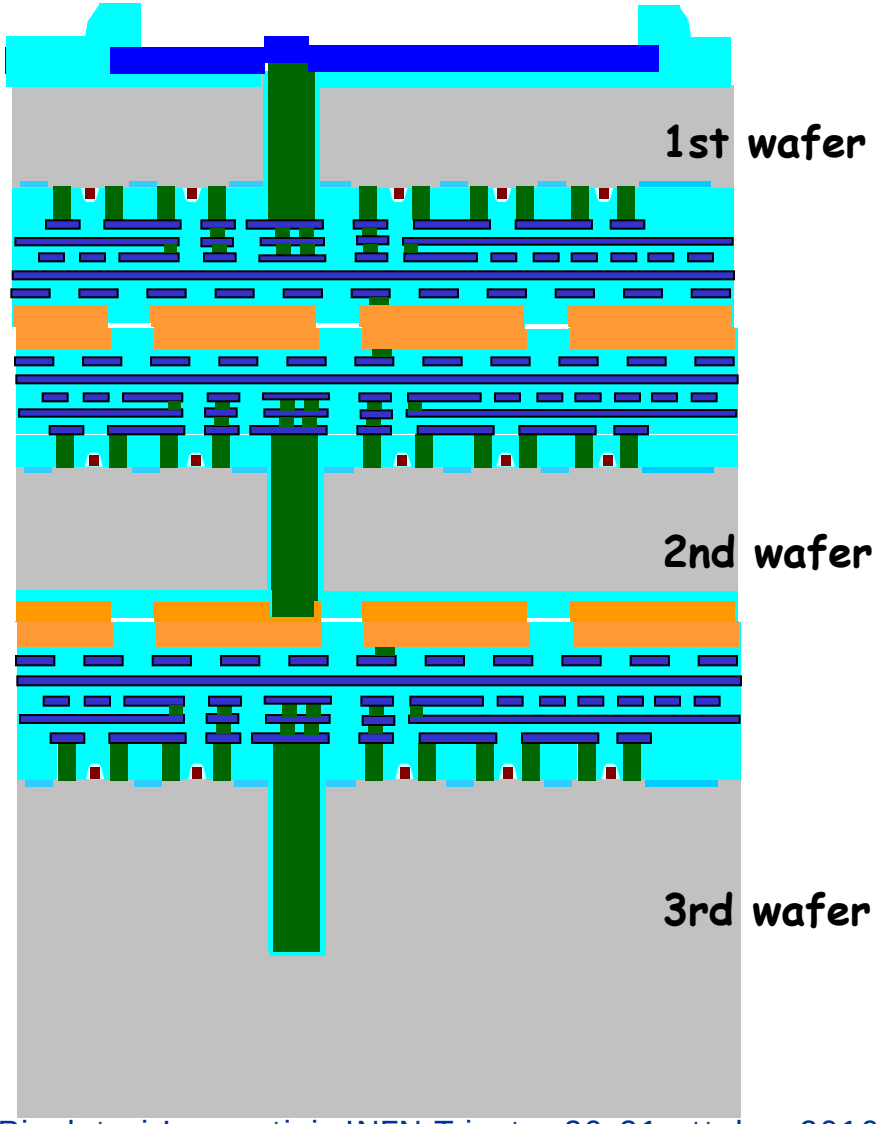
Example of Via First Approach: Tezzaron/Chartered process (III)

Step 5: Stack wafer-3



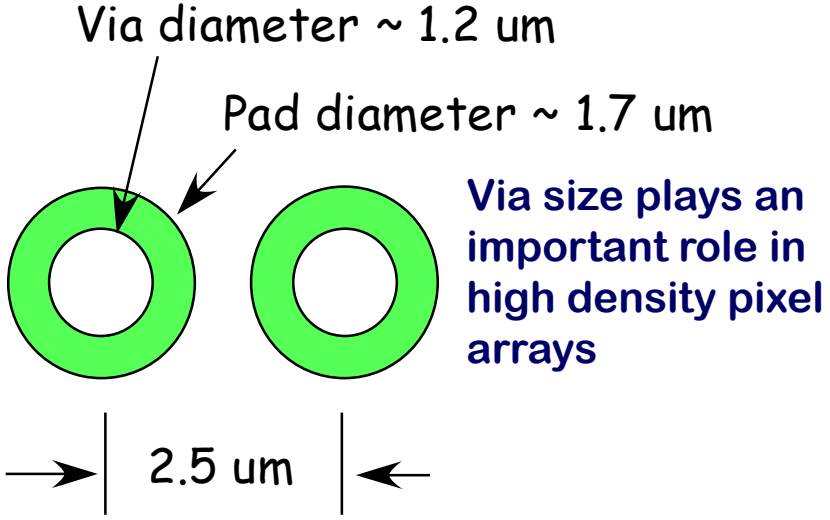
Example of Via First Approach: Tezzaro (IV)

Step 6: Thin wafer-3
Add final passivation and metal for bond pads



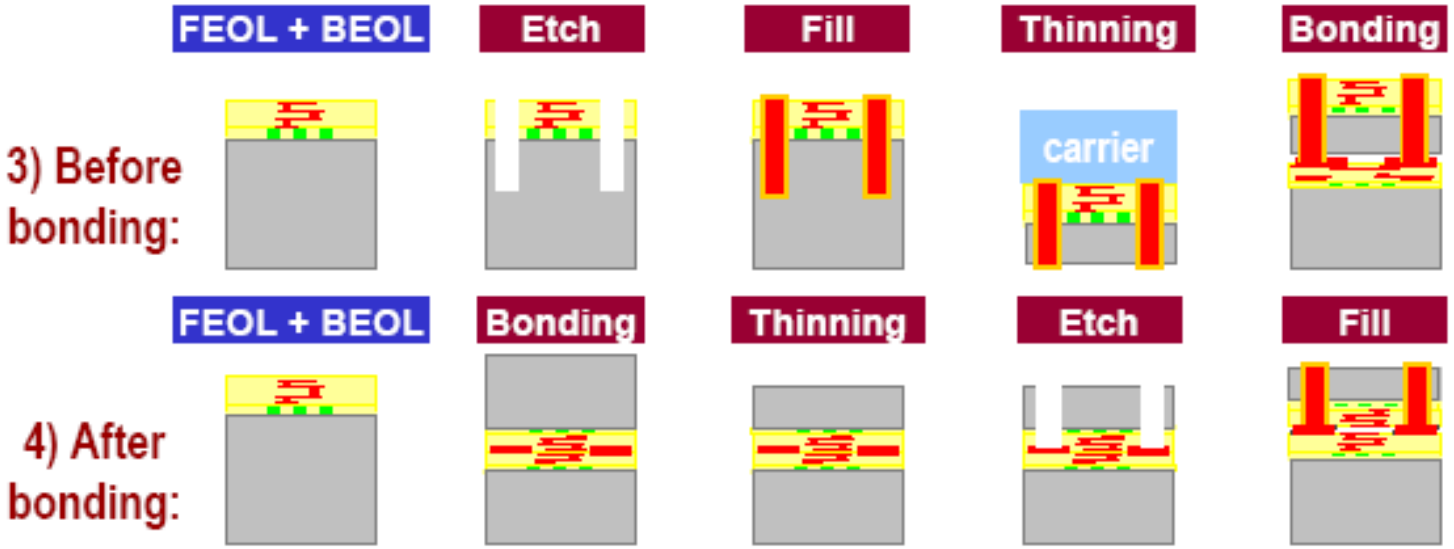
Advantages

- No handle wafers needed
- No extra space allotment in BEOL processing for vias
- Vias are very small
- Vias can be placed close together
- Minimal material added with bond process
  - 35% coverage with 1.6 um of Cu gives Xo=0.0056%
  - No material budget problem associated with wafer bonding.
- Thinned transistors have been characterized



Via Last Approach

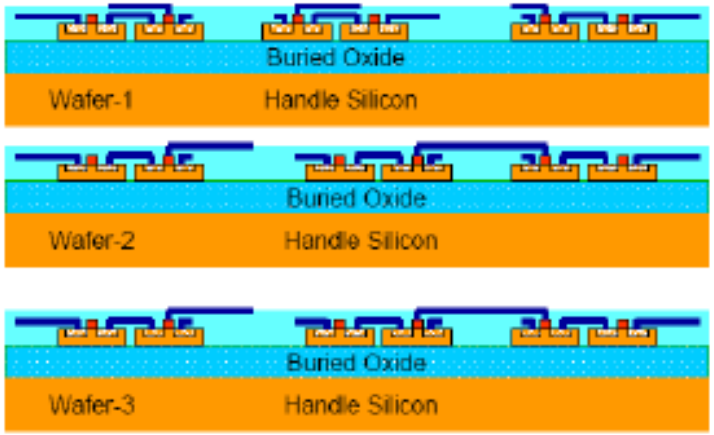
- Via last approach occurs after wafer fabrication and either before or after wafer bonding



Example of Via Last Approach: MIT Lincoln Lab SOI process

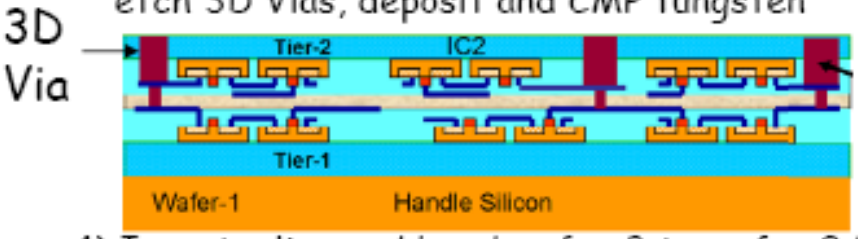
- 3 tier chip (tier 1 may be CMOS)
- Vias formed after FEOL and BEOL processing is completed

1) – fabricate individual wafers

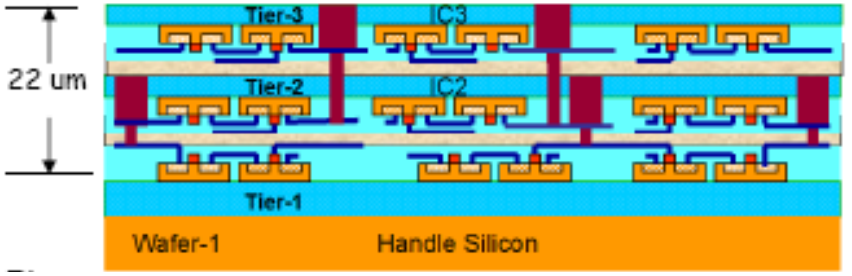


2) Invert, align, and bond wafer 2 to wafer 1

3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

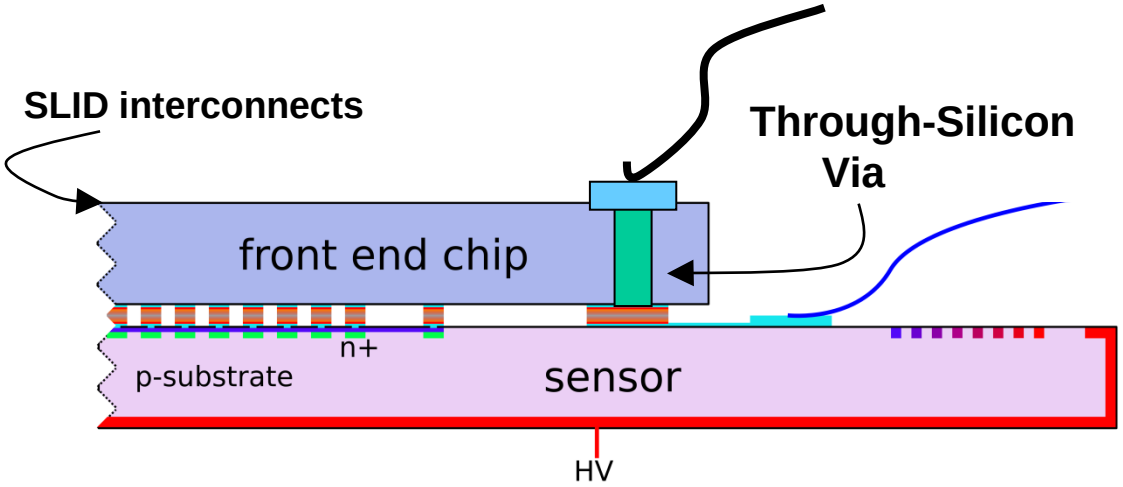


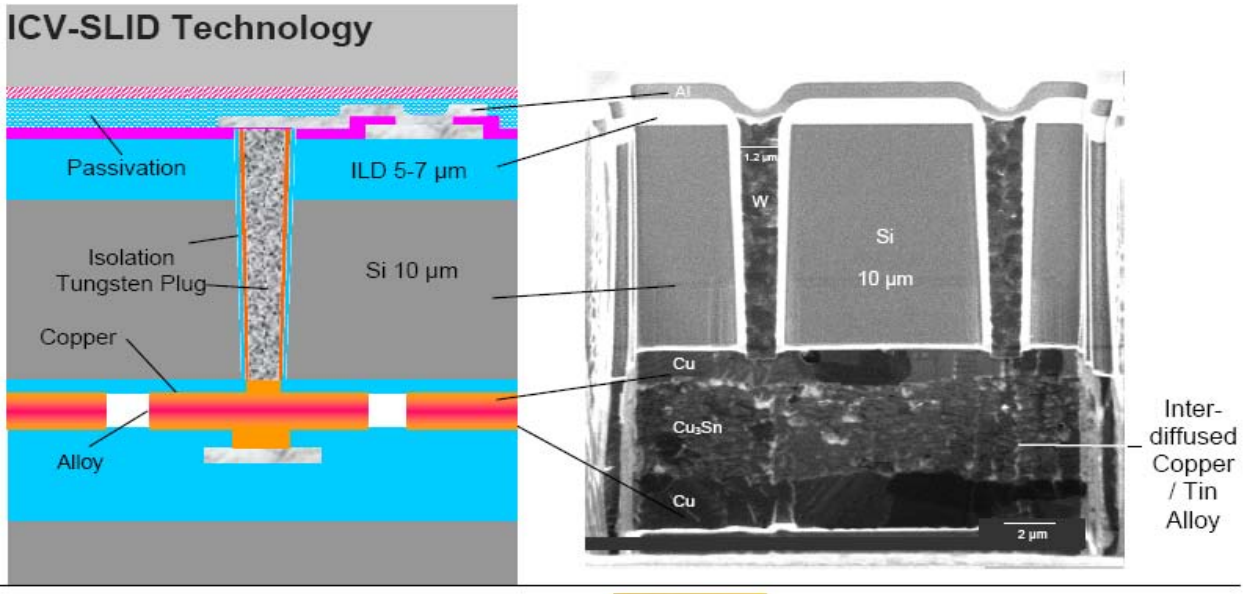
4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



Another example of 3D vertical integration activities

MPI Munich: 3D interconnection with SLID (Solid-Liquid InterDiffusion) technology by IZM





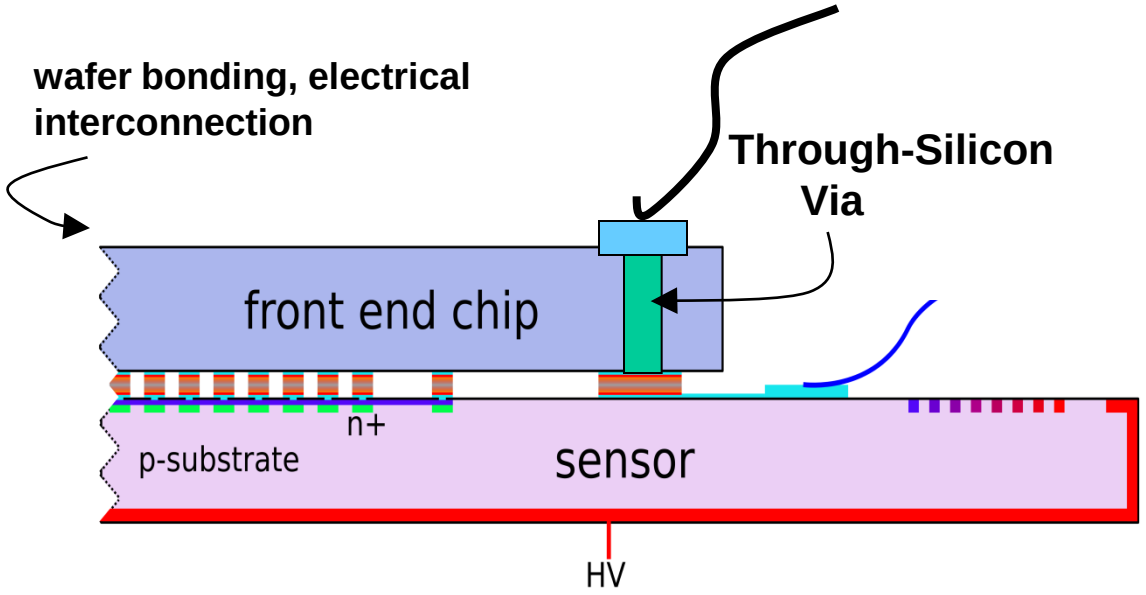
Build demonstrator using LHC pixel chip (FEI2) and thin (75/150 μm) pixel sensors made by MPI (single chip module)

R&D goals:

- **Test thin detectors (less trapping, rad hard)**
- **Thinning of readout chips**
- **Practice SLID and ICV (InterChip Vias) to achieve 4-side buttable ASICs (material reduction)**

Benefits of vertical integration…

- 4-side buttable sensor for full area coverage (no dead area)



OKI-SOI Consortium

Silicon-on-Insulator (SOI):

Handle wafer (bulk): high resistivity silicon sensor

Top wafer: readout electronics

Well suited to vertical integration, several SOI wafers can be stacked

KEK (Japan)
Tsukuba Univ. (Japan)
Osaka Univ. (Japan)
JAXA/ISAS (Japan)
Lawrence Berkeley Laboratory (USA)
Fermi National Laboratory (USA)
Univ. of Hawaii (USA)
IFJ Krakow (Poland)

Interests in Participation:
Rutherford Appleton Lab (England)
Univ. of Barcelona (Spain)
Tata Institute (India)
Louvain-la-Neuve Univ. (Belgium)

No bump bonding, small capacitance of sensing nodes (fully depleted diodes)

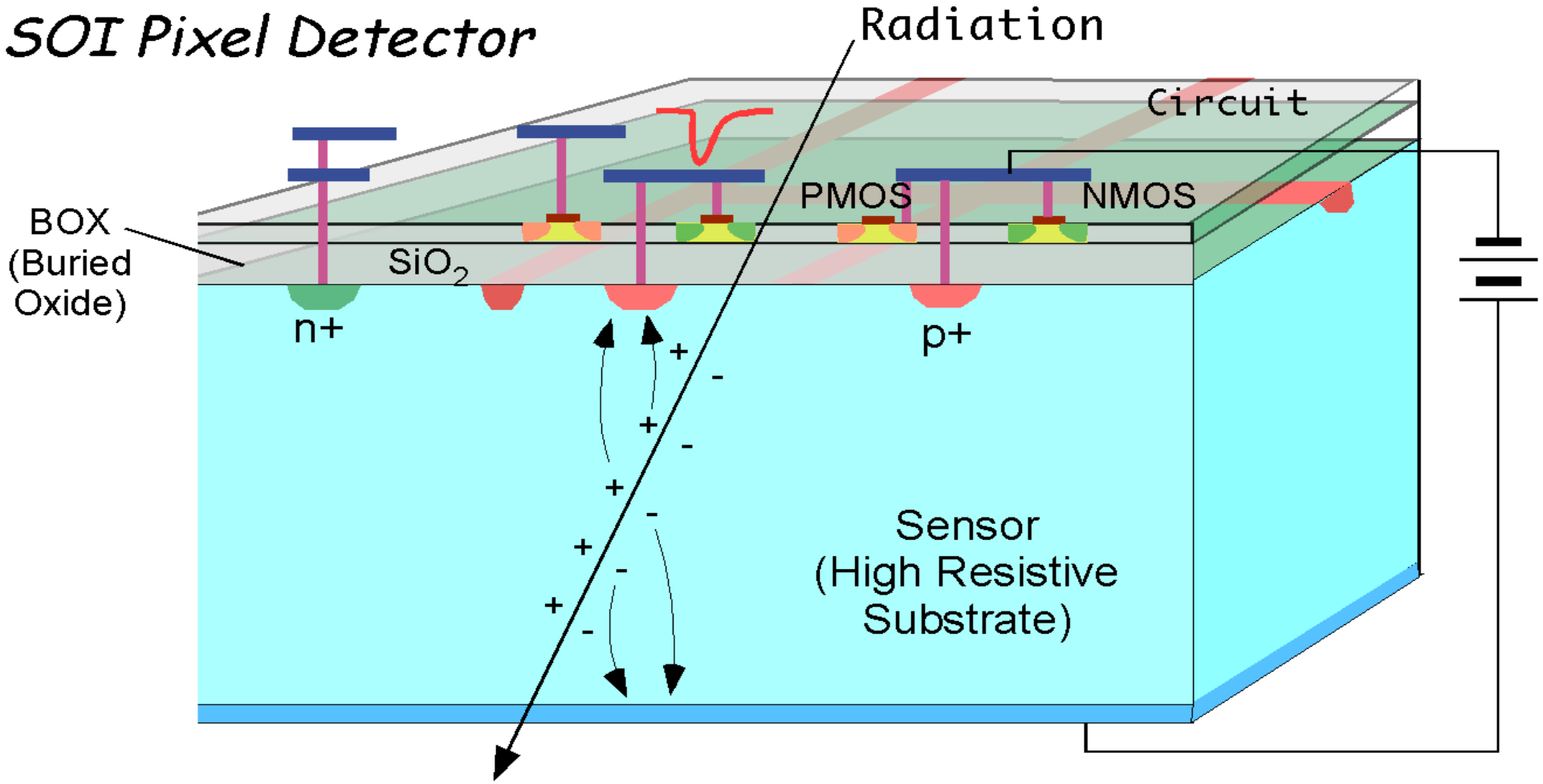
Full CMOS circuitry in the pixel cell (dielectrically isolated from sensor substrate)

Mitigation of coupling between electronics and sensor:

by a buried P-well structure (reduction of backgate effects)

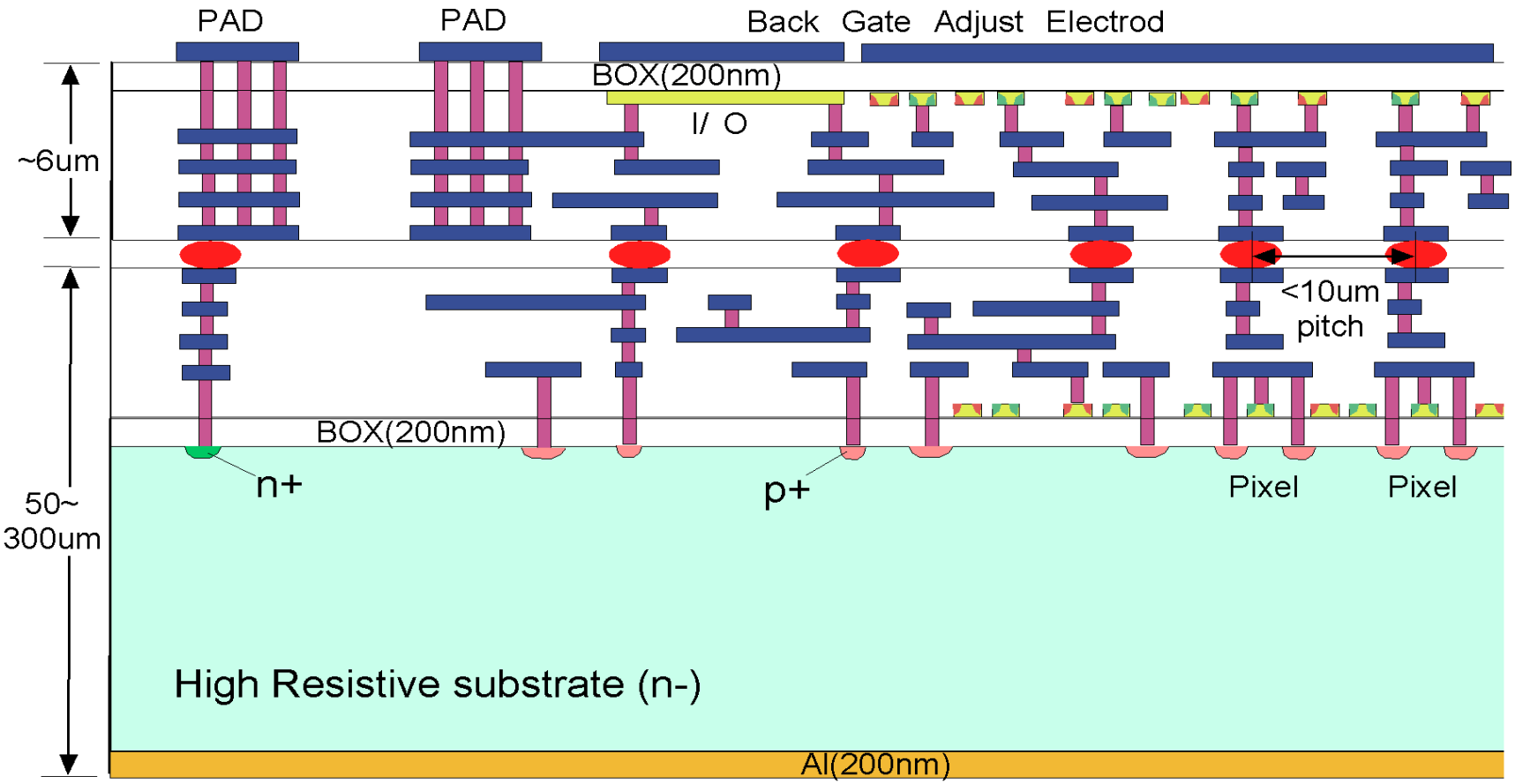
or by vertical integration (sensitive circuit blocks and sensor in two different wafers)

From an SOI pixel detector…



… to devices based on vertical integration of two SOI wafers

ZyCube: combination of μ-bump bonding (~5 um pitch)
with an injected adhesive bond
First bonded chip available soon.



3D Technology Advantages for HEP

- Aggressive thinning leads to low mass circuits resulting in low particle scattering applications such as the ILC vertex detector.
- New bonding technologies for 3D lead to alternatives to conventional bump bonding that can provide lower mass, finer pitch, and enhanced mechanical robustness for additional mechanical processing (thinning without destroying the connections)
- Via formation allows for increased circuit density with multiple tiers, and/or allows for 4 side buttable circuits.
- 3D via formation allows for mixed circuit technology design and independent analog and digital substrates.

Particle detectors and 3D vertical integration

- **3D pixel arrays with high functionality and smaller form factor** for particle tracking

- Vertical integration is a very appealing way to achieve a small pixel pitch (≤ 20 μm for ILC, ≤ 50 μm for SuperB and SLHC), improving the resolution and reducing the single pixel occupancy, and at the same time implementing complex functionalities in the pixel itself, such as low-noise amplification, sparsified readout and time stamping.

- **Digital readout architecture** can be designed to handle a **large data flow** without the constraints that may arise when it is implemented on the same substrate as the sensor (as in MAPS) or as the analog electronics (as in hybrid pixel readout chips).

- **Imagers for advanced X-ray sources** (XFEL) may strongly benefit from the improved functionalities and performance that come along with vertical integration and allow for small pitch pixels capable of handling high data rates.

Active Pixel Sensors and Vertical Integration Technologies

- The very crowded zoo of vertical integration processes can be reduced to two different basic approaches (and technical problems):

1. **Interconnection between 2 (or more) CMOS layers,**
   a) one layer with a MAPS (Monolithic Active Pixel Sensor) device and analog front-end, and the other layer(s) with the digital readout

2. **Interconnection between a CMOS readout electronics chip (2D or 3D) and a fully-depleted high resistivity sensor**
   a) with bump bonding (standard, but low pitch may be needed)
   b) with a vertical integration technique (low material budget, more advanced)

The 3D MAPS approach

- MAPS (Monolithic Active Pixel Sensors) are a promising solution for low-mass, high granularity pixel trackers

  ILC VTX: < 0.1% X_0 per layer; space point precision < 5 μm

  SuperB SVT Layer0: < 0.5% X_0; hit resolution 10 - 15 μm

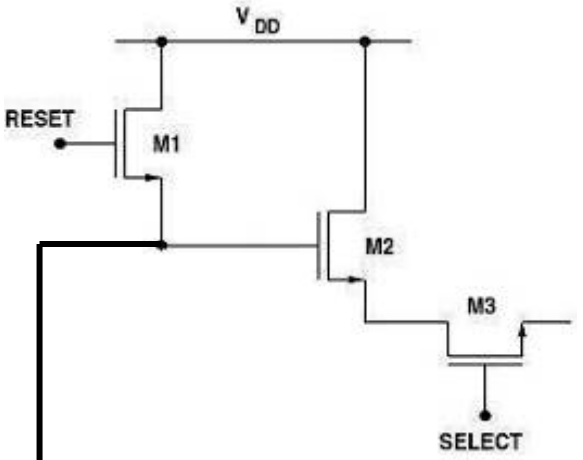
- After several years of R&D, MAPS for particle detection are reaching a good maturity level, but there is still room for substantial improvements

- The performance of standard MAPS needs to be upgraded if they have to fulfill specifications of experiments at ILC or SuperB (to say nothing of the SLHC…)

- MAPS can benefit from technological advances; the scenario of microelectronics processes and performance typically changes in a time scale of 1-2 years.

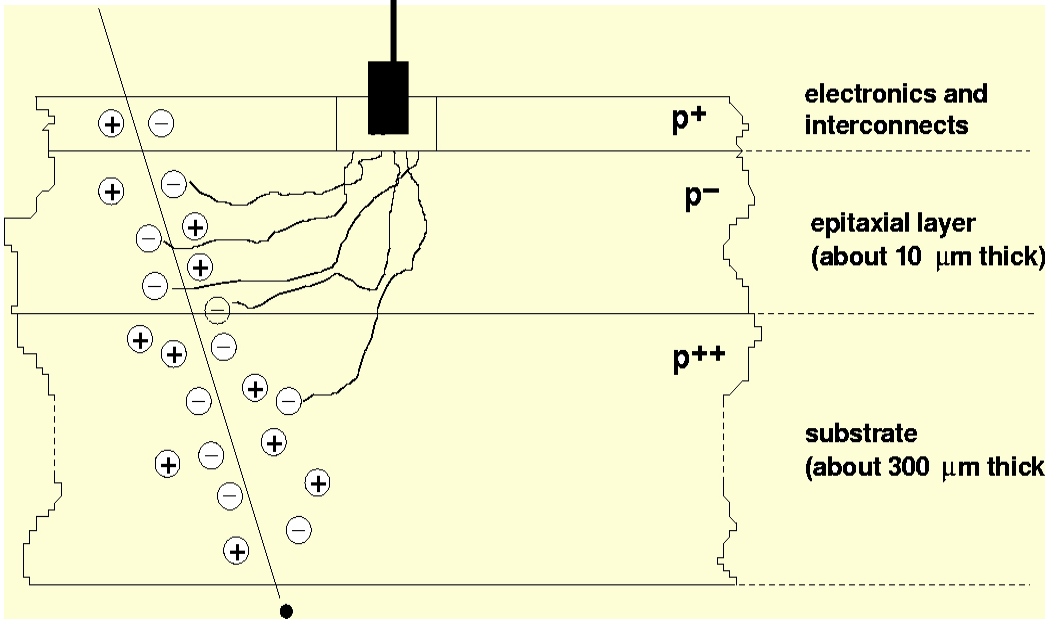
The standard reference: 3T CMOS MAPS

- Developed for imaging applications
- Several reasons make them very appealing as tracking devices :
  - detector & readout on the same substrate
  - wafer can be thinned down to few tens of μm
  - high functional density and versatility
  - low power consumption and fabrication costs



Principle of operation

- The undepleted epitaxial layer (or a non-epi substrate) acts as a potential well for electrons
- Signal (~1000 e-) collected through diffusion by the n-well contact
- Charge-to-voltage conversion provided by the sensor capacitance
  → small collecting electrode
- Simple in-pixel readout (PMOS not allowed)
  → sequential readout



MAPS R&D strategies

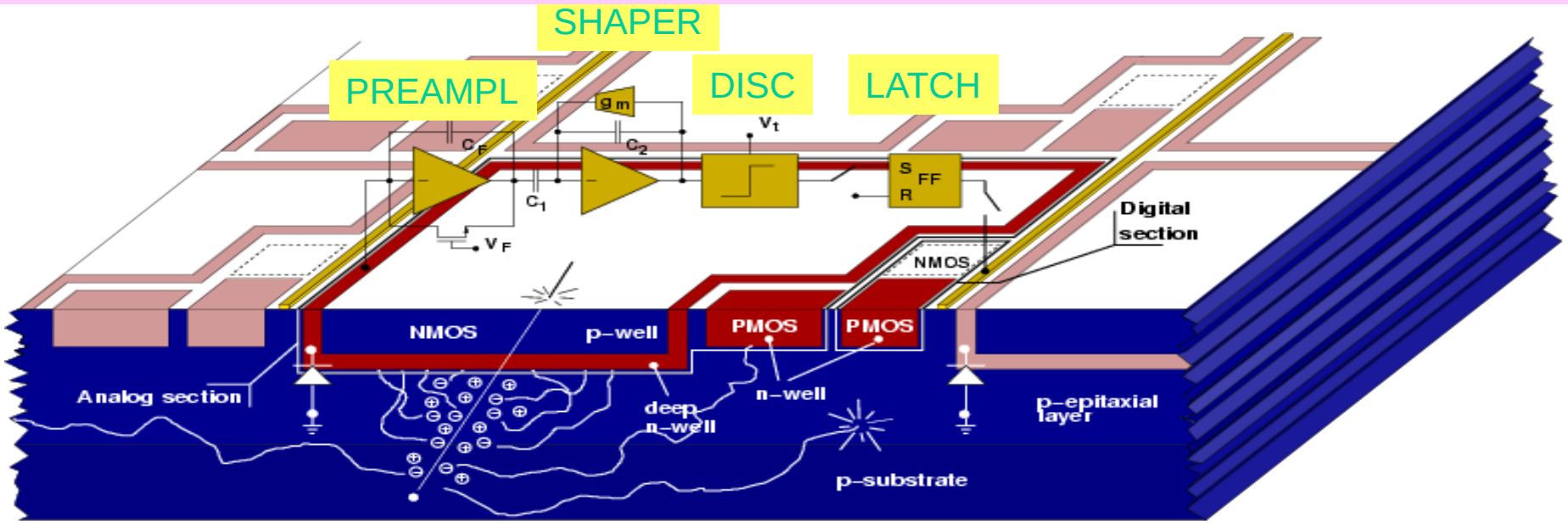
Two main development lines are followed by the MAPS community:

- Improve electronics performance:
  - ➔ put more intelligence on the chip, and possibly on the pixel itself
    (handling of high data rates, analog-to digital conversion, sparsification,…)

- Improve sensor performance:
  - ➔ improve the quality of the sensor substrate and the charge collecting properties of sensing electrodes
    (increase efficiency, collected charge and signal-to-noise ratio, improve radiation tolerance,…)

Deep N-Well (DNW) sensor concept

New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential

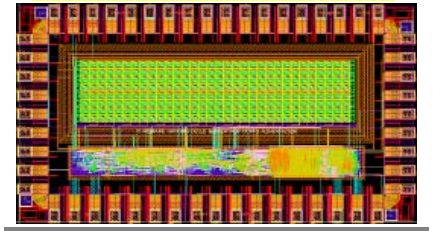


Classical optimum signal processing chain for capacitive detectors can be implemented at pixel level:

- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss to competitive N-wells where PMOSFETs are located
- Fill factor = DNW/total n-well area ~90% in the prototype test structures

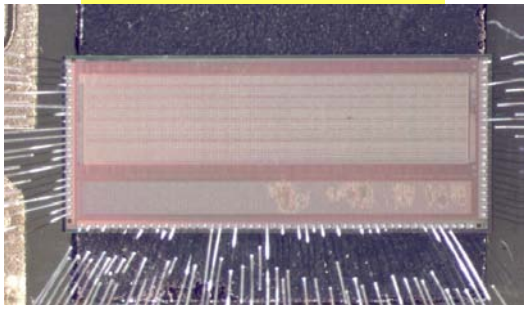
130 nm DNW MAPS: first generation of CMOS sensors with in-pixel sparsification and time stamping

APSEL3D



8x32 matrix.
Shielded pixel
Data Driven
sparsified readout

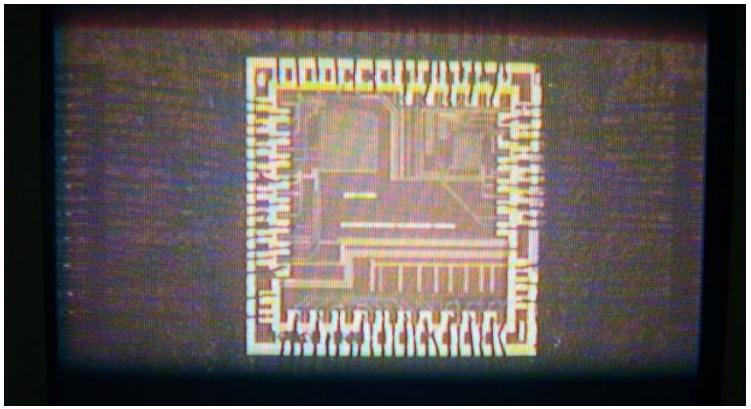
APSEL4D



32x128 matrix.
Data Driven,
continuously operating
sparsified readout
Beam test Sep. 2008

50x50 um pitch

SDR0



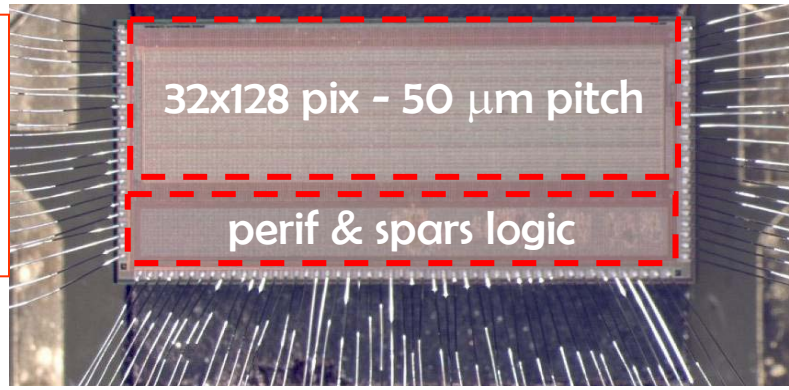
16x16 matrix + smaller test structures.
Intertrain sparsified readout

25x25 um pitch

APSEL4D

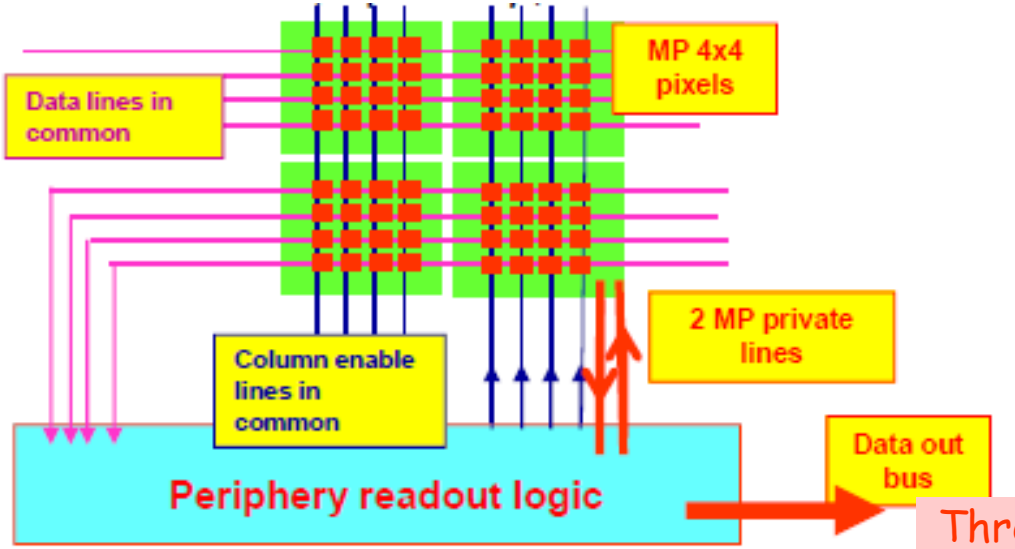
In the active sensor area we minimized:

- logical blocks with PMOS to reduce the area of competitive n-wells
- digital lines for point to point connections to allow scalability of the architecture with matrix dimensions



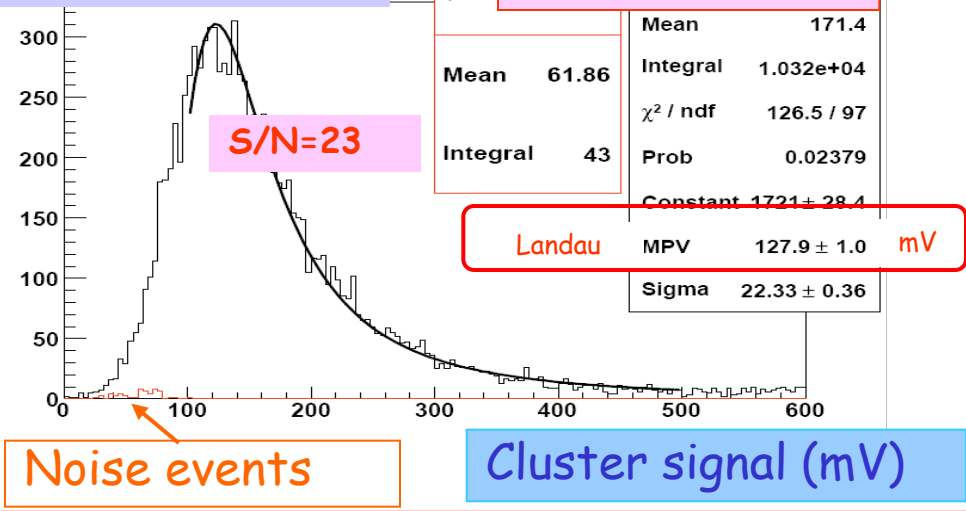
- 4K(32x128) 50x50 μm² matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:
  - Register hit MP & store timestamp
  - Enable MP readout
  - Receive, sparsify, format data to output bus

- S/N ~ 20 with power consumption ~ 30 μW/ch



^{90}Sr electrons

Signal for MIP (MPV) =980e-



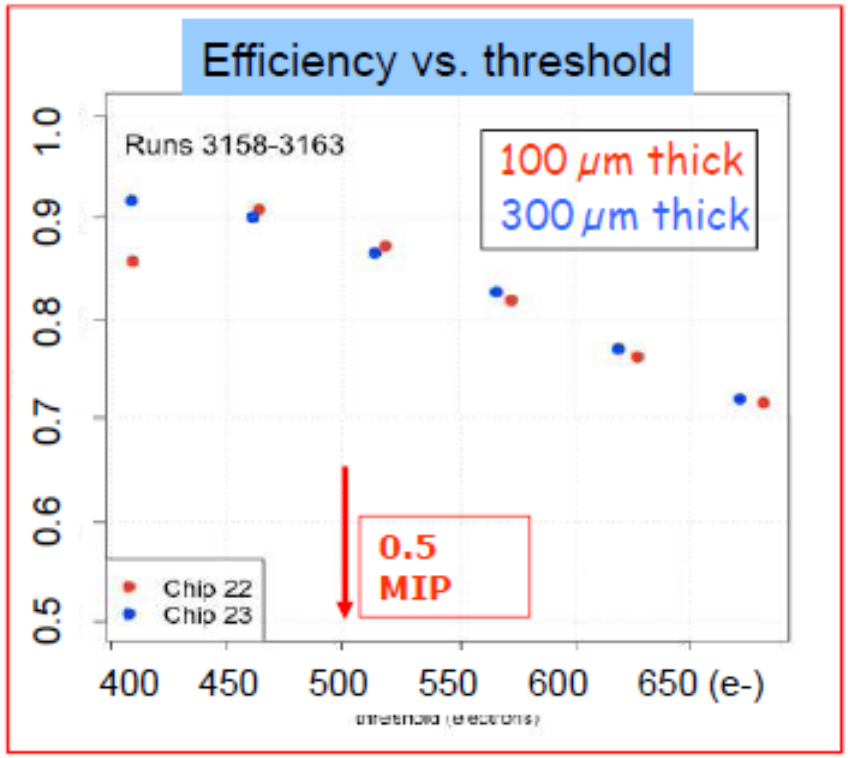
Noise events

Cluster signal (mV)

Threshold dispersion = 60 e-

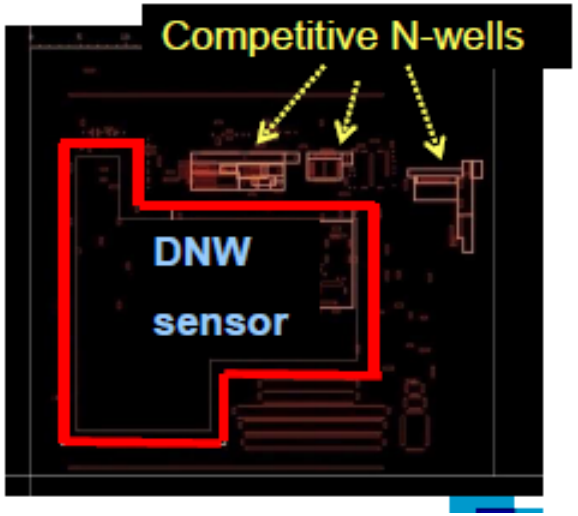
Gain = 860 mV/fC

DNW MAPS Hit Efficiency measured in a CERN beam test (APSEL4D)



Measured with tracks reconstructed with the reference telescope extrapolated on MAPS matrix

- MAPS hit efficiency up to 92 % with threshold @ 400 e- (~ 4σ_noise+2σ_thr_disp)
- 300 and 100 μm thick chips give similar results
- Intrinsic resolution ~ 14 μm compatible with digital readout.



- Competitive N-wells (PMOS) in pixel cell can steal charge reducing the hit efficiency

MAPS and Vertical Integration

Interconnection between 2 (or more) CMOS layers:

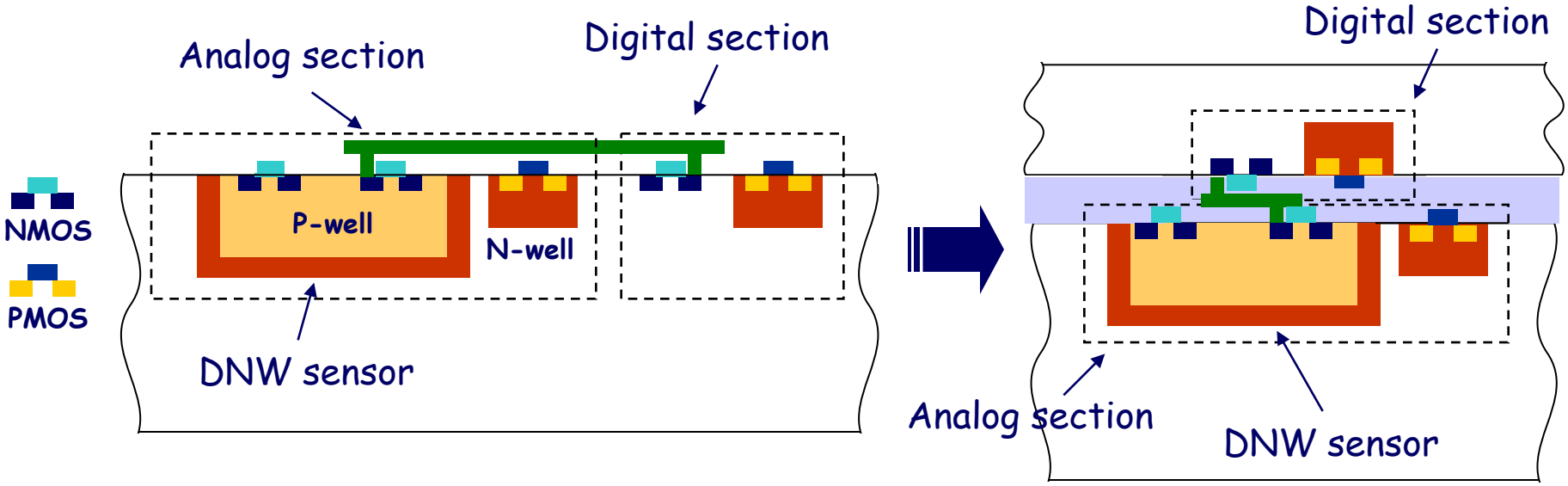
one layer with a MAPS (DNW) device and analog front-end, and the other layer(s) with the digital readout

may overcome limitations typically associated to MAPS:

⇒ shrink pixel size
⇒ remove digital PMOSFETs form the sensor layer, drastically reducing the area of competitive N-wells and improving detection efficiency
⇒ reduce digital interferences, since digital electronics is located in a dedicated layer, different from the layer housing the sensor and the analog
⇒ remove layout constraints on readout architecture

From 2D to 3D CMOS pixel sensors

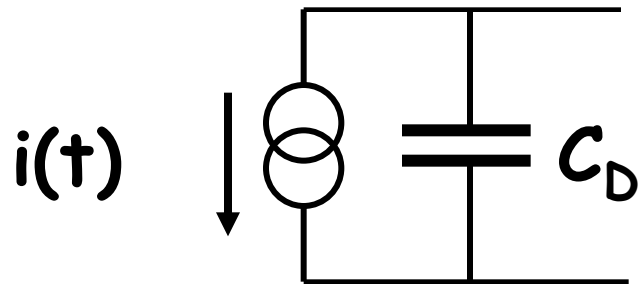
- Guideline: separate analog from digital section to minimize cross-talk between digital blocks and sensor/analog circuits



- Tier 1: collecting electrode (deep N-well/P-substrate junction) and analog front-end and discriminator
- Tier 2: digital front-end (2 latches for hit storage, pixel-level digital blocks for sparsification, 2 time stamp registers, kill mask) and digital back-end (X and Y registers, time stamp line drivers, serializer)

Acquiring the signal from the sensor: the charge-sensitive preamplifier

- The detector signal is a current pulse i(t) of short duration
- The physical quantity of interest is the deposited energy, so one has to integrate the sensor signal

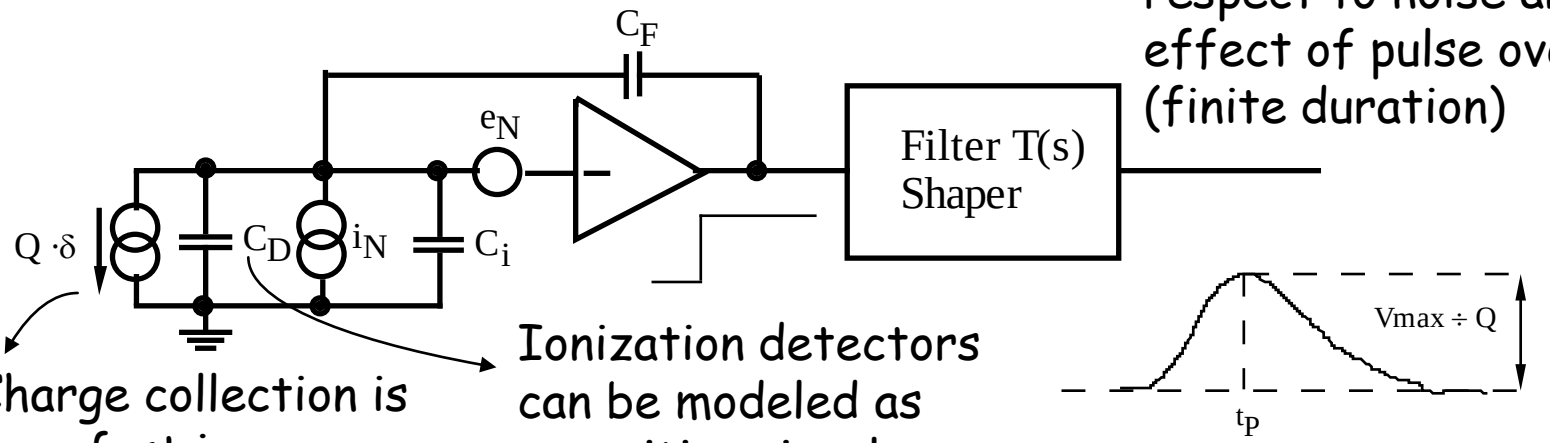


$$E_S \div Q_S = \int i(t)dt$$

- The detector capacitance C_D is dependent on geometry (e.g. strip length or pixel size), biasing conditions (full or partial depletion), aging (irradiation)
- Use an integrating preamplifier (charge-sensitive preamplifier), so that charge sensitivity ("gain") is independent of sensor parameters

Charge measuring system and the effect of noise

Filter minimizes the measurement error with respect to noise and the effect of pulse overlap (finite duration)



Charge collection is very fast in semiconductor detectors

Ionization detectors can be modeled as capacitive signal sources

Noise arises from two uncorrelated sources at the input (series and parallel noise):

$$S_{e_N}(\omega) = A_W + \frac{A_f}{f} \qquad S_{I_N}(\omega) = B_W$$

Noise sources

White series noise

$$A_W = 4kT\frac{\Gamma}{g_m}$$

White noise in the main current (drain, collector) of the input device

other components in the input stage

stray resistances in series with the input

1/f series noise

$$A_{1/f} = \frac{A_f}{f}$$

1/f component in the drain current

White parallel noise

$$B_W = 2qI_{\det} + 2qI_{G(B)} + \frac{4kT}{R}$$

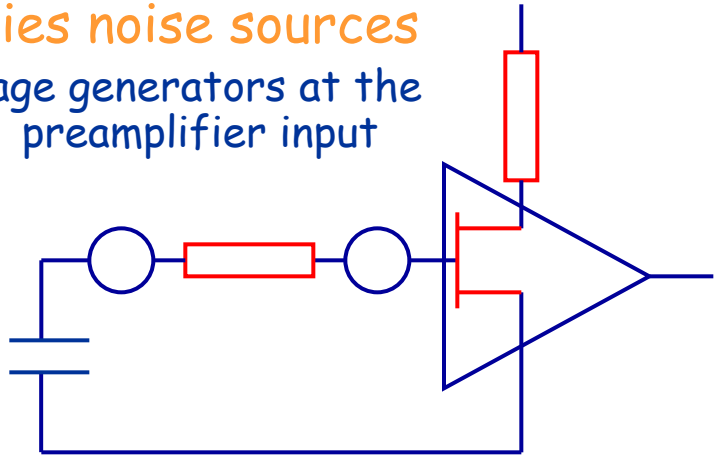
Shot noise in detector leakage current

shot noise in input device gate (base) current

thermal noise in feedback resistor

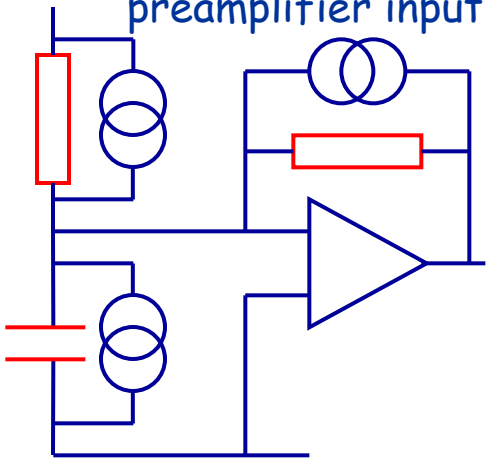
Series noise sources

Voltage generators at the preamplifier input

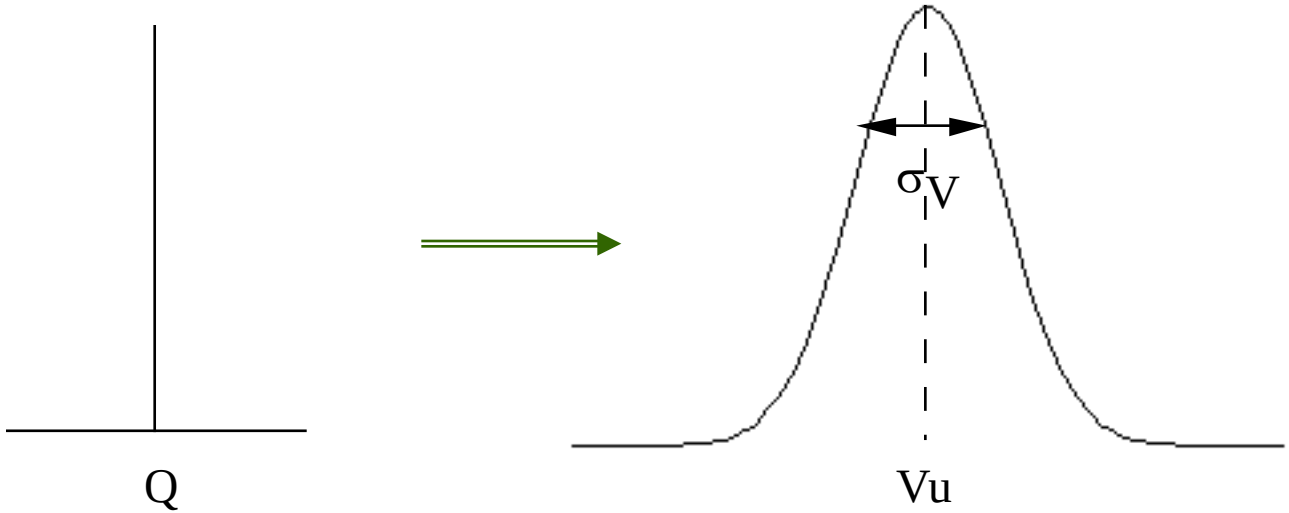


Parallel noise sources

Current generators at the preamplifier input



Effect of electronic noise on charge measurements

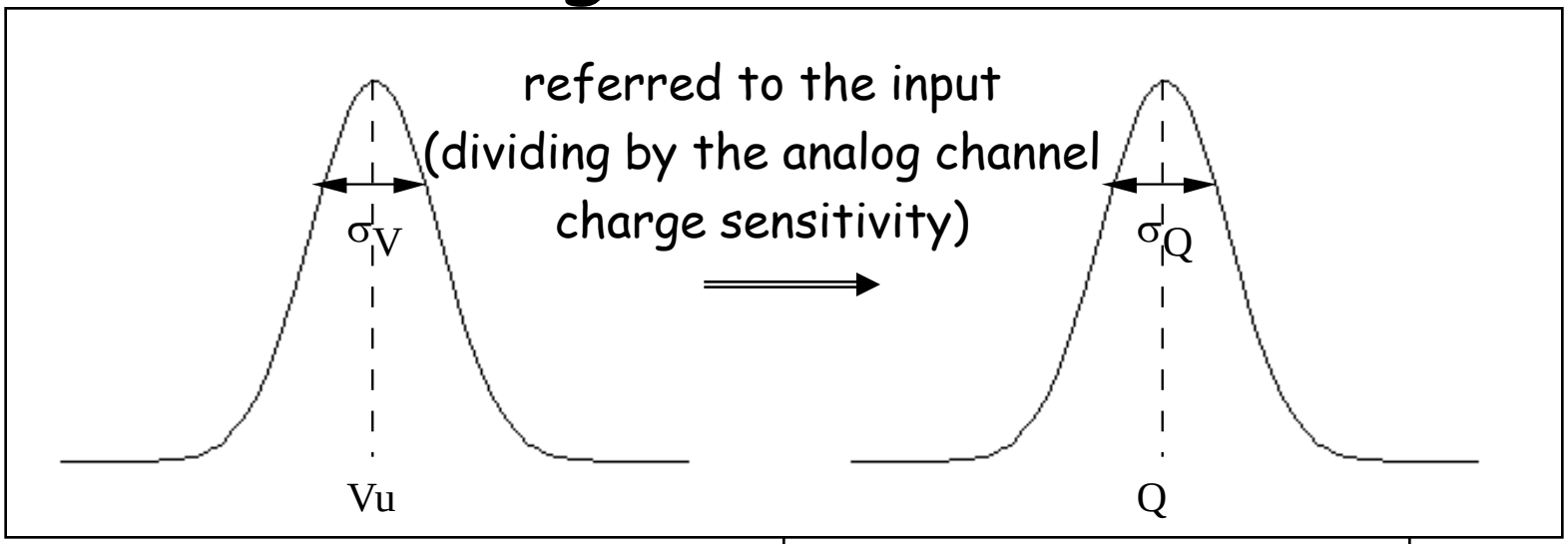


Ideally indefinitely narrow distribution of detector charge (neglecting statistics in energy deposition and charge creation)

Broadening of pulse amplitude distribution at the shaper output due to electronic noise

Because of electronic noise, the signal amplitude at the shaper output has a Gaussian probability density function

Effect of electronic noise on charge measurements



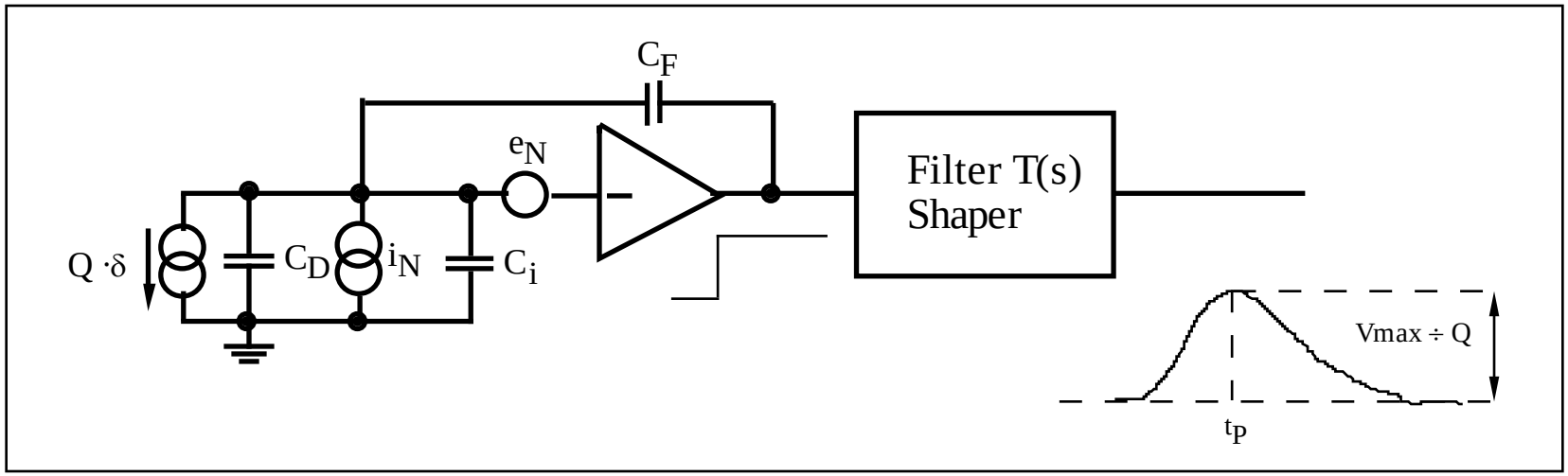
The signal amplitude at the output of the linear analog channel is characterized by a Gaussian probability density function

$$S/N = \frac{V_u}{\sigma_V} = \frac{Q}{\sigma_Q} = \frac{Q}{ENC} = \eta_Q$$

Equivalent Noise Charge = standard deviation in the charge measurement

charge injected at the input producing at the output of the linear processor a signal whose amplitude equals the root mean square output noise

Equivalent Noise Charge (ENC)



The mean square value of the noise voltage at the shaper output can be calculated as follows:

$$\overline{v_{u,N}^2} = \int_0^\infty S_u(\omega)df = \int_0^\infty \left[\left|T_{e_N}(j\omega)\right|^2 \cdot S_{e_N}(\omega) + \left|T_{I_N}(j\omega)\right|^2 \cdot S_{I_N}(\omega) \right] df$$

$$= \int_0^\infty \left[\left|T(j\omega)\right|^2 \cdot \frac{(C_D + C_i + C_F)^2}{C_F^2} \left(A_W + \frac{A_f}{f} \right) + \left|T(j\omega)\right|^2 \frac{1}{\omega^2 C_F^2} \cdot B_W \right] df =$$

Equivalent Noise Charge (ENC)

$$= A_W \frac{(C_D + C_i + C_F)^2}{C_F^2} \frac{1}{2\pi} \int_0^\infty |T(j\omega)|^2 d\omega +$$

$$+ A_f \frac{(C_D + C_i + C_F)^2}{C_F^2} \int_0^\infty \frac{|T(j\omega)|^2}{\omega} d\omega + B_W \frac{1}{C_F^2} \frac{1}{2\pi} \int_0^\infty \frac{|T(j\omega)|^2}{\omega^2} d\omega$$

$$\frac{1}{2\pi} \int_0^\infty |T(j\omega)|^2 d\omega = \frac{A_1}{t_P}$$

$$\int_0^\infty \frac{|T(j\omega)|^2}{\omega} d\omega = A_2$$

$$\frac{1}{2\pi} \int_0^\infty \frac{|T(j\omega)|^2}{\omega^2} d\omega = A_3 t_P$$

t_P = peaking time of the signal at the shaper output

A_1, A_2, A_3 = filter-dependent coefficients

Equivalent Noise Charge (ENC)

$$ENC = \frac{\sqrt{\overline{v_{u,N}^2}}}{Charge \quad sensitivity}$$

$$ENC^2 = \overline{v_{u,N}^2} \cdot C_F^2 = A_W (C_D + C_i + C_F)^2 \frac{A_1}{t_P} + A_f (C_D + C_i + C_F)^2 A_2 + B_W A_3 t_P$$

$C_T = C_D + C_i + C_F$

= total capacitance at the preamplifier input

In a well designed preamplifier, the noise is determined by the input device.

Equivalent Noise Charge (ENC)

$$ENC^2 = A_W C_T^2 \frac{A_1}{t_P} + A_f C_T^2 A_2 + B_W A_3 t_P$$

White series noise:

Neglecting noise in parasitic resistors:

$$A_W = 4kT \frac{\Gamma}{g_m}$$

$\Gamma = 0.5$ (BJT)

$\Gamma = 2/3$ (Long channel FETs)

$\Gamma \approx 1$ (Short-channel FETs)

White parallel noise:

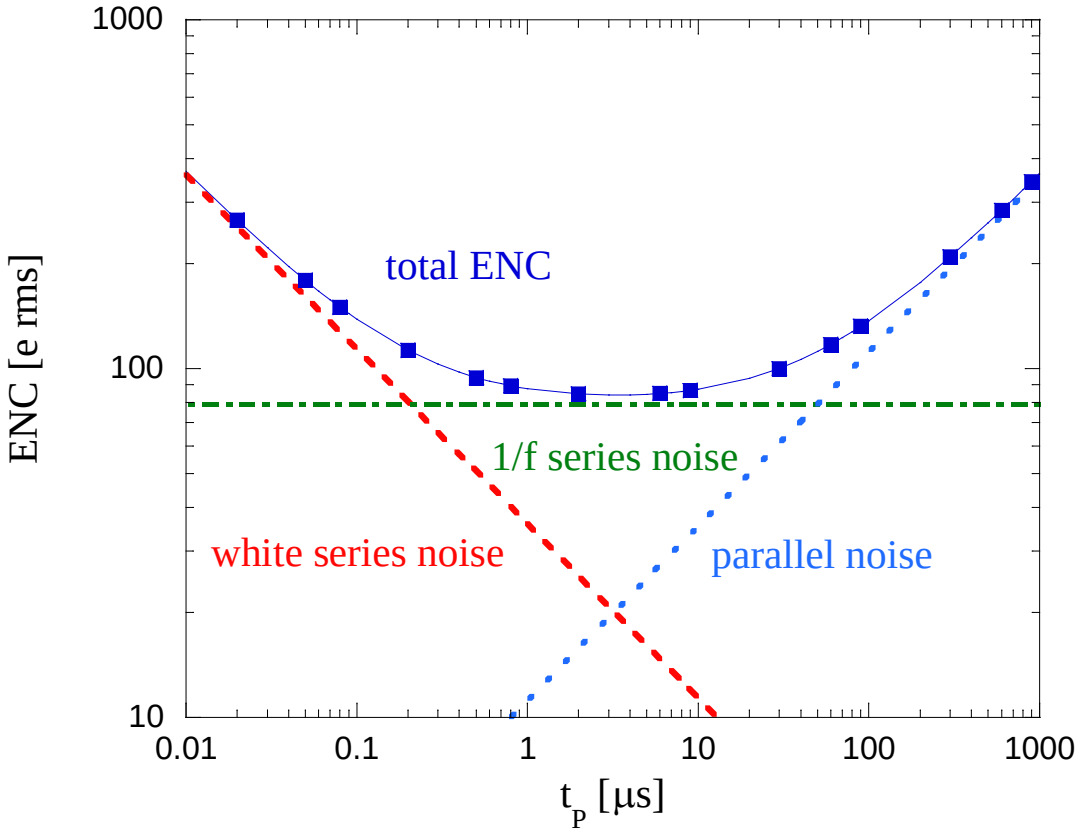
$$B_W = 2qI$$

$I = I_B$ (BJT)

$I = I_G$ (gate tunneling current in nanoscale CMOS)

$I = I_{leak}$ Detector leakage current

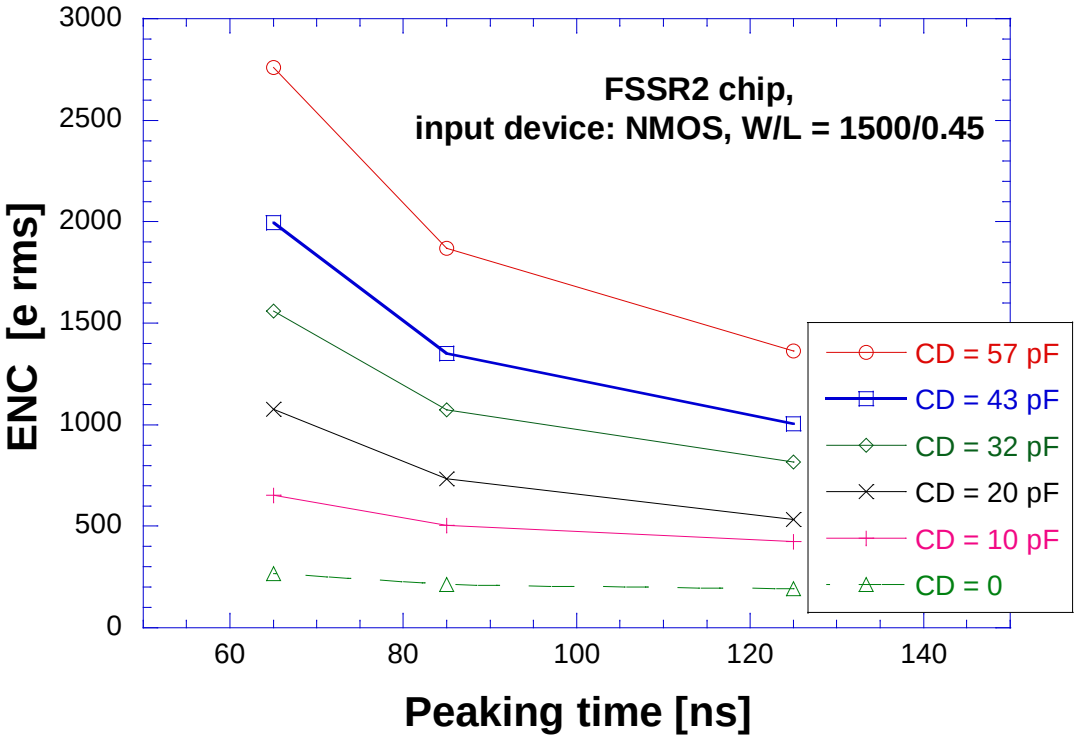
- In trackers for high luminosity colliders, event rate is very high, and the peaking time has to be short (< 100 ns).
- White series noise is usually dominant here, except with irradiated sensors, where leakage current (and the associated shot noise) may increase to a very large extent.

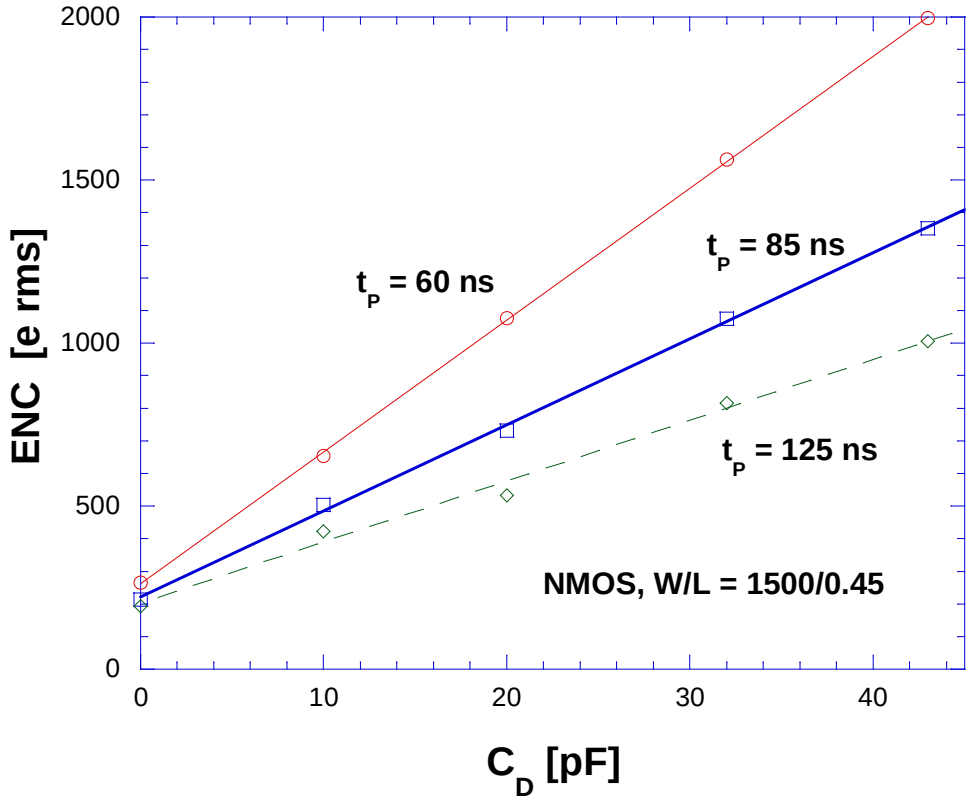


Noise and detector capacitance

White and 1/f series noise terms (dominant in CMOS) give a contribution to ENC linearly increasing with the detector capacitance ($C_T = C_D + C_{IN} + C_F$).

$$ENC^2 = \left(A_W \frac{A_1}{t_P} + \frac{K_f}{C_{OX} W L} A_2 \right) C_T^2$$





Noise and power dissipation; shrinking pixel size by going 3D

At short peaking times, white series noise is dominant;

We commonly operate at low power, and MOSFETs are biased in weak inversion, where their transconductance is proportional to the drain current:

$$ENC^2 = \left(A_W \frac{A_1}{t_P} \right) C_T^2 = \frac{4kT\Gamma}{g_m} \frac{A_1}{t_P} C_T^2 \div \frac{C_T^2}{I_D}$$

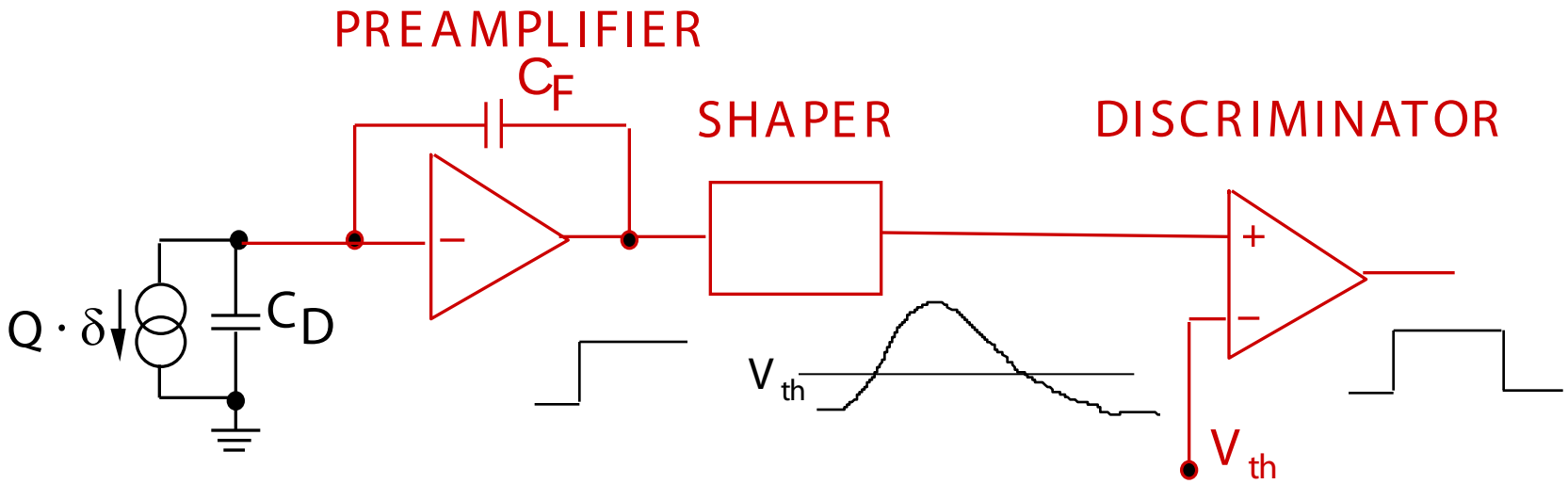
At a given noise, $I_D \div C^2$

Since power dissipation P_D is proportional to I_D: $P_D \div C^2$

Scaling pixel size helps reducing power and/or noise

Extracting a hit information from the sensor signal: the discriminator

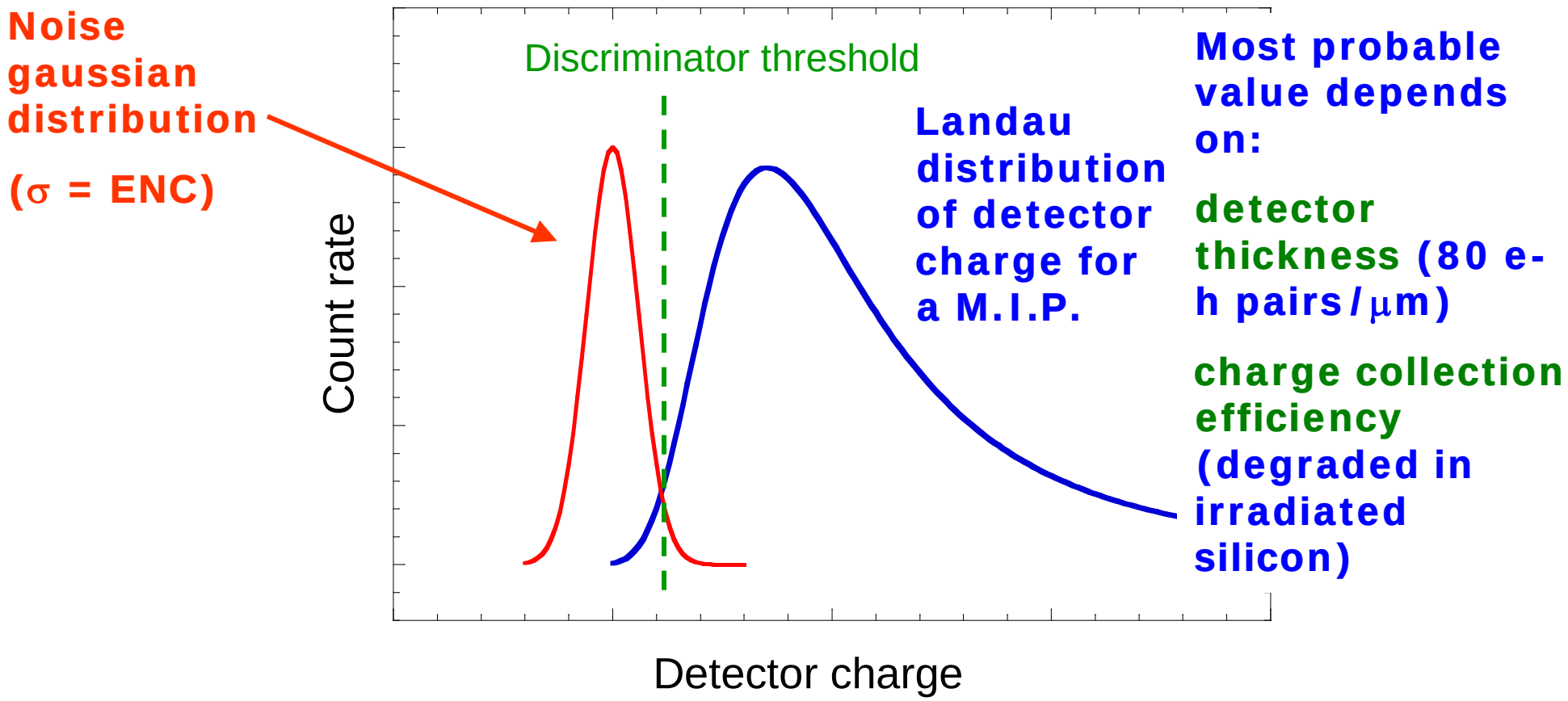
- Binary readout: hit/no hit information from a discriminator
- This can also be associated to an ADC system, providing an information about the charge delivered by the detector



- In a multichannel readout chip, channel-to-channel threshold variations due to device mismatch may degrade detection efficiency and spurious hit rate

Efficiency and noise occupancy

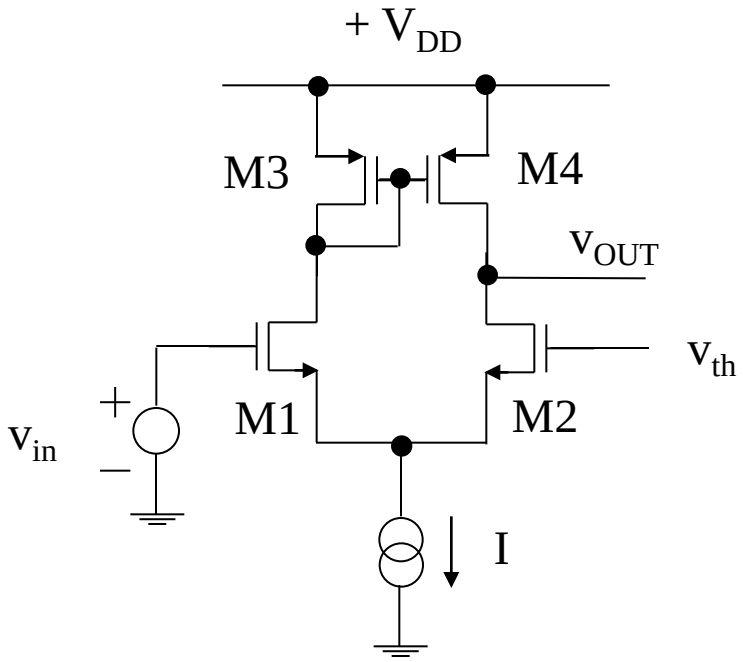
- An excessive threshold dispersion can lead to channels with high noise hit rate or reduced efficiency in signal detection.



Threshold dispersion

- Discriminator threshold dispersion is given by statistical variations of the threshold voltage of MOSFETs in the differential pairs used in the discriminator input stage:

$$\sigma^2(\Delta V_{th}) = \frac{A_{vth}^2}{WL}$$



Large area transistors help reduce the effect of threshold mismatch

- As for the noise, the discriminator threshold and its dispersion (divided by the analog channel charge sensitivity) can be treated in term of input-referred charges, Q_{th} and σ_{qth} respectively.

- For a second-order semigaussian shaper, and series white noise as the dominant contribution to ENC, the frequency of noise hits can be calculated as:

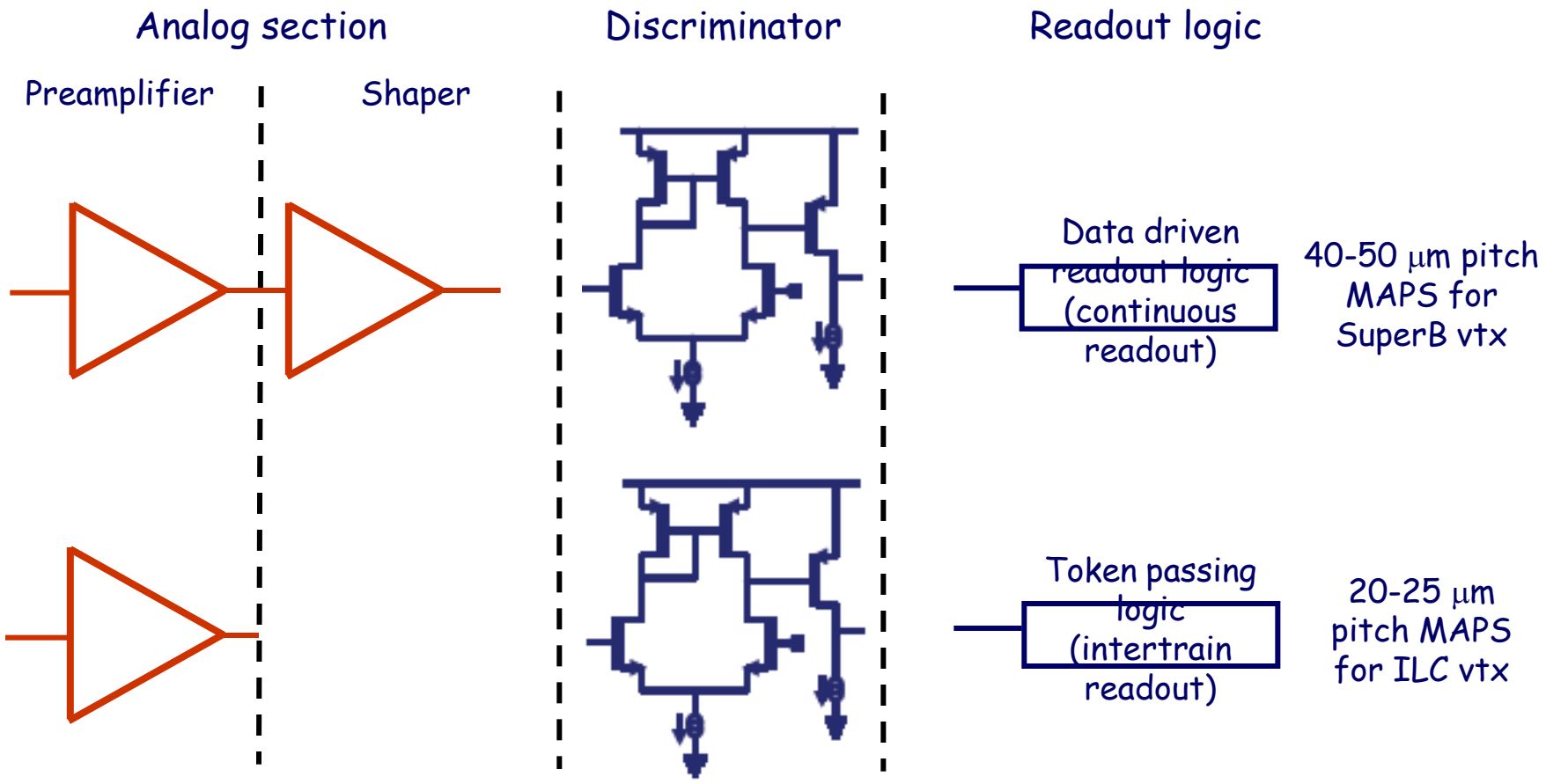
$$f_n = \frac{\sqrt{3}}{\pi t_p} e^{-\frac{Q_{th}^2}{2ENC^2}}$$

- In practical conditions, the number of noise hits can be kept at acceptably low values by satisfying this condition:

$$Q_{th}^{sig} > 4\left(ENC + \sigma_{qth}\right)$$

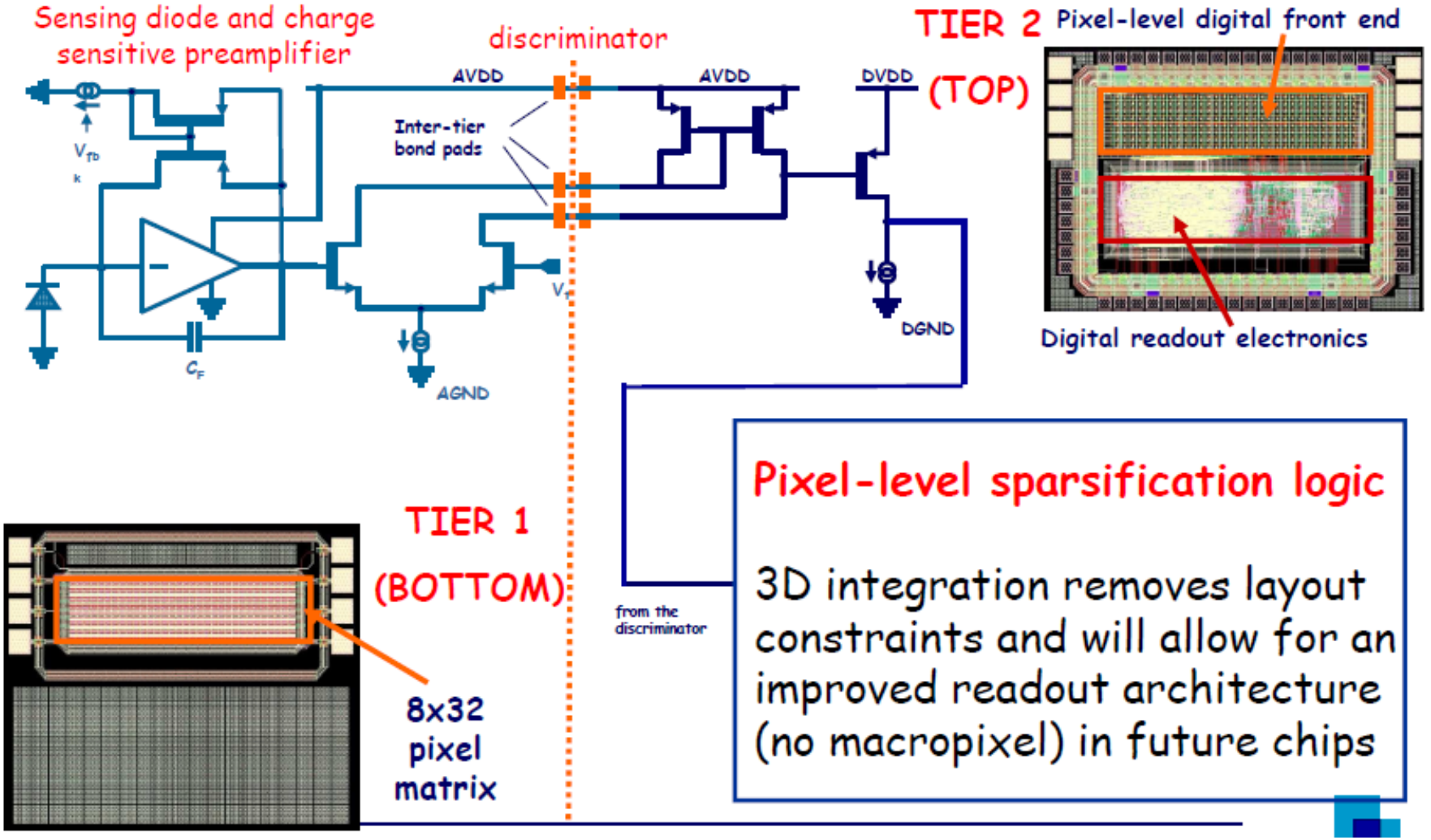
- To maintain an adequate efficiency, a channel-by-channel threshold adjustment may be necessary (threshold DAC in the pixel cell)

Pixel-level front-end electronics



- Fully CMOS analog and digital FE (more than a hundred transistors per pixel)

Readout electronics in a 40 x 40 μm² 3D MAPS pixel cell

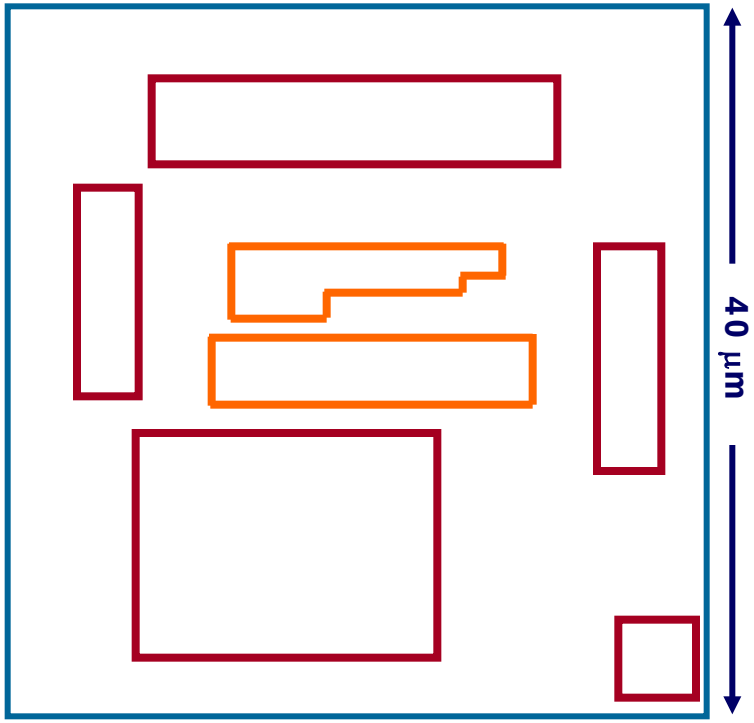


Analog design aimed at minimizing the number and size of PMOS devices in the sensor layer

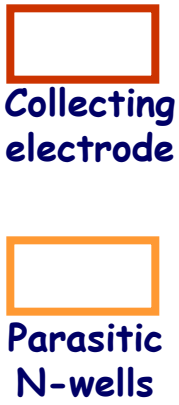
Only preamplifier PMOS devices are kept in the analog layer (TIER 1)

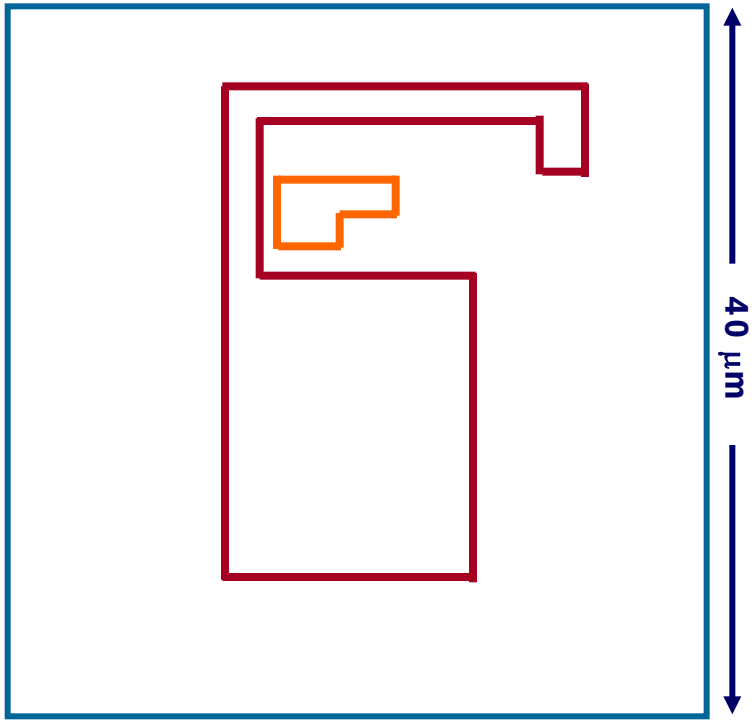
Collecting electrode layout

- Adoption of a three-dimensional technology makes it possible to significantly reduce the area covered by charge stealing N-wells → significant improvement in charge collection efficiency expected



Apsel5T cell (planar CMOS technology)

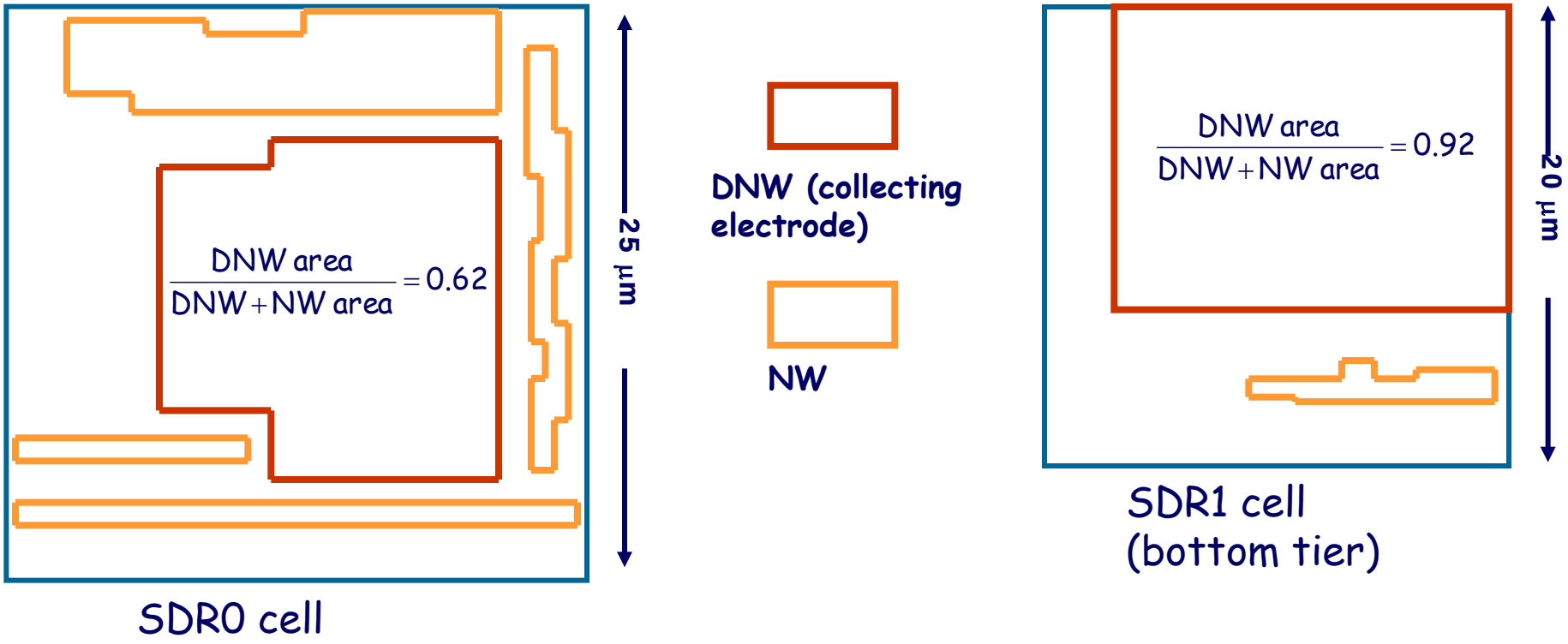




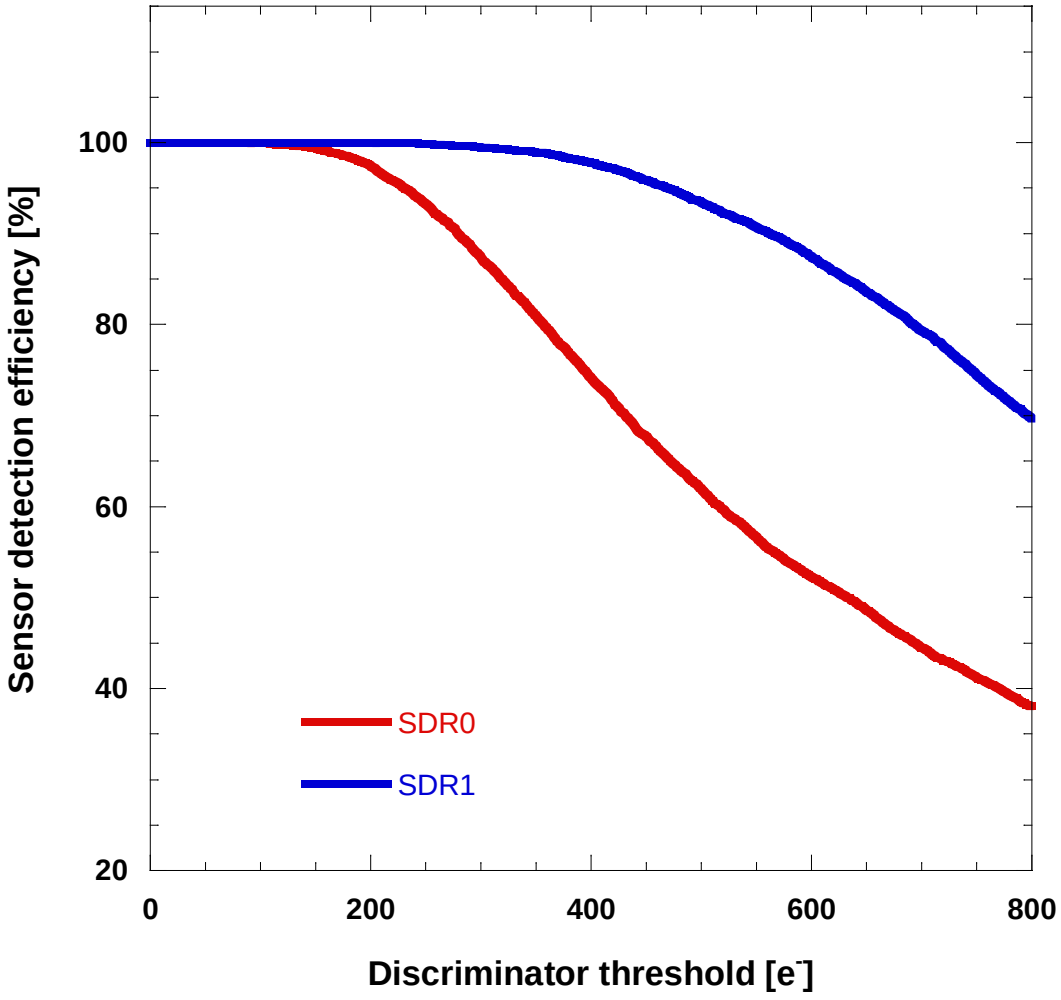
Apsel_3D cell (vertical integration CMOS technology)

Collecting electrode layout shrinks in the 3D version…

- Moving most of the PMOS transistors to the top (digital) tier may significantly improve the detector collection efficiency
- The DNW covers about 35% of the cell area in the SDR0 chip, more than 50% in its 3D release

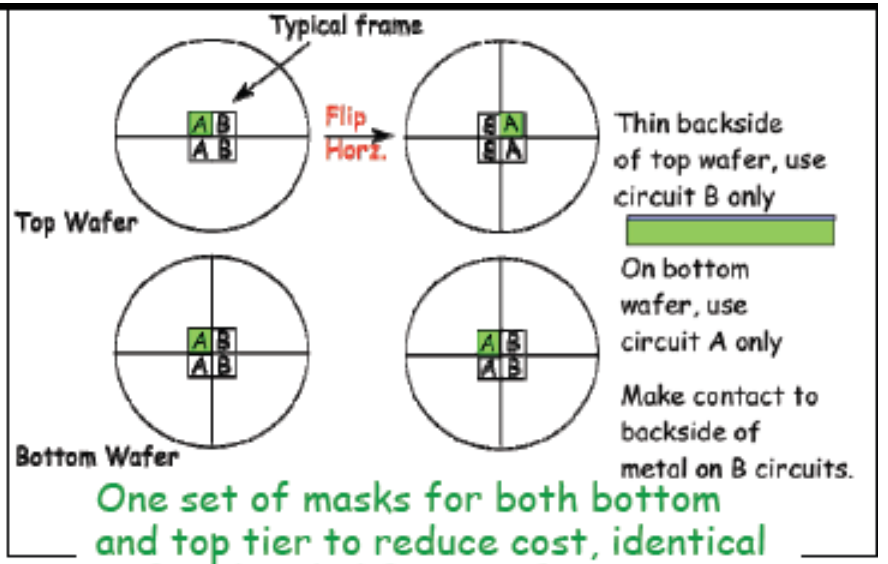


…and detection efficiency is much better in the 3D MAPS



First 3D-IC Tezzaron Multiproject Run 5

Broad range of architectures and applications (more than 25 designs)



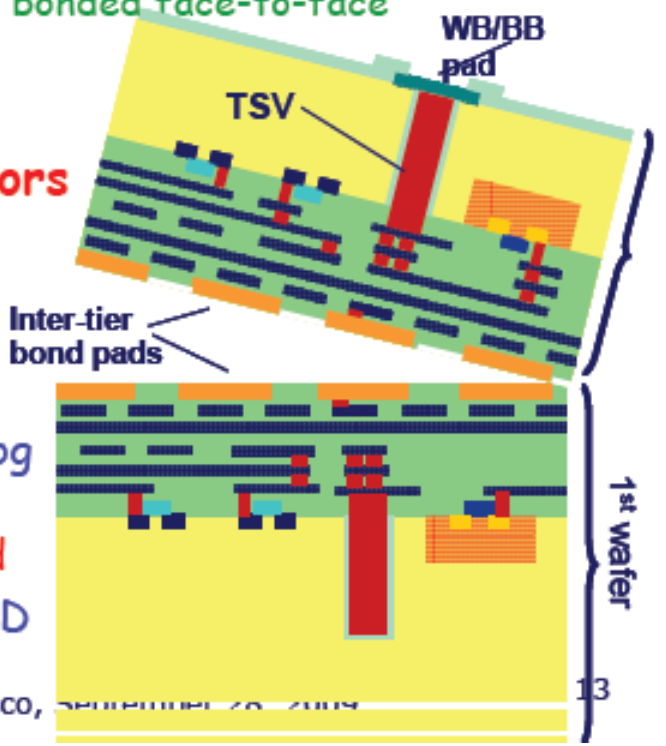
One set of masks for both bottom and top tier to reduce cost, identical wafers bonded face-to-face

MAPS

- Convert 2D MAPS device to a full CMOS 3D design, with digital readout separated from the sensor and the analog front-end – Italy, France

Readout chips for high resistivity pixel sensors

- Convert MIT LL 3D SOI design to the Tezzaron/Chartered process – Fermilab
- Convert current 0.25 μm readout pixel electronics to a 3D structure with separate analog and digital tiers – France/US
- X-ray imaging/timing chip - Fermilab/BNL/Poland
- 3D chip with structures to test feasibility of a 3D integrated stacked trigger layer. - Fermilab



Valerio Re - IEEE 3D-IC Conference, San Francisco, [illegible]

13

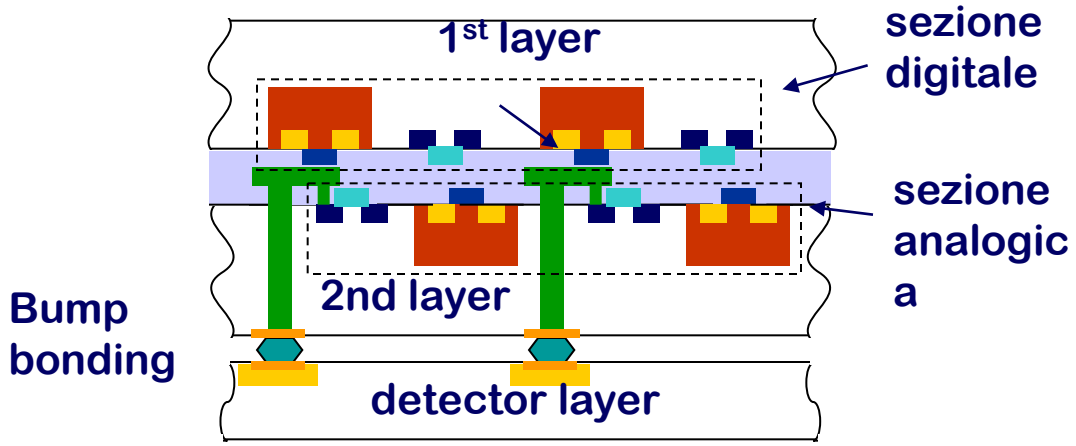
High resistivity sensors and vertical integration

- Much better sensor properties with respect to bulk CMOS MAPS (larger and faster signal, radiation hardness,…).
- Material budget (> 1% X_0) and pitch of present HEP hybrid pixel systems is too large for SuperB or ILC applications
- Vertical integration will help reduce pixel pitch and interconnection material
- A much better S/N vs. power dissipation vs. speed operating point should be attained with respect to MAPS

Vertical Integration of CMOS Readout Electronics and High resistivity, fully depleted pixel sensors

1) **Interconnessione con bump bonding fra un chip 3D (processo Tezzaron/Chartered) con l'elettronica di lettura e un sensore ad alta resistività completamente svuotato**

- L'utilizzo di un sensore ad alta resistività presenta evidenti vantaggi per il rapporto segnale-rumore e per la resistenza alle radiazioni.
- Tecnica standard per l'interconnessione fra sensore ed elettronica
- La realizzazione tridimensionale del circuito integrato di lettura può consentire una riduzione delle dimensioni dei pixel (senza ridurne le funzionalità), rendendo ragionevole l'obiettivo di un'area non superiore a 50 μm x 50 μm (SuperB, SLHC,...).

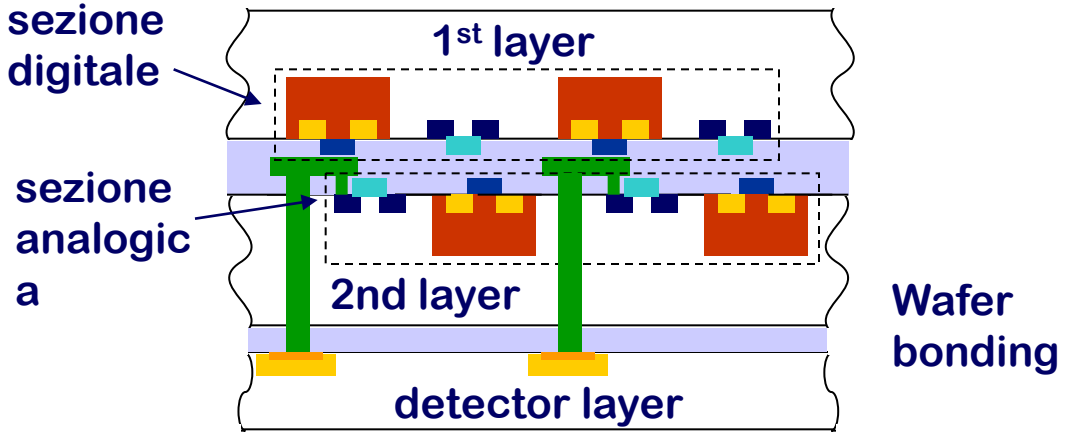


Vertical Integration of CMOS Readout Electronics and High resistivity, fully depleted pixel sensors

2) **Integrazione verticale fra un chip (2D o 3D) con l'elettronica di lettura e un sensore ad alta resistività completamente svuotato**

L'integrazione verticale offre la possibilità di ridurre la quantità di materiale e di ridurre la dimensione dei pixel grazie all'eliminazione del bump bonding.

Va verificata la compatibilità fra processo di integrazione verticale e qualità del sensore ad alta resistività.



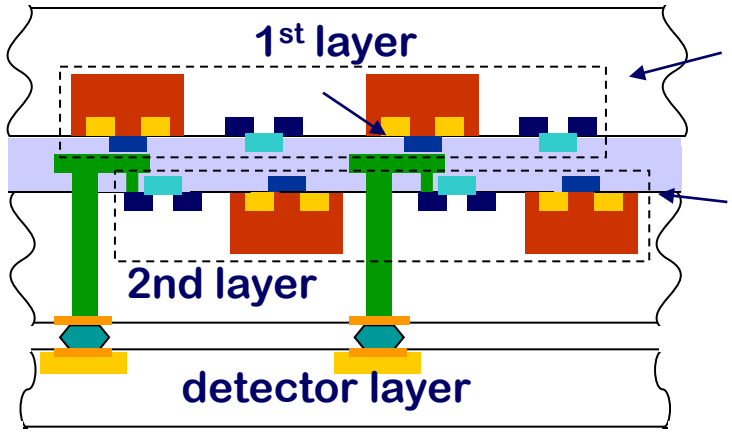
Vertical integration of high resistivity pixels

- Bump bonding can have significant mass and represent a high Xo for fine pitch assemblies or high density interconnects.
- Vertical integration may sizably reduced the amount of material
- Commercially available processes: Ziptronix (USA), IZM – Munich, T-Micro

3D readout integrated circuits interconnected to high resistivity sensors:

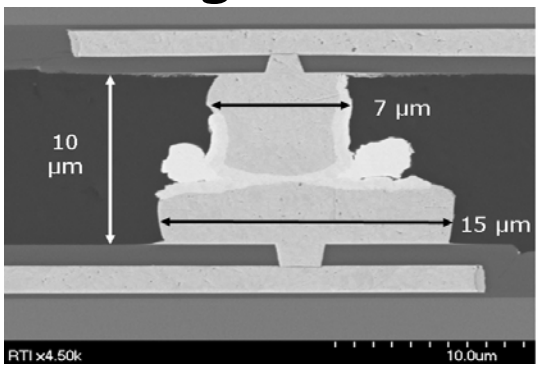
standard bump bonding vs vertical integration

Bump bonding



Digital section

Analog section

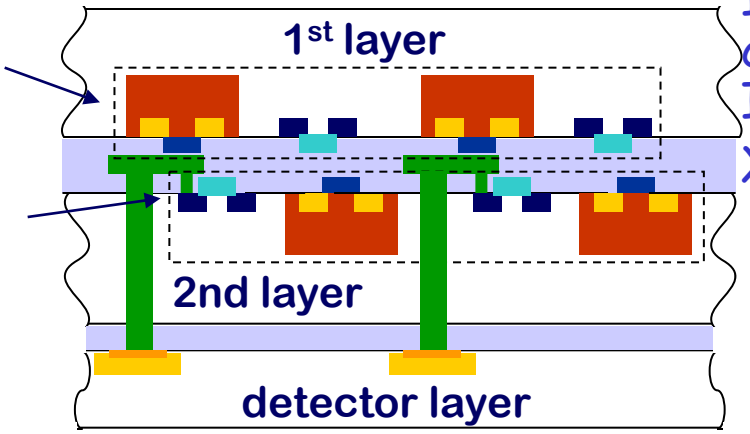


CuSn bond cross section

Conventional solder bumps or more advanced, low pitch CuSn bonding may still pose a problem for low mass assemblies

Digital section

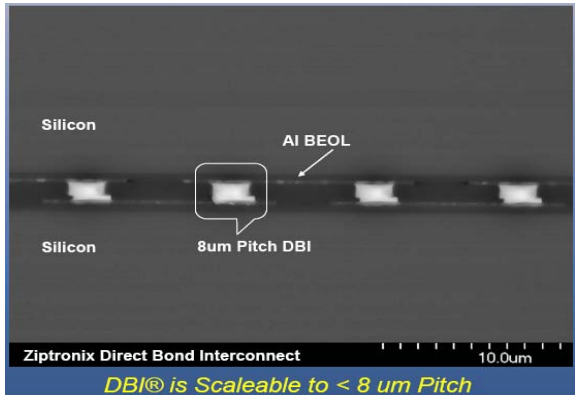
Analog section



Investigate bonding of sensors to readout circuits from the first run using the Direct Bond Interconnect (DBI) process by Ziptronix.

Xo < 0.001%

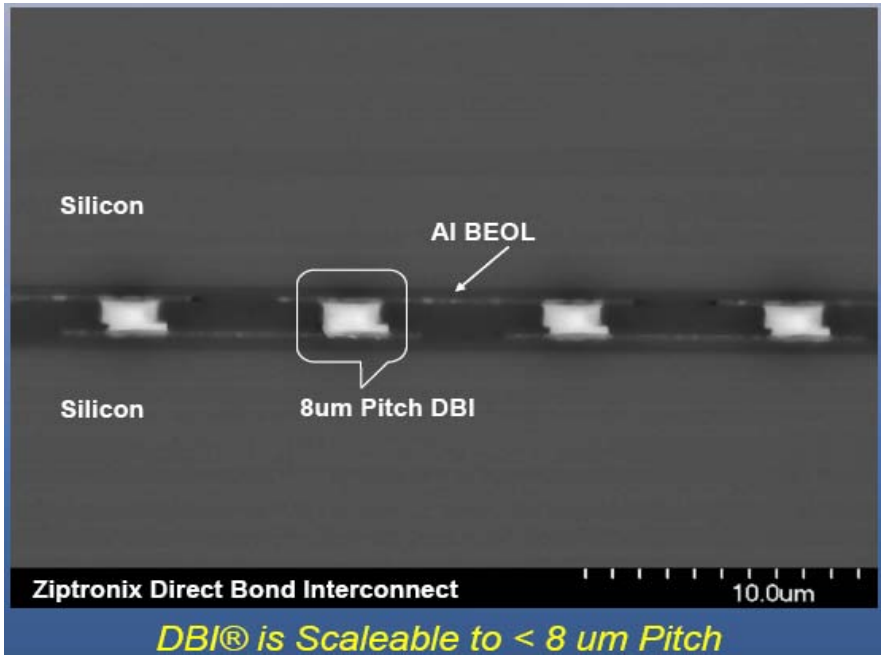
Wafer bonding



Vertical integration between readout chip and fully depleted sensor: Ziptronix

- Some 3D bond processes introduce significant material between bonded layers.
  - Conventional solder bumps or CuSn can pose a problem for low mass fine pitch assemblies

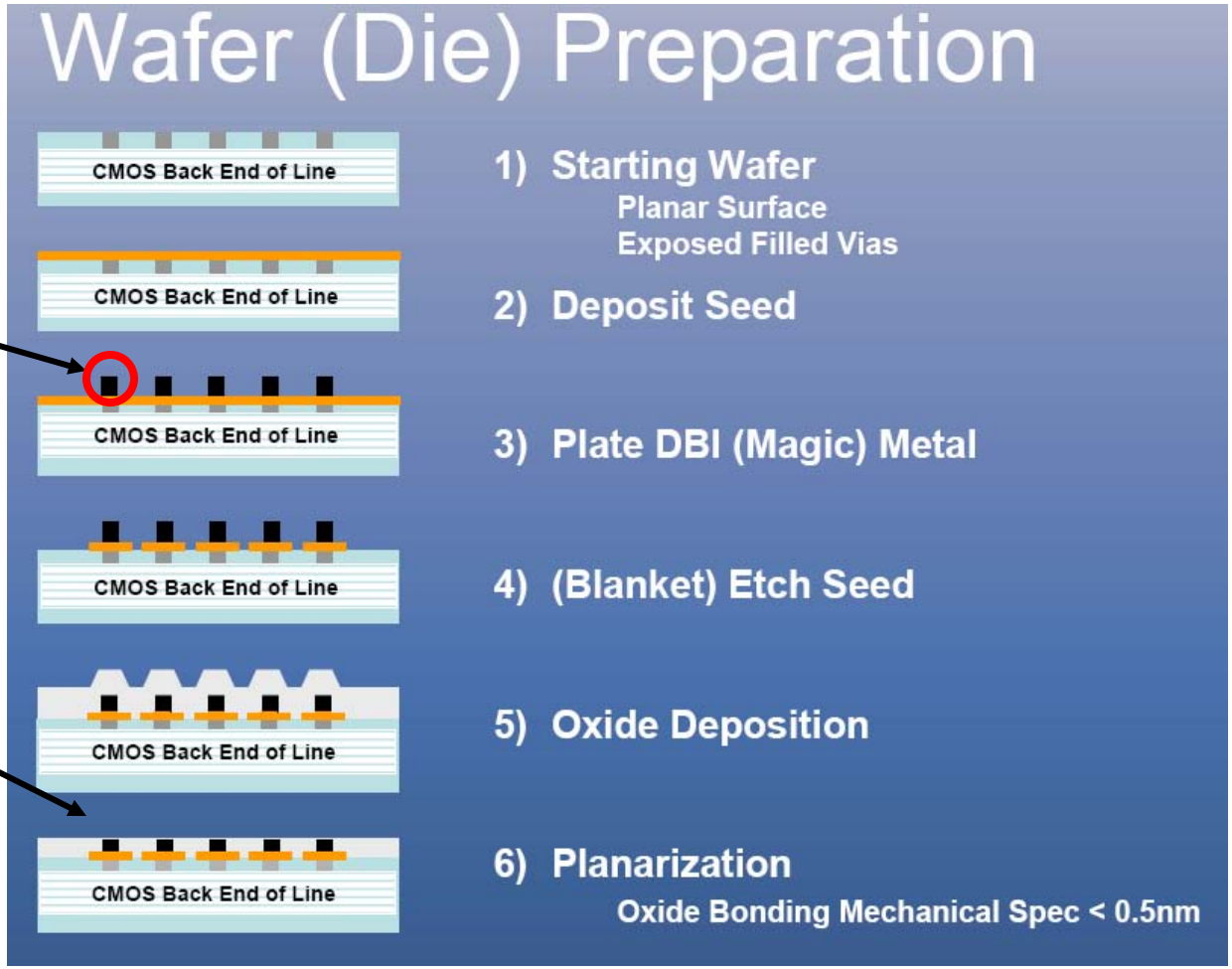
- IC bonding to a detector will be done by Ziptronix using the Direct Bond Interconnect (DBI) process.[6]
  - Xo < 0.001%



- Ziptronix is located in North Carolina
- Orders accepted from international customers

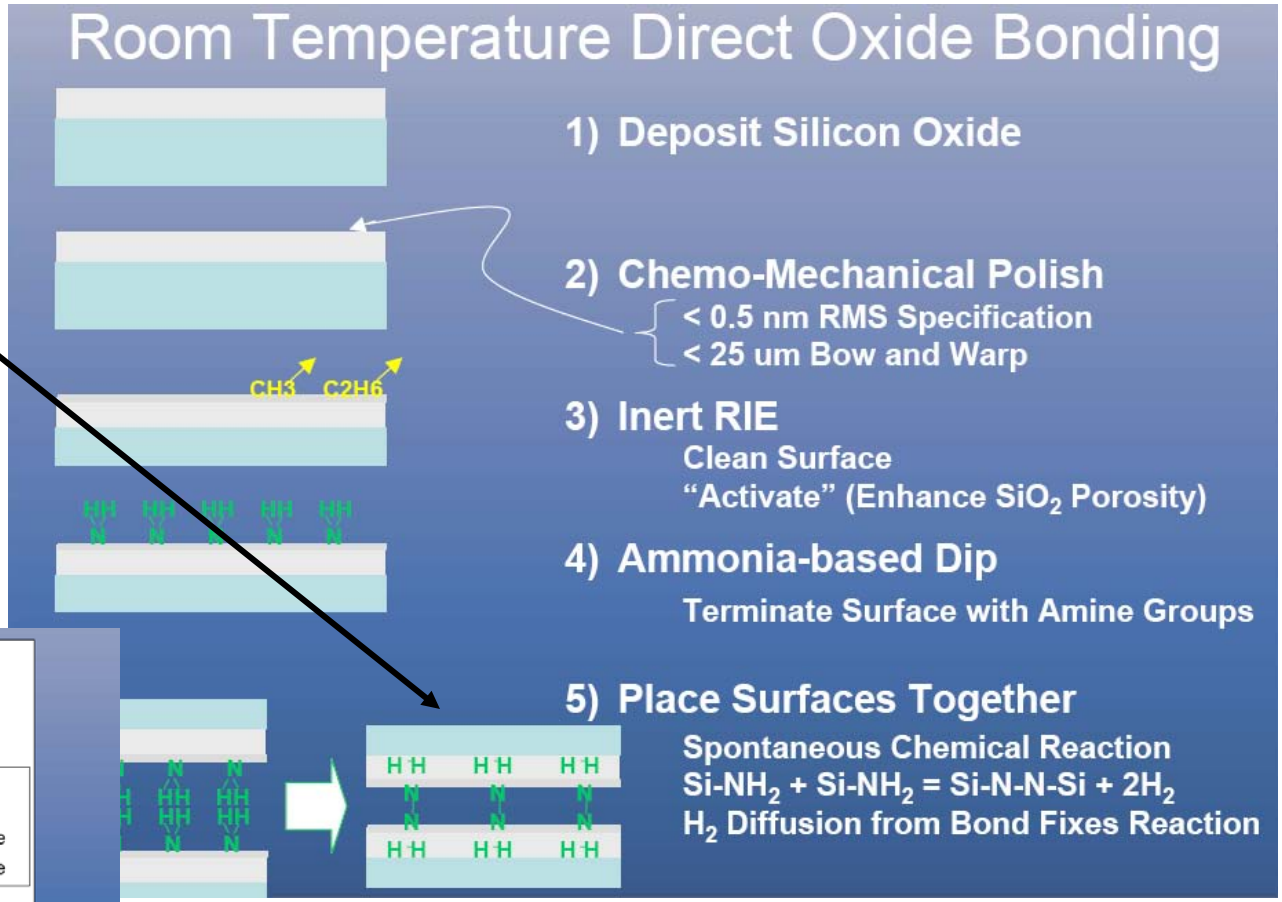
DBI Process from Ziptronix

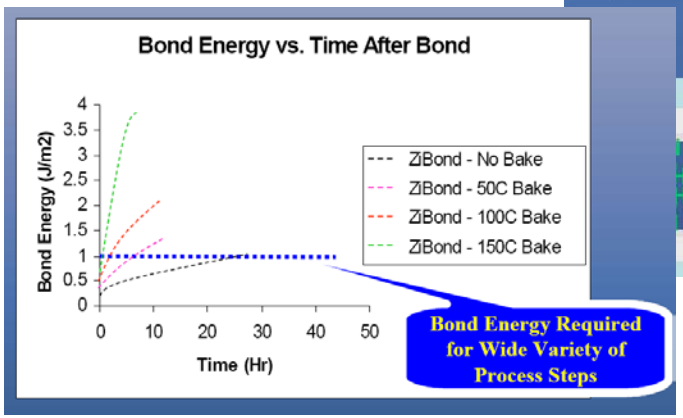
- Add DBI metal for electrical connections
- Prepare surface for oxide bonding



Oxide Bonding

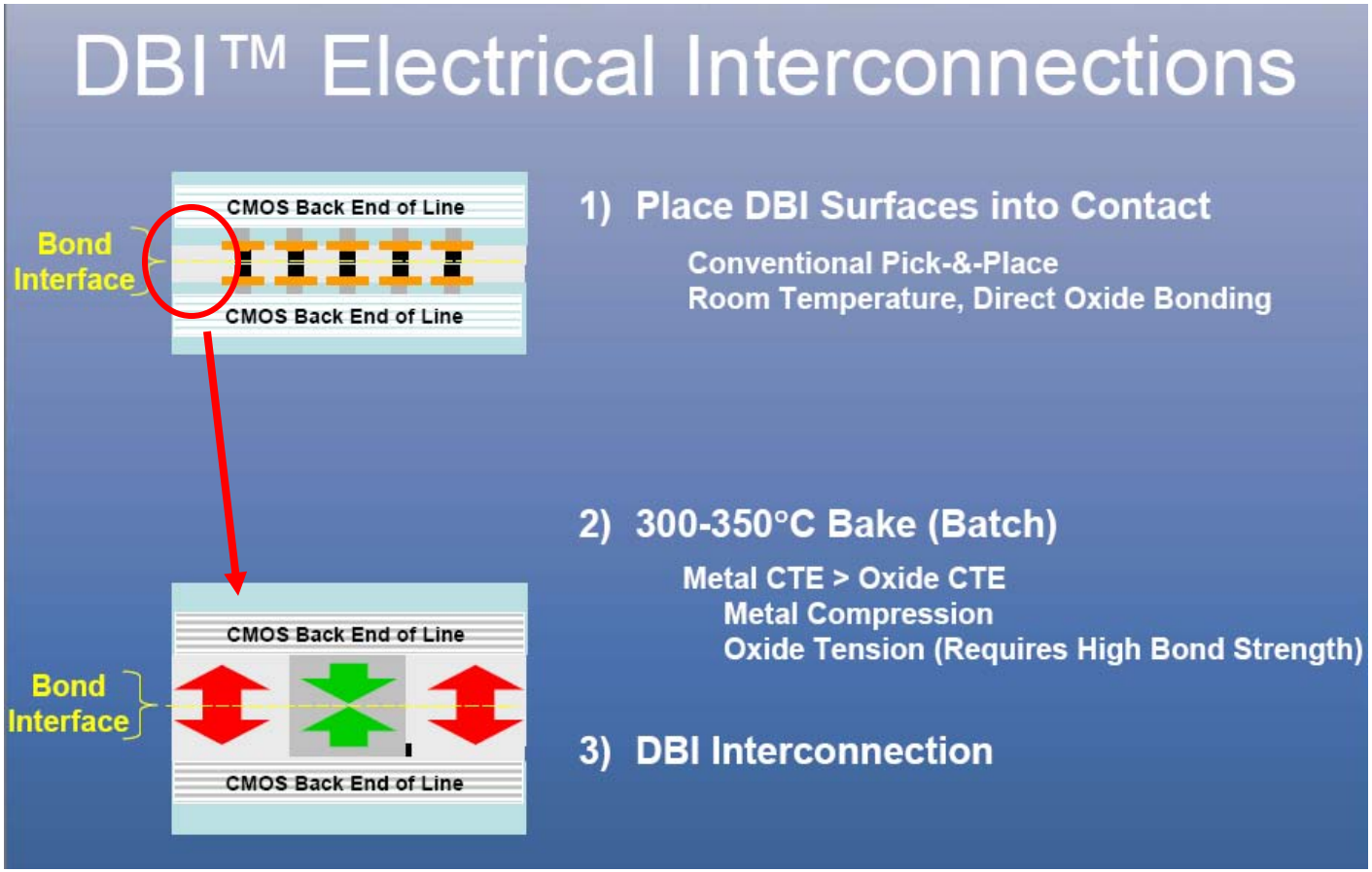
- Surfaces bond immediately due to Van der Waals force.
- Bonding occurs at room temperature
- Bond strength increase with time



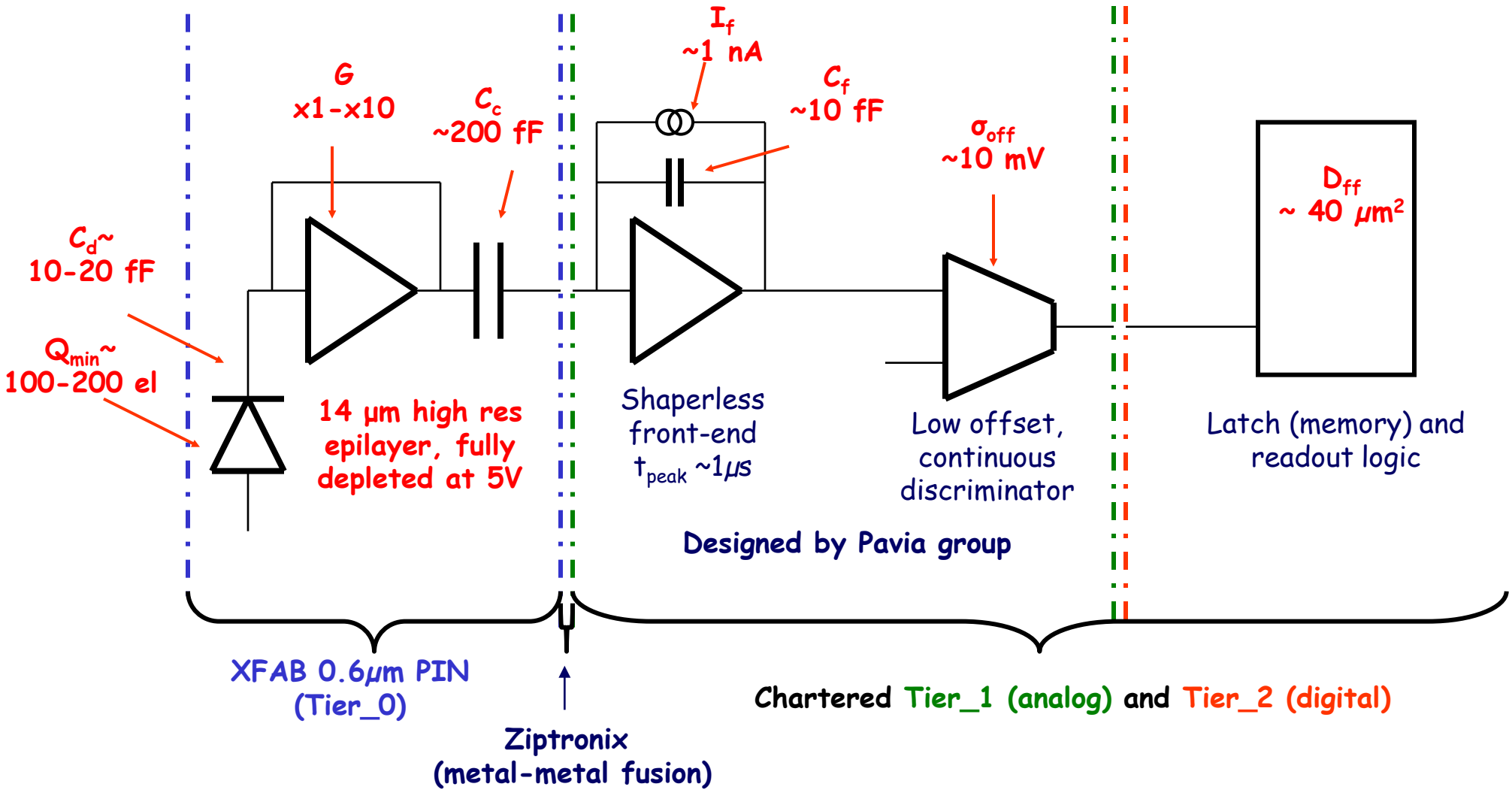


DBI Electrical Connections

- After oxide bond is strong enough, wafers are heated to form thermo compression bond between Magic Metal implants.

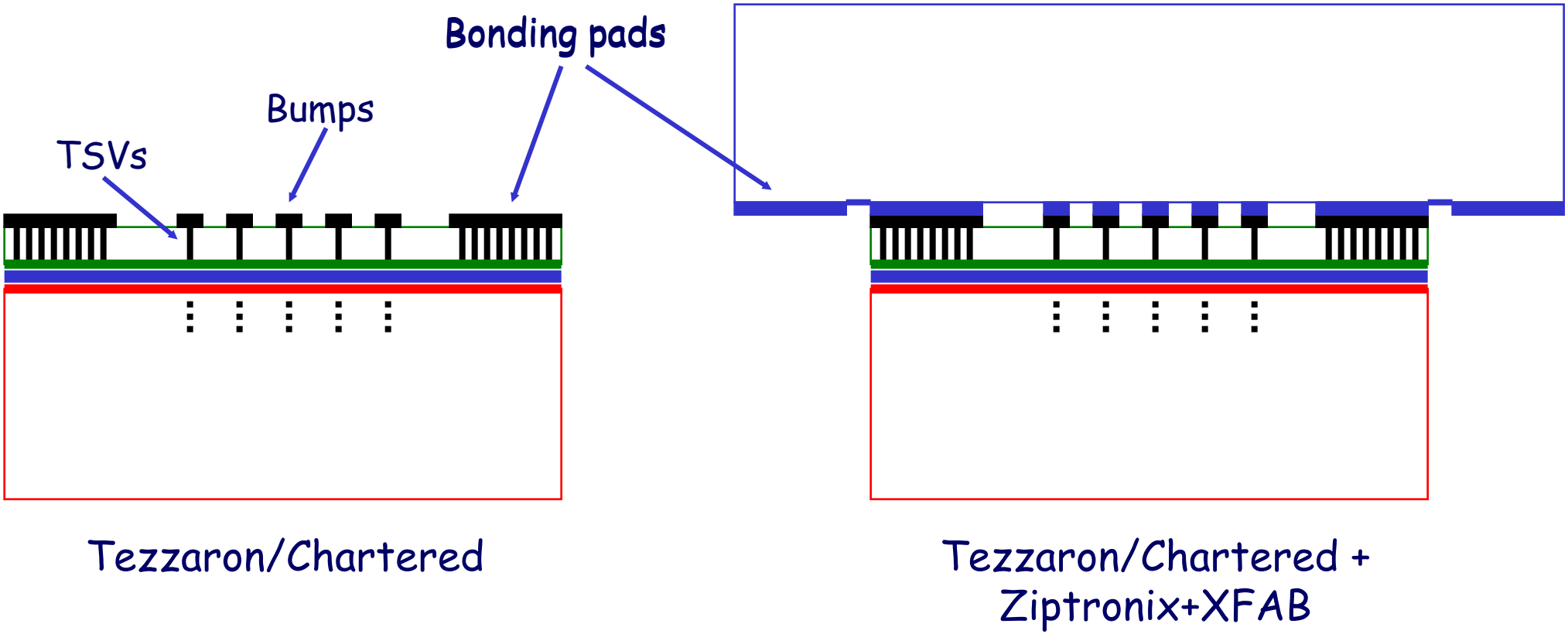


3D FE for the XFAB detector (W. Dulinski and coworkers, IPHC Strasbourg)



Chip to XFAB wafer bonding

- Direct bonding (through Ziptronix DBI technology) between the Tezzaron/Chartered 3D wafer and the XFAB wafer

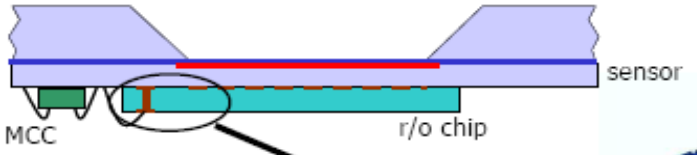


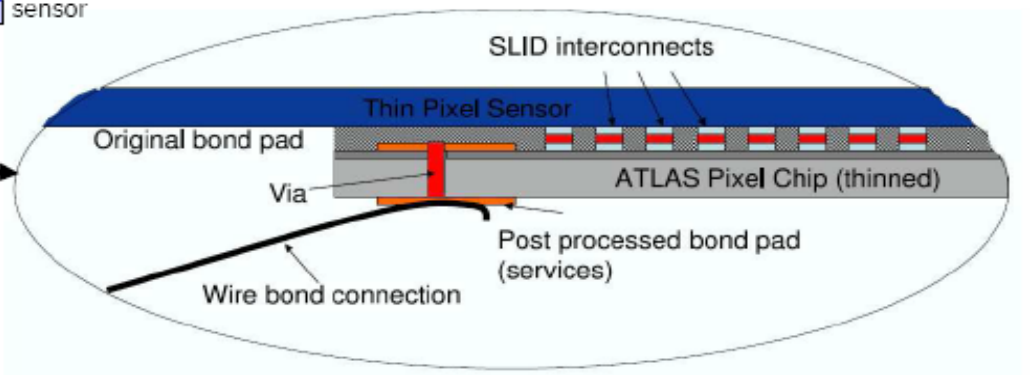
Vertical integration between readout chip and fully depleted sensor: IZM

- Example: ICV-SLID technology developed by Fraunhofer-IZM and MPI-HLL

sLHC: R&D Program 2007 - 2009 → Demonstrator

Existing ATLAS Pixel chip (FE-I3) face-to-face attached to a thin sensor!



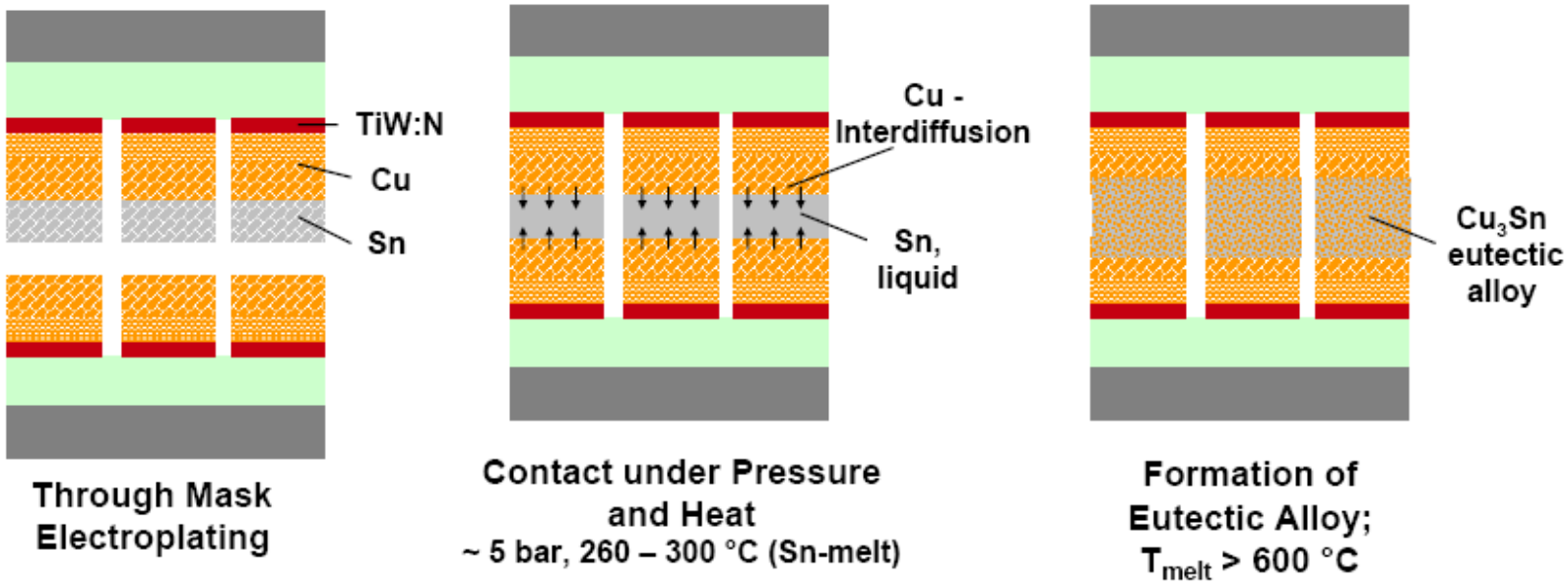


Goals

-: Test thin detectors
-: thinning of r/o chips
-: practice SLID and ICV

Vertical integration between readout chip and fully depleted sensor: IZM

Metallization SLID (Solid Liquid Interdiffusion)



3D: T-Micro

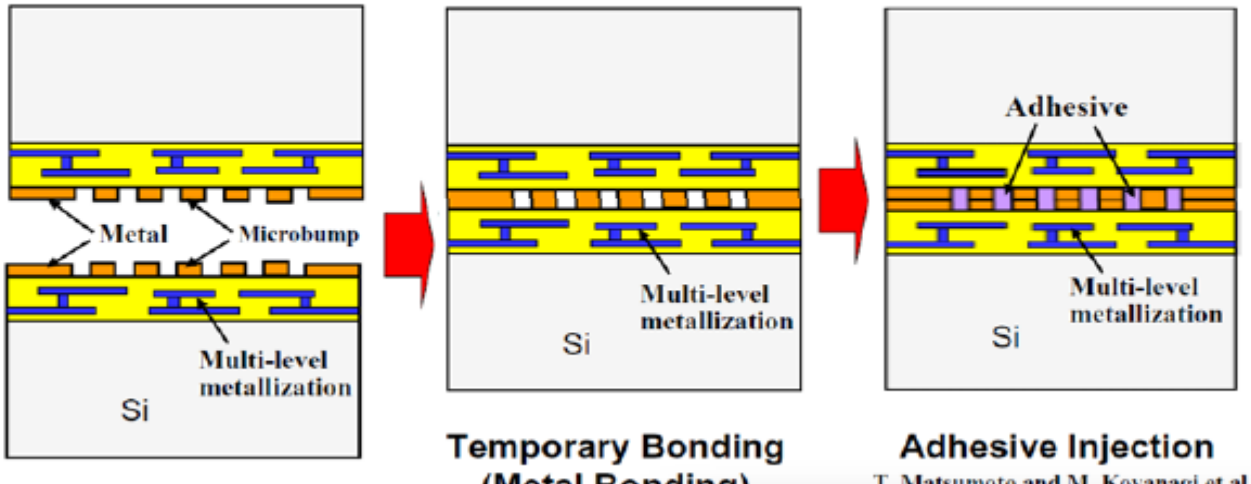
Tohoku-Micro Tec Co.

Foundation: 2010/4/2

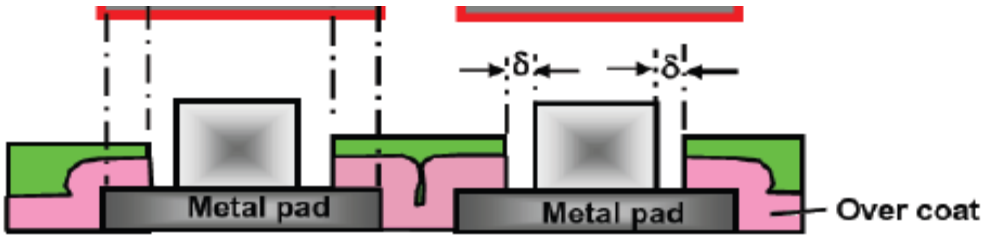
Co-founder : M. Koyanagi (CTO) Tohoku University

M . Motoyoshi (CEO) ex-ZyCube president

Wafer Bonding by μ-Bumps



T. Matsumoto and M. Koyanagi et al, SSDM, pp.460-461, 1997



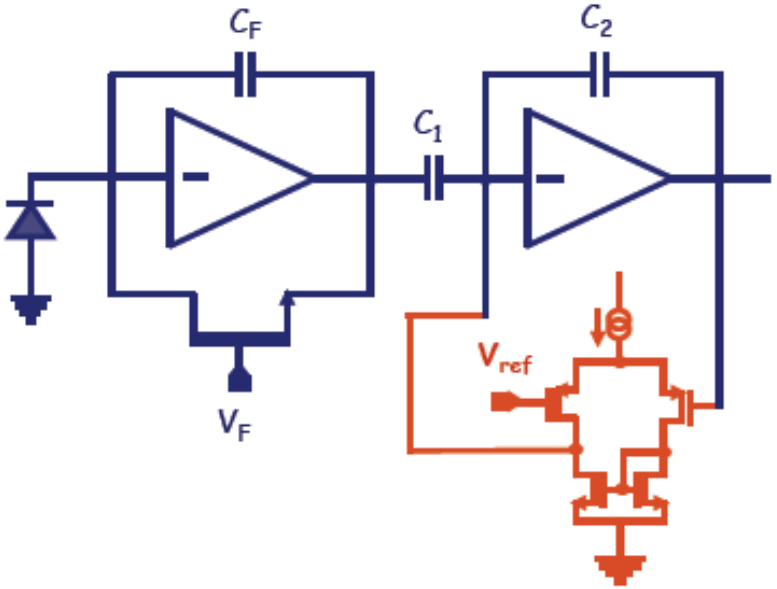
bump pitch	5.0 μm
Metal pad	4.0 x 4.0 μm
Bump opening	3.0 x 3.0 μm
Bump size	2x2 μm (bottom)

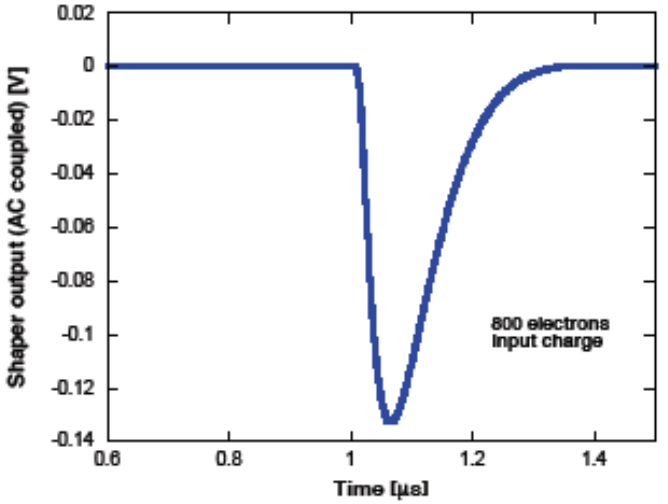
3D Front-end for MAPS…

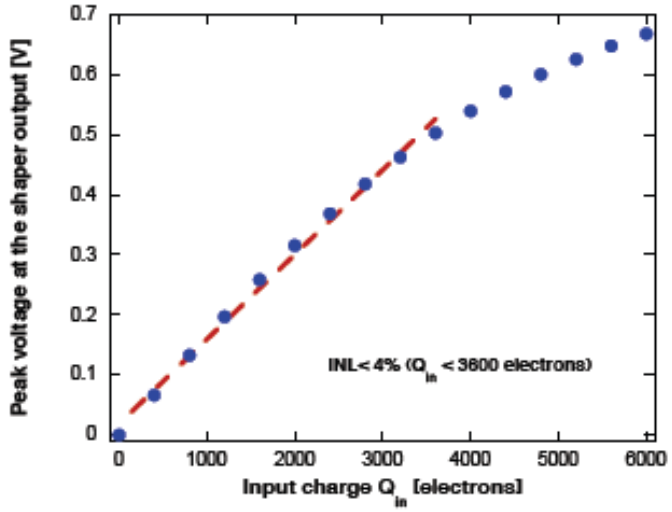
Front-end for 3D MAPS

Main design features and simulation results

- W/L=28/0.25
- I_D=26 μA, power dissipation≈40 μW
- C_D=300 fF
- 70 ns peaking time
- Charge sensitivity (G_Q): 950 mV/fC
- Equivalent noise charge (ENC): 60 electrons





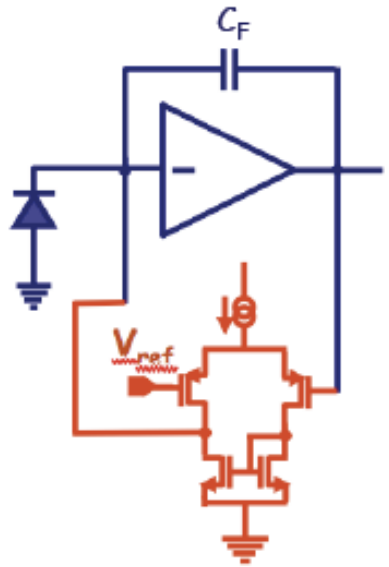


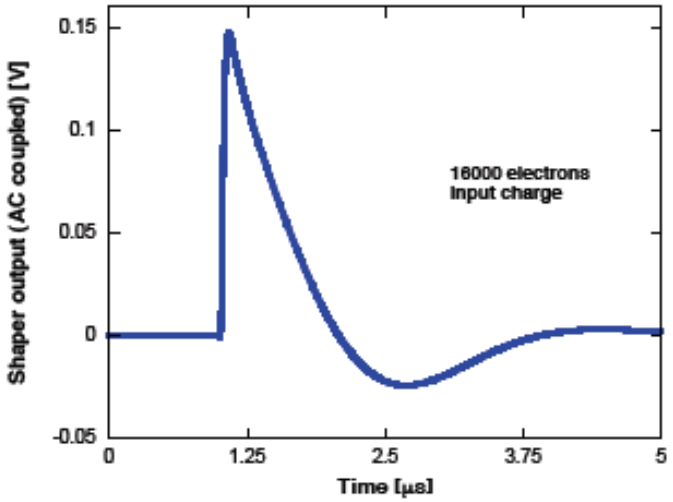
…and for high resistivity pixels

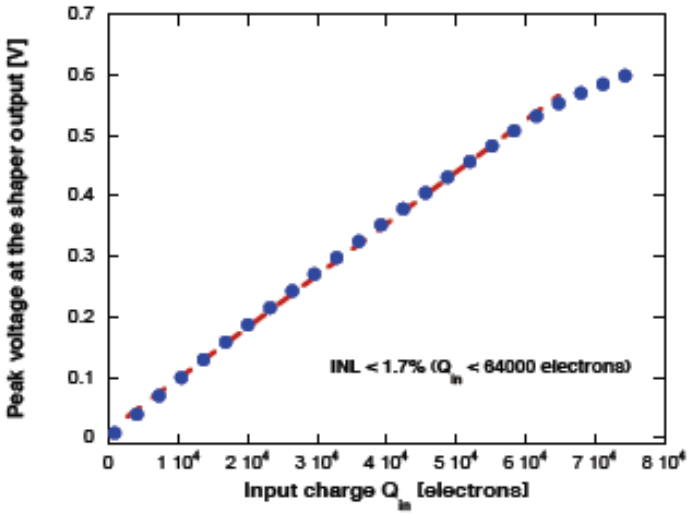
Front-end for hybrid pixels

Main design features and simulation results

- W/L=30/0.35
- I_D=4.4 μA, power dissipation=6.6 μW
- C_D=150 fF
- 80 ns peaking time
- Charge sensitivity (G_Q): 55 mV/fC
- Equivalent noise charge (ENC): 170 electrons







Readout architecture

- Digital information of hit signals is further processed by circuitry associated to each pixel (strip) and at the chip periphery. Position (pixel or strip address), timing (time stamp) and possibly pulse amplitude (from ADC) information must be provided.
- All architectures perform data sparsification, processing only data from channels where the signal exceeds the discriminator threshold
- Often, a trigger system selects only a fraction of the events for readout, reducing the data volume sent to the DAQ. In this case, information for all hits must be buffered for some time, waiting for a trigger signal (delay of a few μs).
- Triggerless (data push architectures) are also available. All hits are read out immediately (as long as the rate is not too high). This allows the tracker information to be used for Level 1 Trigger (BTeV, SLHC)

Time stamp readout in pixel readout chips

- A time stamp counter generates a time reference.

  The time stamp code:

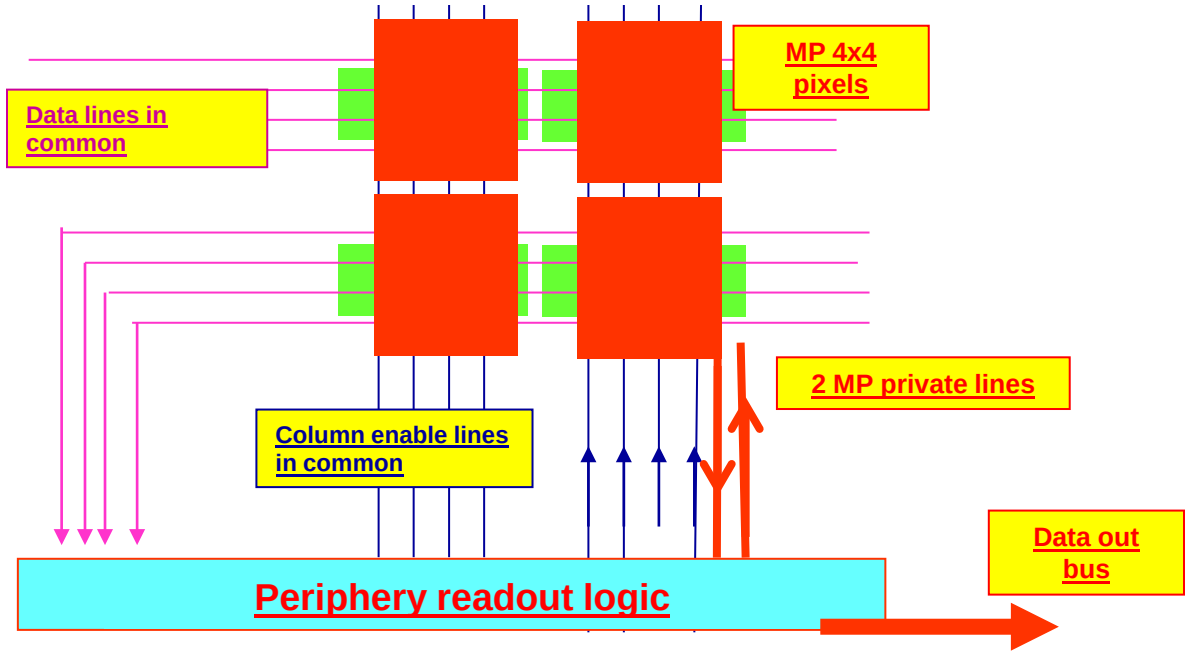
  1) can be distributed to all pixels

  The content of an in-pixel time stamp register is frozen when the pixel detects a hit and is then transmitted to the periphery.

  2) can stay in the chip periphery or in the “end-of-column” control logic block.

  When a pixel is hit, the end-of-column or periphery logic is informed that one or more hits have occurred and stores the relevant time stamp in a register.

A macropixel readout architecture for the sparsified readout of MAPS in standard CMOS technology



Exploiting 3D integration: readout architecture without MacroPixel

- The MacroPixel arrangement was adopted to reduce the pixel-level logic (limiting the area of competitive N-wells) and the digital switching lines running above pixel columns

- Reasons to eliminate the MacroPixel architecture:
  - **The routing of private lines (FastOR, Latch Enable) scales with matrix column dimension**
  - **Inefficiency due to dead time (freezed MP) depends on MP dimensions**
  - **Not-fired MP columns of fired MPs are also scanned (time consuming) by the sparsification logic**
  - **Only MP masking level can be reasonably implemented**

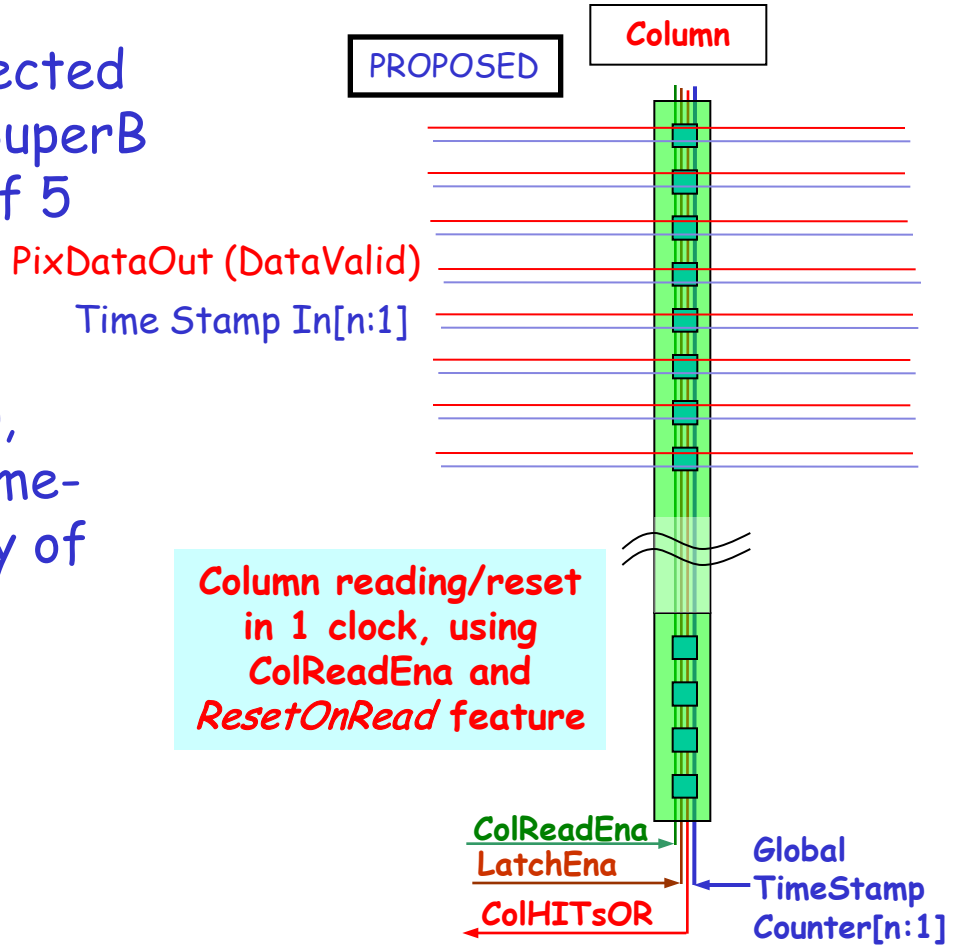
- Matrix readout speed can increase, also carrying along a readout logic simplification

- Removing the MacroPixel and implementing timestamp latching at the pixel level appears possible with 3D integration, without reducing the pixel efficiency

Exploiting 3D integration: readout architecture

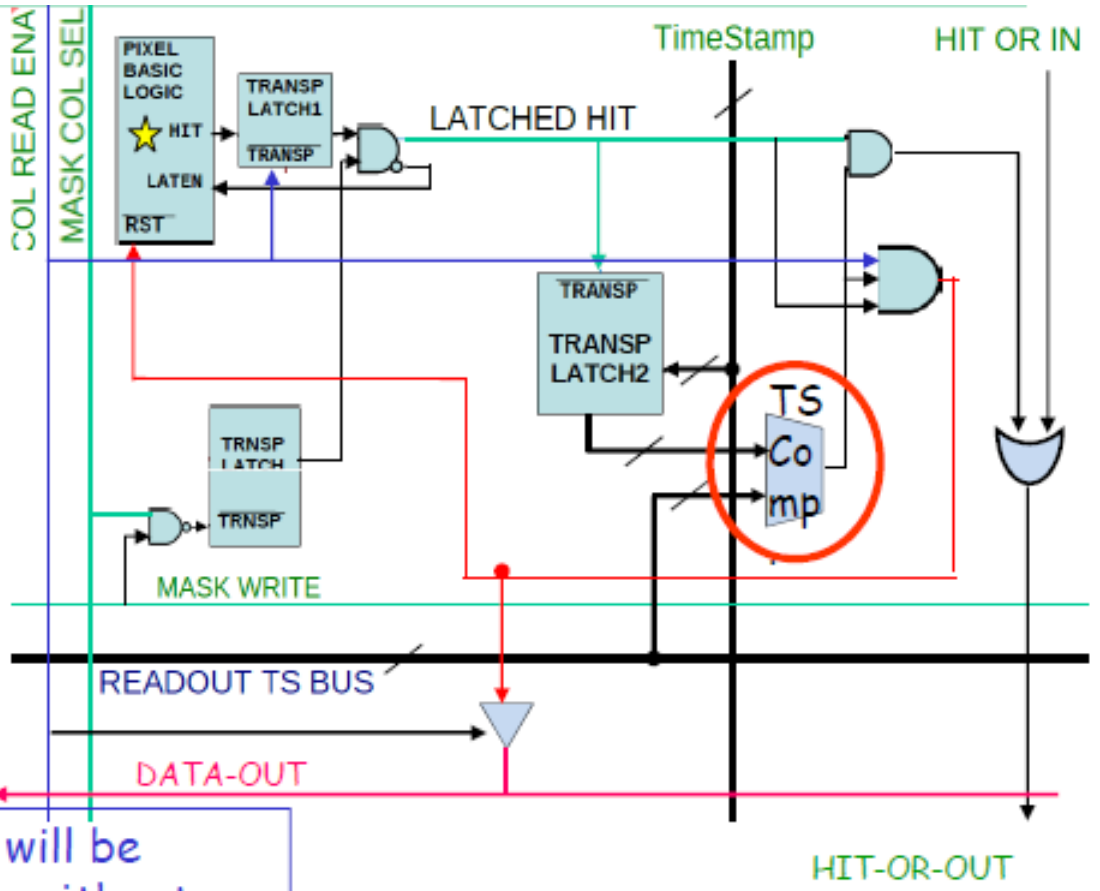
Main goals:

- handle a hit rate of 100 MHz/cm^2 (expected background rate in the Layer0 of the SuperB Silicon Vertex Tracker, with a factor of 5 safety factor)
- In a large MAPS matrix (e.g., 320x216), perform data-driven hit readout in a time-ordered fashion, with a time granularity of 100 ns



Exploiting 3D integration: pixel-level logic with time-stamp latch and comparator for a time-ordered readout

- No Macropixel
- Timestamp (TS) is broadcast to pixels & pixel latches the current TS when is fired.
- Matrix readout is timestamp ordered
  - A readout TS enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that TS.
  - A column is read only if HIT-OR-OUT=1
  - DATA-OUT (1 bit) is generated for pixels in the active column with hits associated to that TS



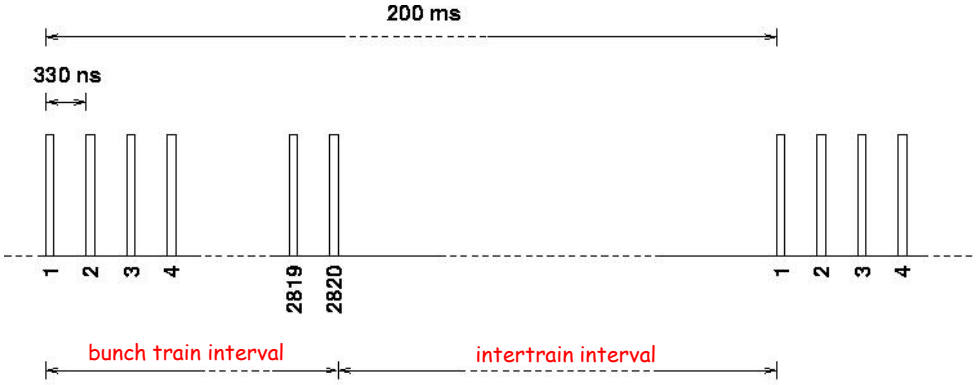
- This more complex in pixel logic will be implemented with 3D integration without reducing the pixel collection efficiency ever improving the readout performance (*readout could be data push or triggered*)

VHDL simulation of the data push chip (100MHz/cm^2 input hit rate)

- Readout Effi > 99 % @ 50 MHz clock with timestamp of 200 ns.

Another readout architecture: a 3D vertically integrated pixel sensor for the ILC vertex detector

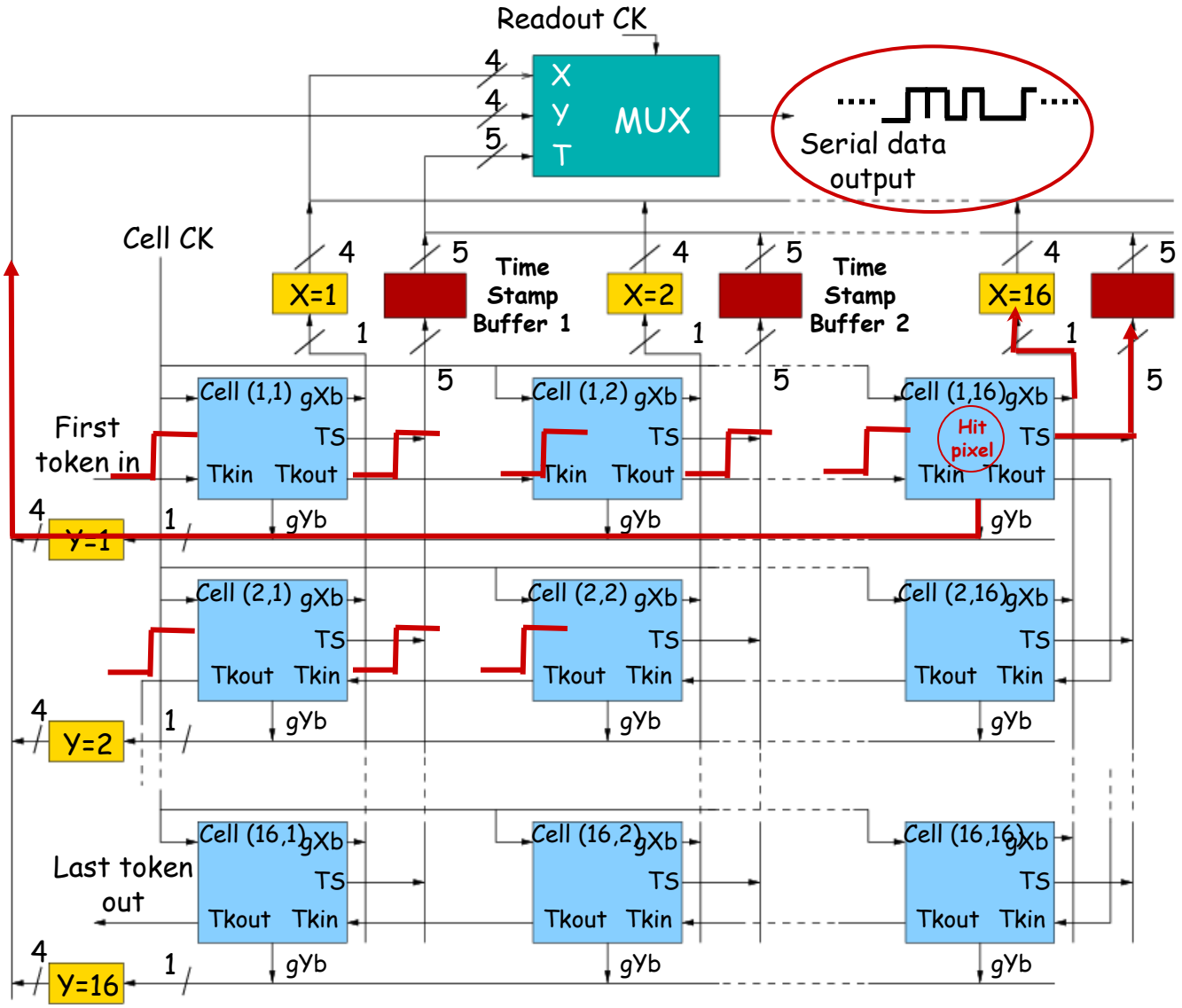
- The beam structure of ILC will feature 2820 crossings in a 1 ms bunch train, with a duty-cycle of 0.5%



  - assuming maximum hit occupancy 0.03 part./Xing/mm^2
  - if 3 pixels fire for every particle hitting → hit rate ≈ 250 hits/train/mm^2
  - if a digital readout is adopted 5μm resolution requires 17.3 μm pixel pitch
  - 15 μm pitch → $O_c \approx 0.056$ hits/train → 0.0016 probability of a pixel being hit at least twice in a bunch train period

- A pipeline with a depth of one in each cell should be sufficient to record > 99% of events without ambiguity
- Data can be readout in the intertrain interval → system EMI insensitive

ILC VTX pixel readout architecture: intertrain readout



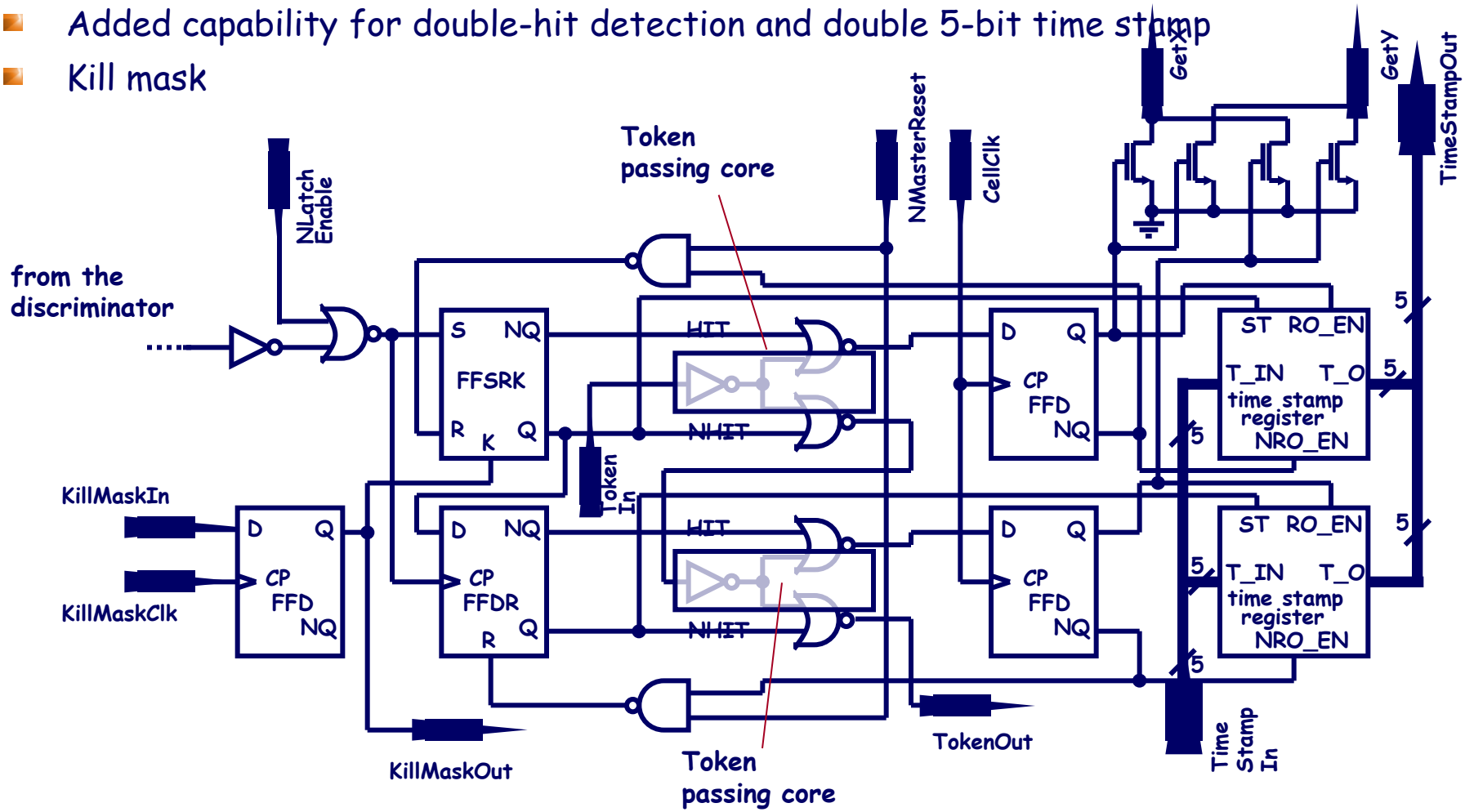
Readout phase:

- token is sent
- token scans the matrix and
- gets caught by the first hit pixel
- the pixel points to the X and Y registers at the periphery and
- sends off the time stamp register content
- data are serialized and token scans ahead

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

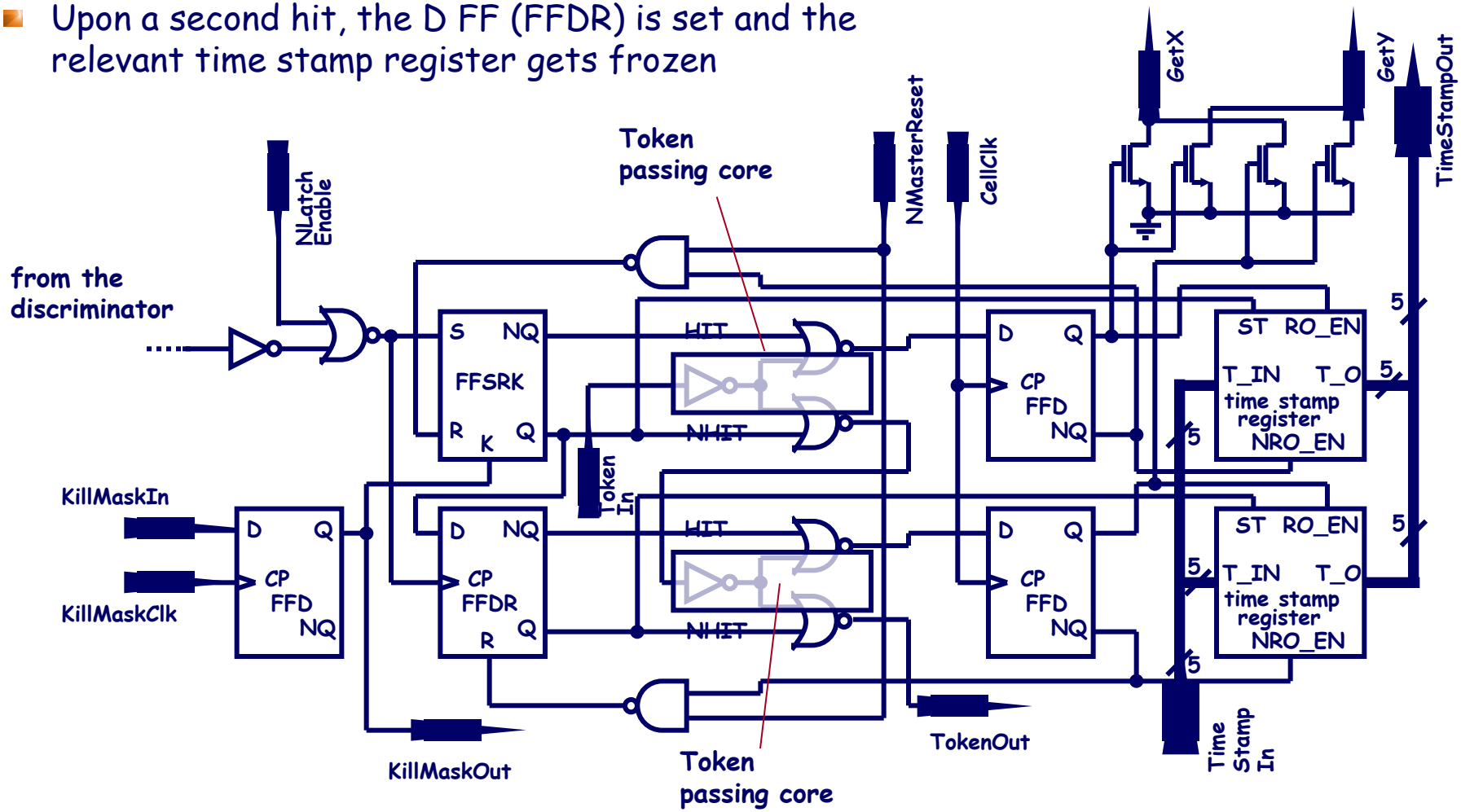
Advantages of 3D for the ILC architecture

- Increase digital functional density (still getting a smaller point resolution)
  - Pixel pitch reduced from 25 μm to 20 μm
  - Added capability for double-hit detection and double 5-bit time stamp
  - Kill mask

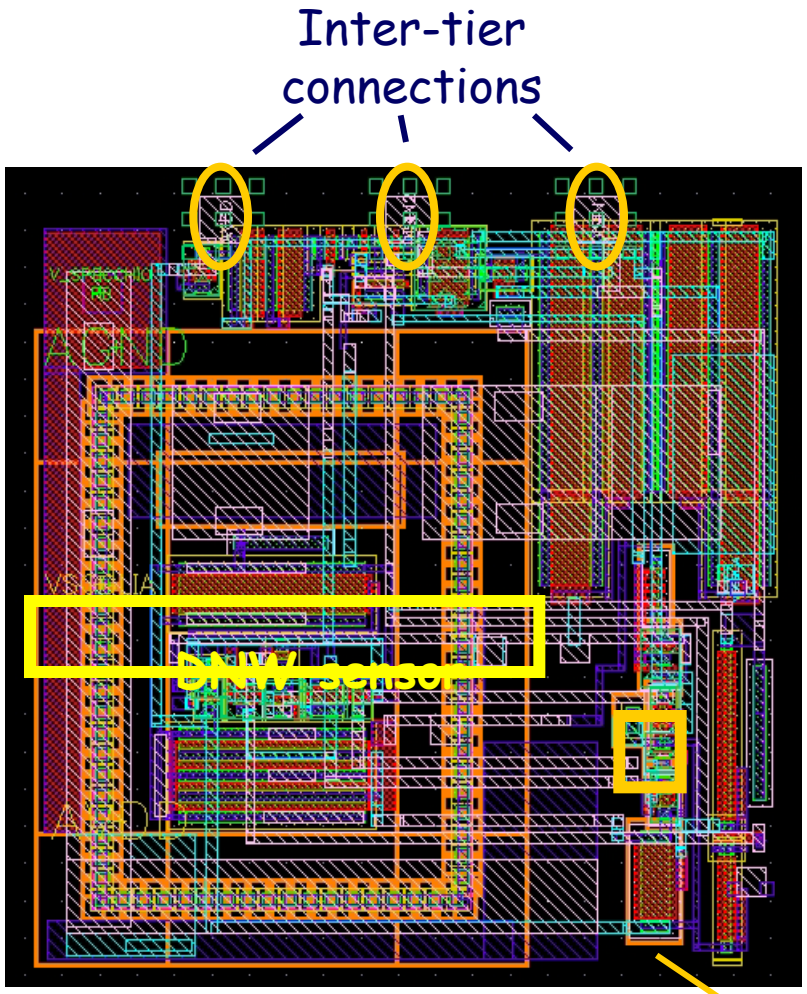


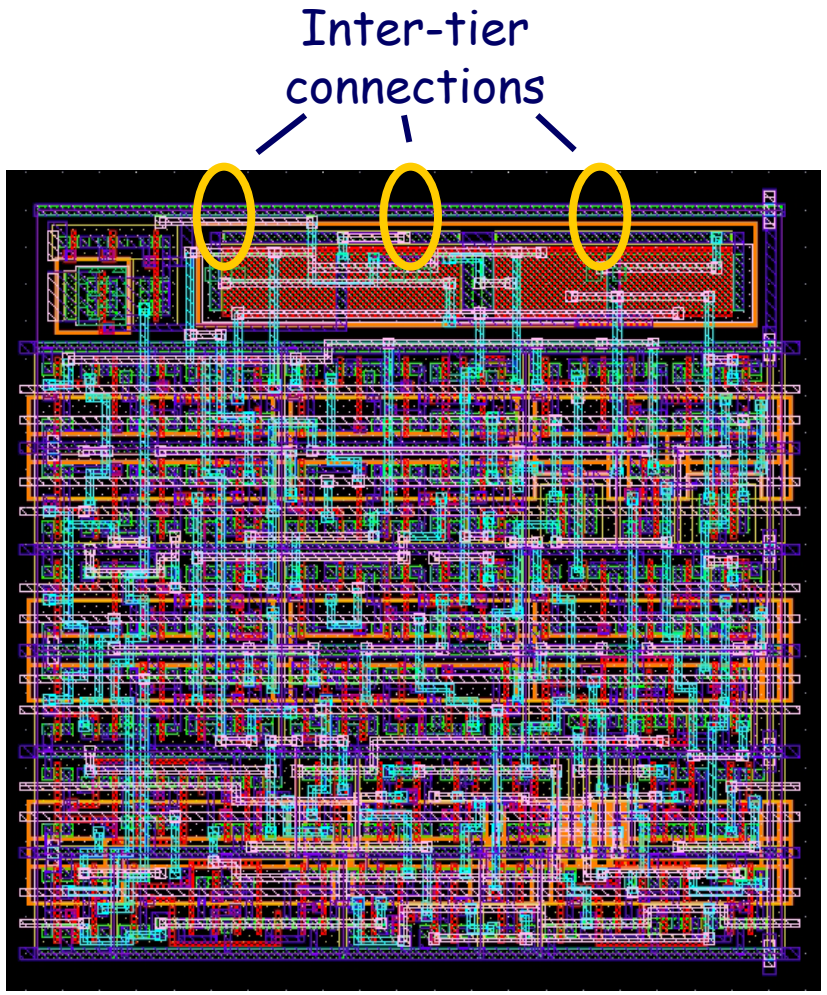
Advantages of 3D for the ILC architecture

- During the bunch train period, the SR FF (FFSRK) is set, and the relevant time stamp register gets frozen, when the pixel is hit for the first time
- Upon a second hit, the D FF (FFDR) is set and the relevant time stamp register gets frozen



The 20 μm x 20 μm 3D cell for ILC MAPS





Pixel sensors for X-ray imaging

HEP:

one hit pattern (image) is one event; information is not uniformly distributed in all hit patterns

"conventional" X-ray imaging:

one image is made of many events, which have to be accumulated (integration or counting) to obtain an image with the required quality

position and energy resolution are required (very large dynamic range)

X-ray imaging at advanced X-ray Sources:

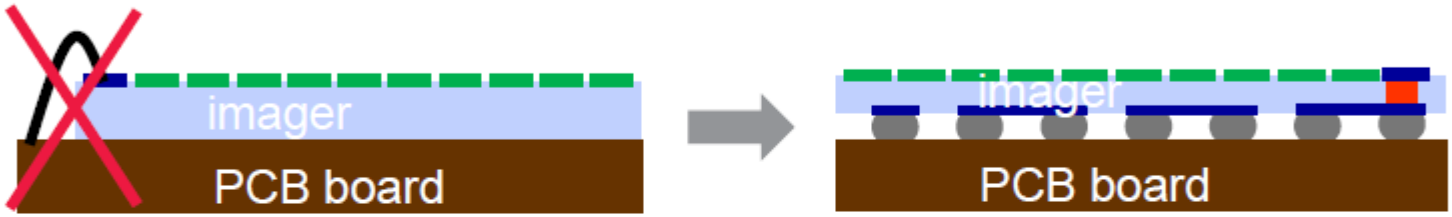
also "single shot" imaging!

What they need … from SL-sources to XFELs

- count rates per pixel > MHz
- high frame rates (100 Hz – 10 kHZ → 5 MHz)
- huge dynamic range (1 photon to 10^6 photons)
- pixel size < 50 μm
- seamless detectors
- "no" dead time

PERIPHERAL 3D INTEGRATED IMAGERS

- Advanced packaging technology at bond pad level:
  - From traditional lateral wire bonding to TSV per bond pad + bump ball bonding
  - = 3D integration at package level using Through Si Vias (TSVs)

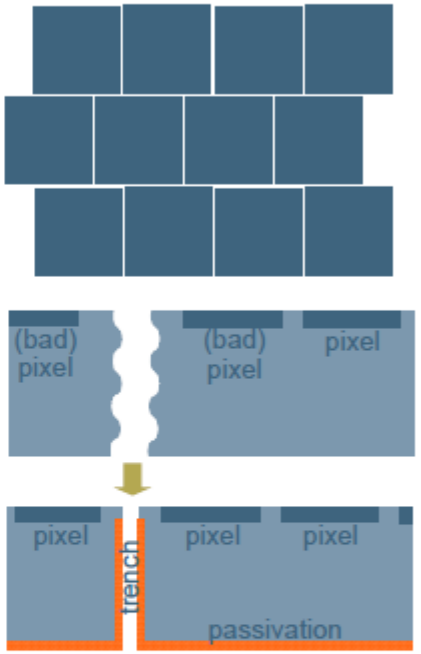


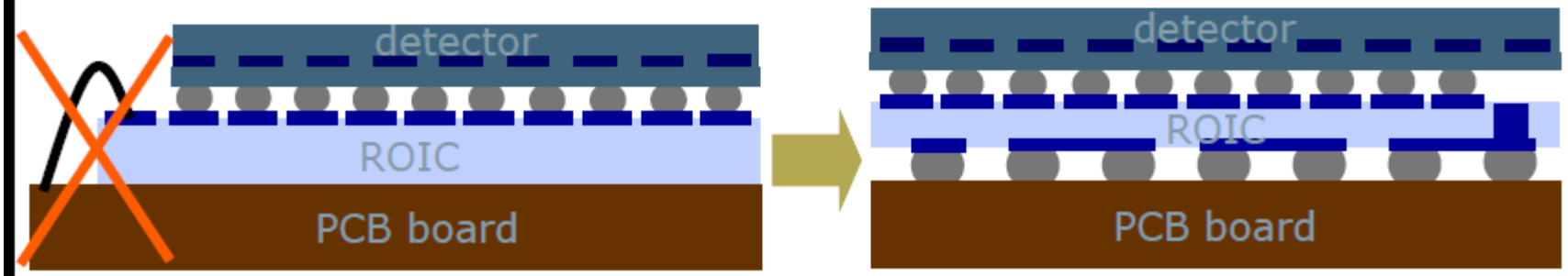
- Advantages:
  - Smaller footprint
  - Reduced capacitance → faster/low power interconnect
  - Buttability with mimimal area loss
- Applications:
  - Consumer imagers
  - Large area tiled imagers with minimal dead area
  - Endoscopes

imec © IMEC 2010 PIET DE MOOR 35

Peripheral 3D integrated imagers:
Tiled edgeless imagers for large area detection

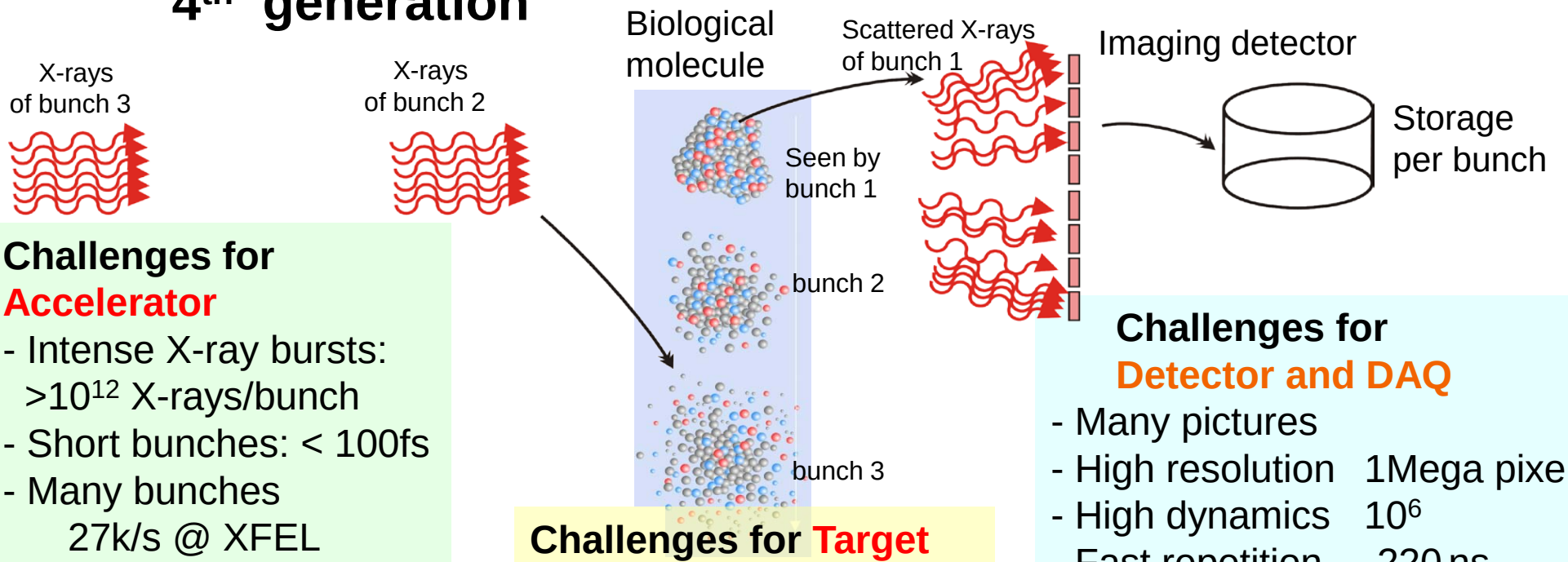
- Problem of large area imagers:
  - Stitching of large area imagers -> yield becomes critical
  - 4-side butting/tiling: dead area between modules
- Concept of edgeless imagers:
  1) 3D integration for vertical interconnections
  2) advanced singulation close to active pixels:
     - Dicing by grinding
     - Side wall passivation





Dream of users : Challenges for the designers

4th generation



Challenges for Accelerator
- Intense X-ray bursts: >10^{12} X-rays/bunch
- Short bunches: < 100fs
- Many bunches
  27k/s @ XFEL

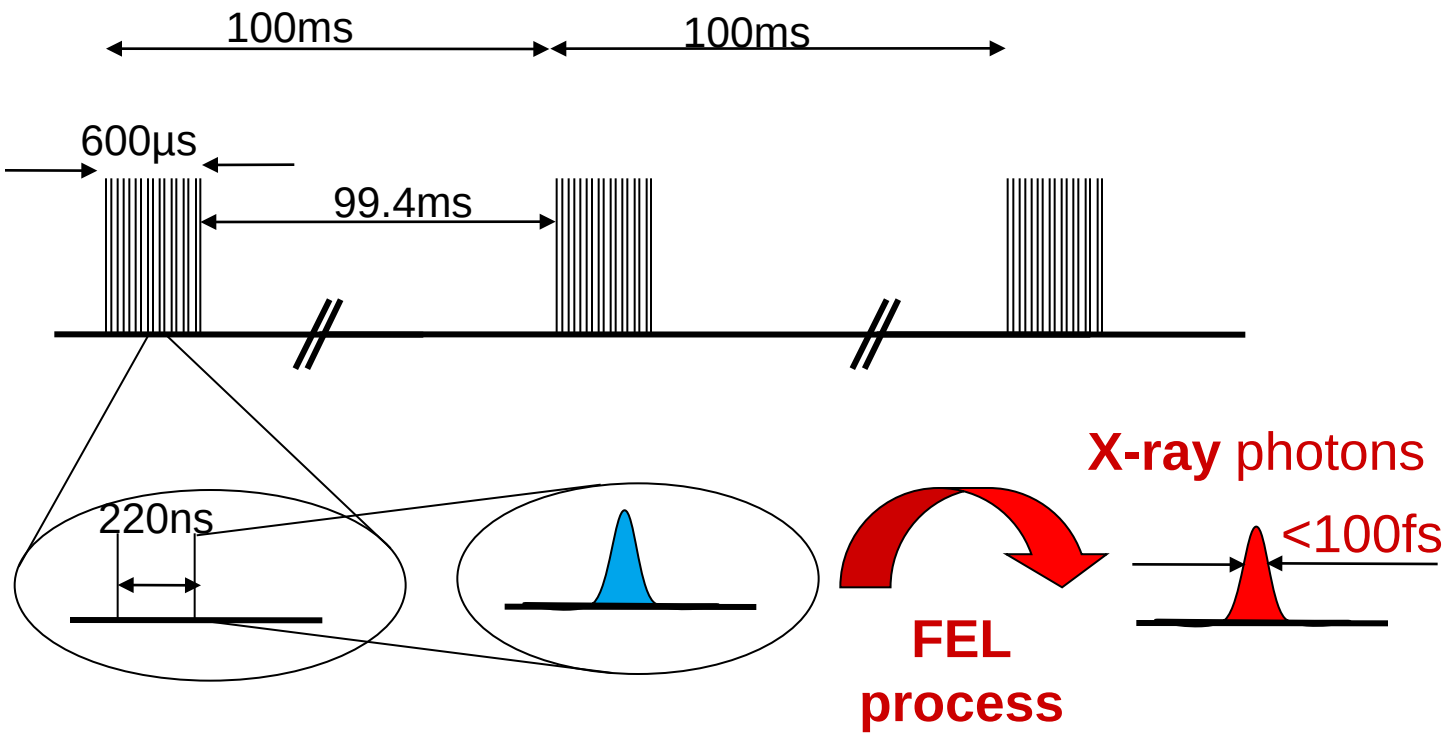
Challenges for Target
- Fast cleaning
- Fast exchange

Challenges for Detector and DAQ
- Many pictures
- High resolution 1Mega pixel
- High dynamics 10^6
- Fast repetition 220 ns
- High data rates ~80 Gbit/s

> All that effort will open new opportunities for science

- Structure and dynamics in complex systems: Molecules, clusters, biological objects, plasma
- Physics, chemistry, material science, biology, medicine

Train structure



> Advantage: 27 000 bunches/sec,
LCLS,SCSS: 60-120 bunches/sec

> Consequence: All systems have to handle 220ns bunch to bunch
4.5MHz operation for 27k-bunches/sec.

DSSC (DEPFET Sensor with Signal Compression) Consortium

[1]Max Planck Institut fuer Extraterrestrische Physik, Garching, Germany
[2]MPI Halbleiterlabor, Muenchen, Germany
[3]Max Planck Institut fuer Physik, Muenchen, Germany
[4]Dipartimento di Elettronica e Informazione, Politecnico di Milano, Milano, Italy
[5]Sezione di Milano, Italian National Institute of Nuclear Physics (INFN), Milano, Italy
[6]Zentrales Institut für Technische Informatik, Universitaet Heidelberg, Heidelberg, Germany
[7]Deutsches Elektronen-Synchrotron DESY, Hamburg, Germany
[8]PNSensor GmbH, Muenchen, Germany
[9]Fachbereich Physik, Universitaet Siegen, Siegen, Germany
[10]Dipartimento di ingegneria industriale, Università di Bergamo, Bergamo, Italy

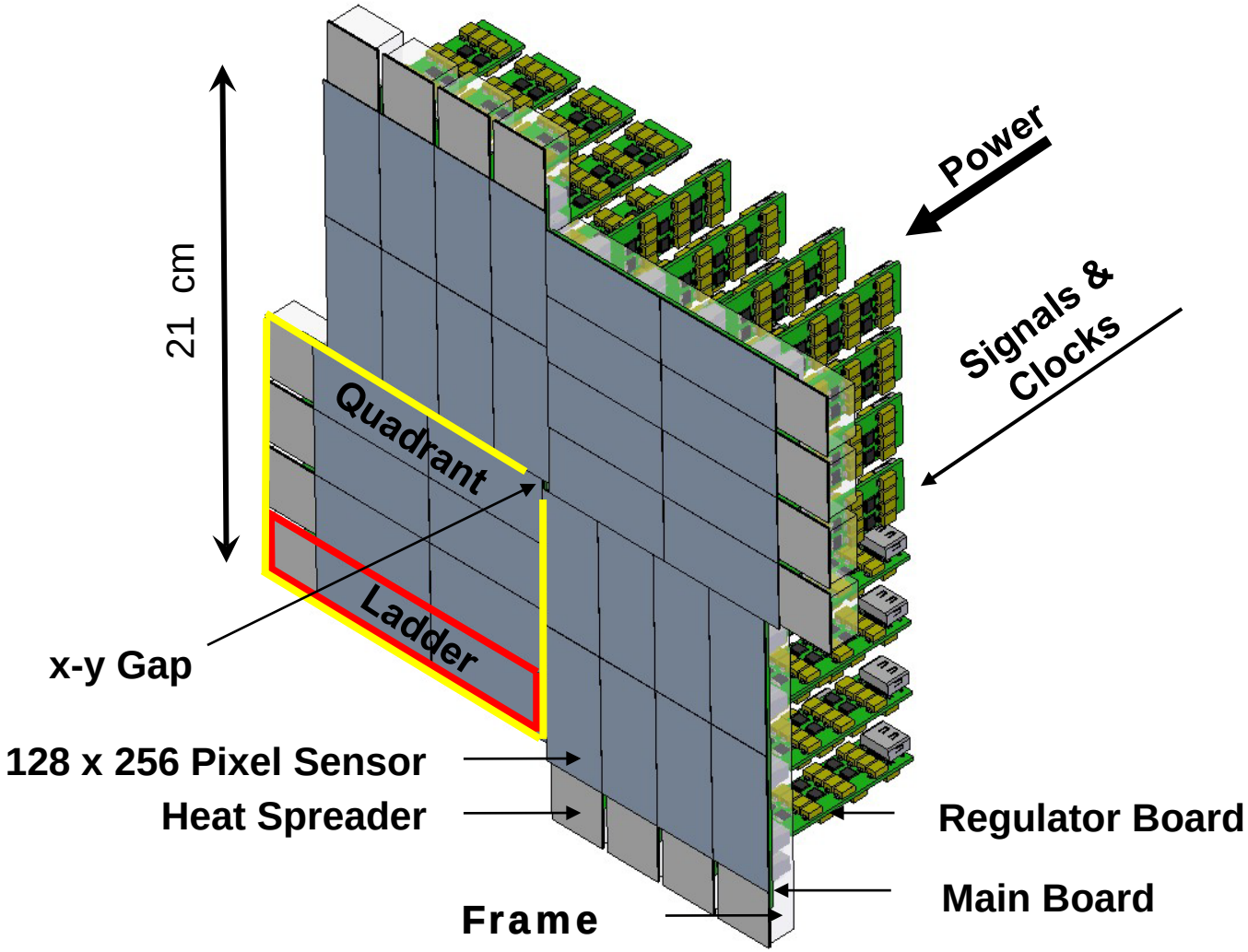


PNSensor

Universität
Gesamthochschule
Siegen

DSSC Detector

scheduled for the middle of 2015



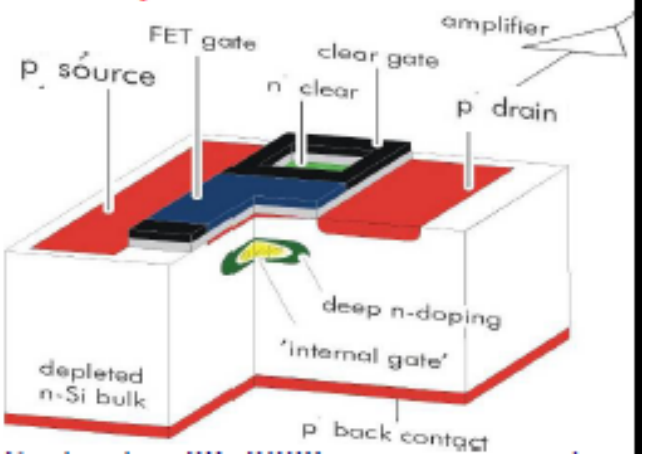
- 1024x 1024 pixels
- 16 ladders/hybrid boards
- 32 monolithic sensors 128x256 6.3x3 cm^2
- DEPFET Sensor bump bonded to 8 Readout ASICs (64x64 pixels)
- 2 DEPFET sensors wire bonded to a hybrid board connected to regulator modules
- Heat spreader
- Dead area: ~15%

Performance requirements for an XFEL detector

Parameter	Expected DSSC performance
Energy range	0.5 … 25 keV (optimized for 0.5 … 4 keV)
Number of pixels	1024 x 1024
Sensor Pixel Shape	Hexagonal
Sensor Pixel pitch	~ 204 x 236 μm^2
Dynamic range / pixel / pulse	> 6000 photons @1 keV
Resolution (S/N >5:1)	Single photon @ 1 keV (5 MHz) Single photon @ 0.5 keV (≤ 2.5 MHz)
Electronics noise	< 50 electrons r.m.s.
Frame rate	1-5 MHz
Stored frames per Macro bunch	≥ 512
Operating temperature	-30˚C optimum, RT possible

DEPFET (DEPleted Field Effect Transistor)[2]

- electrons generated in a high-resistivity, fully-depleted silicon bulk steer the current in an amplifying transistor integrated in the pixel cell
- charge collection by drift improves speed, radiation hardness and signal-to-noise ratio
- limited pixel-level electronic functionalities



Requirements for the readout chip:

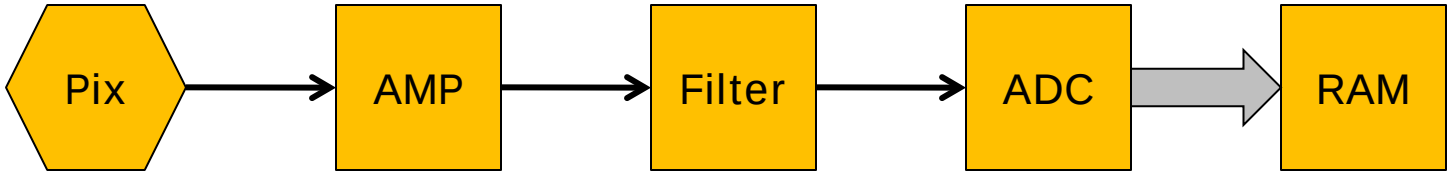
> 5 MHz ↔ 150Gbps (4096 pix, 8Bit) → **local storage**

> Store many words → **digital** storage → **ADC** required

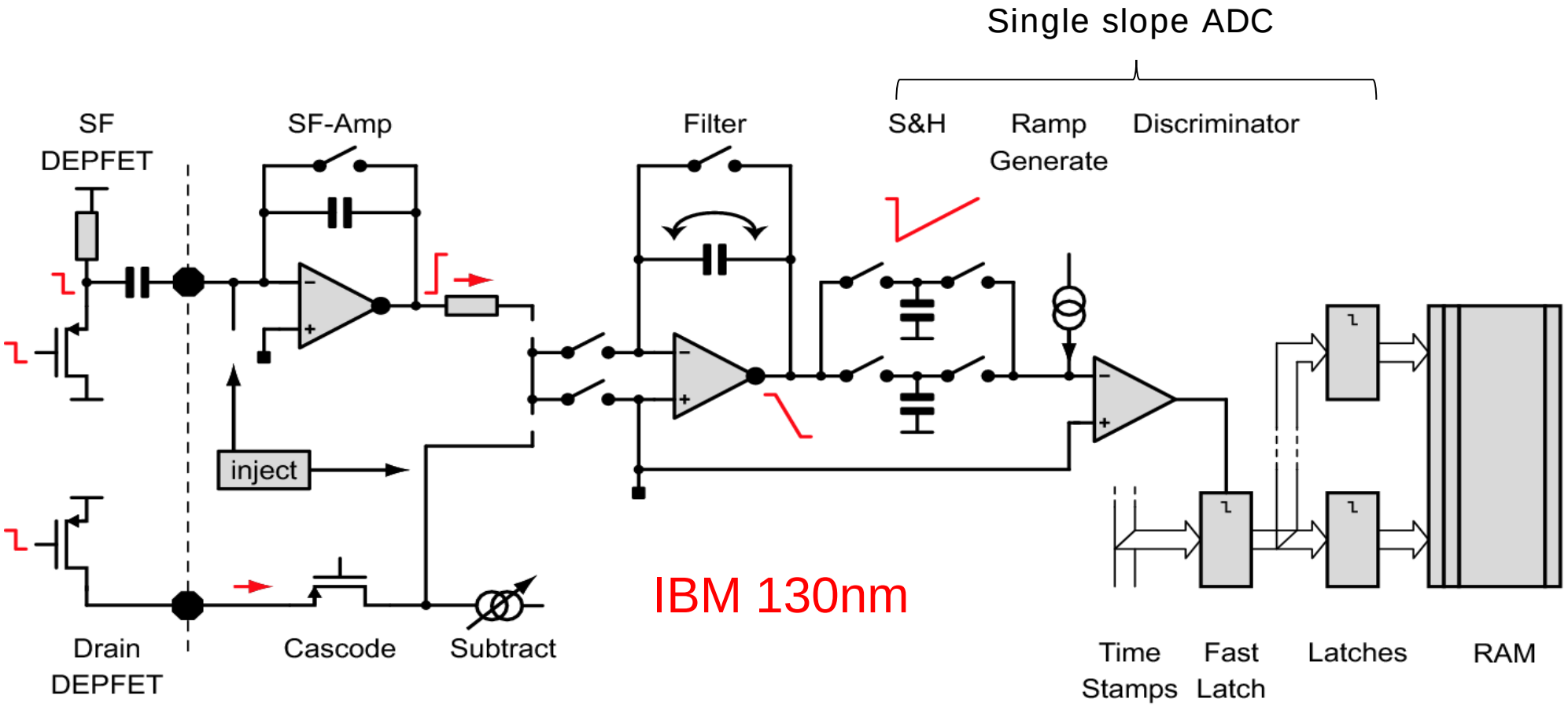
> Read during 100 ms gap → 200 Mbps per chip J

> Bunch of 0.6 ms, 100 ms gap → Power cycling

> Low Energy X-rays, 450µm sensor → no TID problem on chip



Pixel-level electronics in the DSSC readout chip



> Potential benefits from 3D vertical integration

- Reduction of pixel size (presently limited by bump bonding technology)
- Larger RAM capacity (store more images)
- .....

Extending 3D pixel technology from HEP to photon science

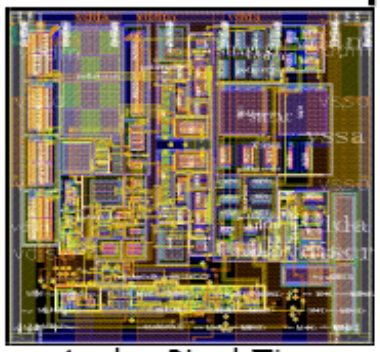
VIPIC-3D (FNAL): demo chip for X-ray imaging (X-ray Photon Correlation Spectroscopy)

64x64 array of 80 μm pixels with high frame rate binary sparsified readout, adaptable to a 4-side buttable X-ray detector array

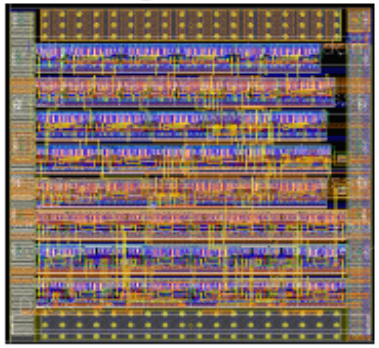
Front End Electronics using 3D Integrated Circuits, FEE2009, Montauk, NY 18-21 May 2009

Fermilab

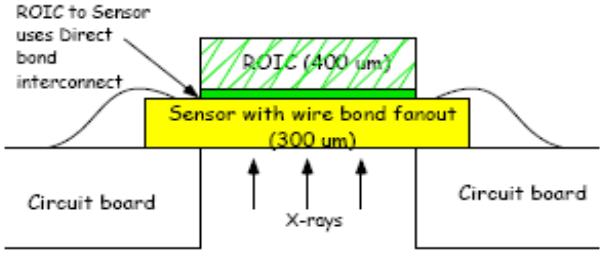
VIPIC-3D Demo-chip for X-ray imaging



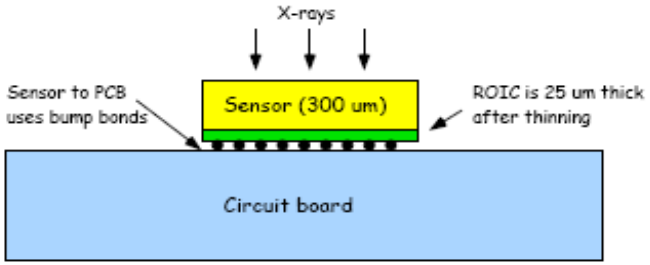
Analog Pixel Tier



Digital Pixel Tier



Option 1 - Less Aggressive Mounting

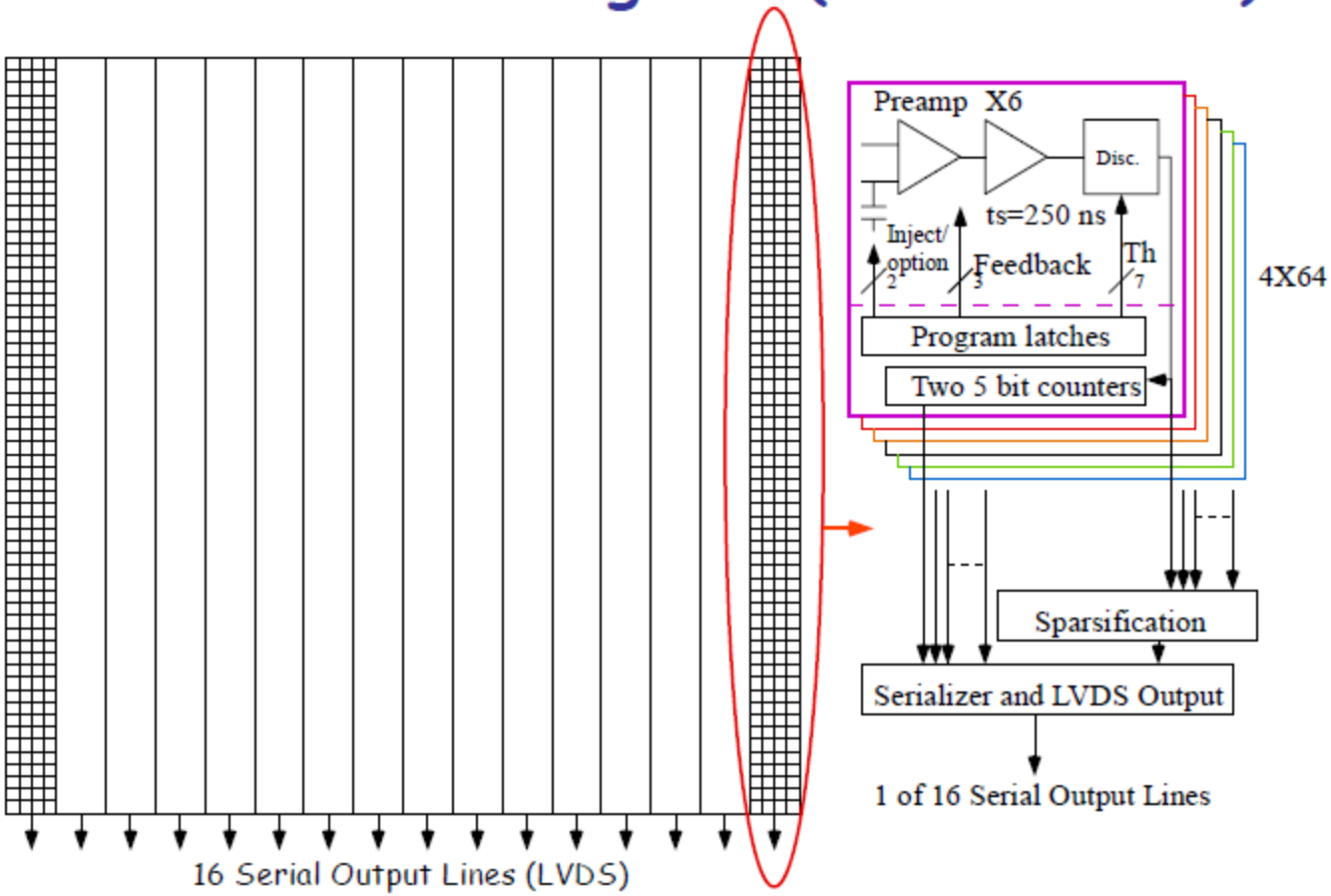


Option 2 - More Aggressive Mounting for four side buttable sensor arrays

VIPIC designed together with AGH UST: P. Grybos, R.Szczygiel

25

VIPIC Block Diagram (4096 Pixels)



Fermilab

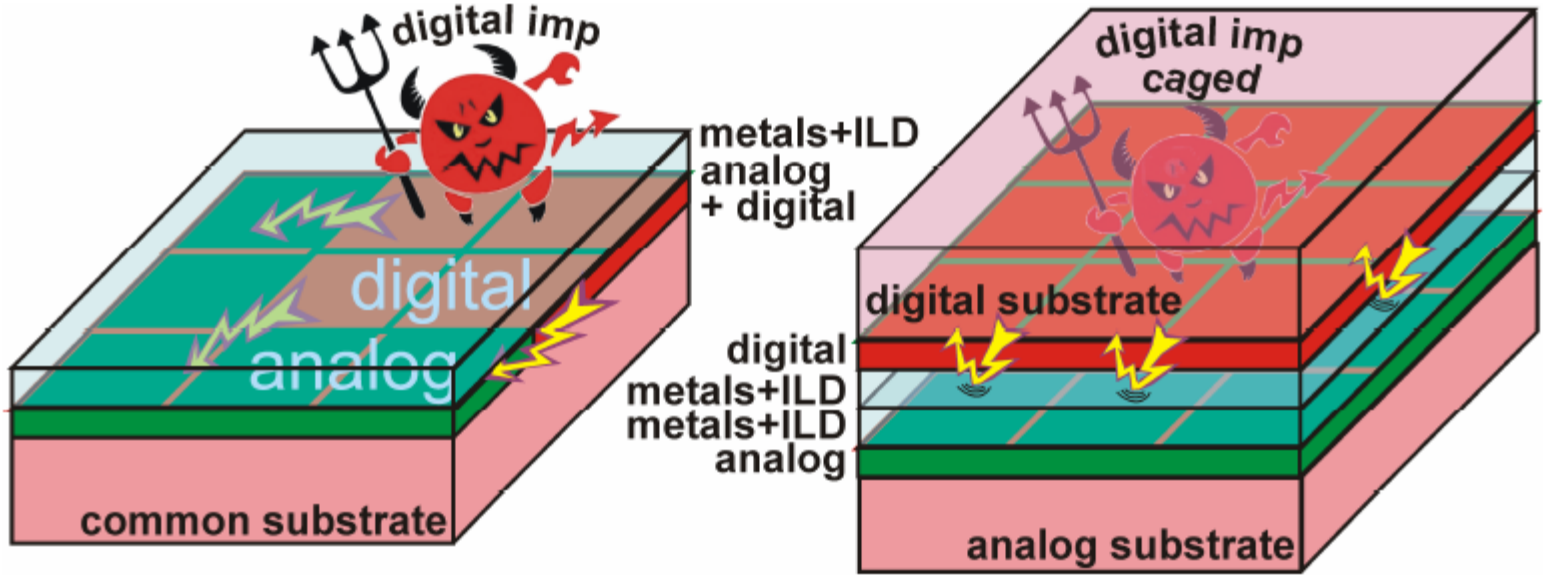
3D-IC opportunities
improvement in noise immunity by separation of digital and analog

– **2D realizations of pixel ROICs suffer noise induced by activity in digital circuitry sharing the same substrate with analog parts**

- Techniques of isolation of power supplies, use of p+/nwell/p+ guardrings separating digital from analog, attempt to reduce substrate currents, elimination of substrate return paths, etc. to reduce interferences

– **3D realization of pixel ROICs allow complete separation of digital activity from low-noise analog parts**

- Substrates are not shared
- Power supplies and grounds can be separated (tied together only where required and harmless)
- Shielding can be implemented on metals on facing sides

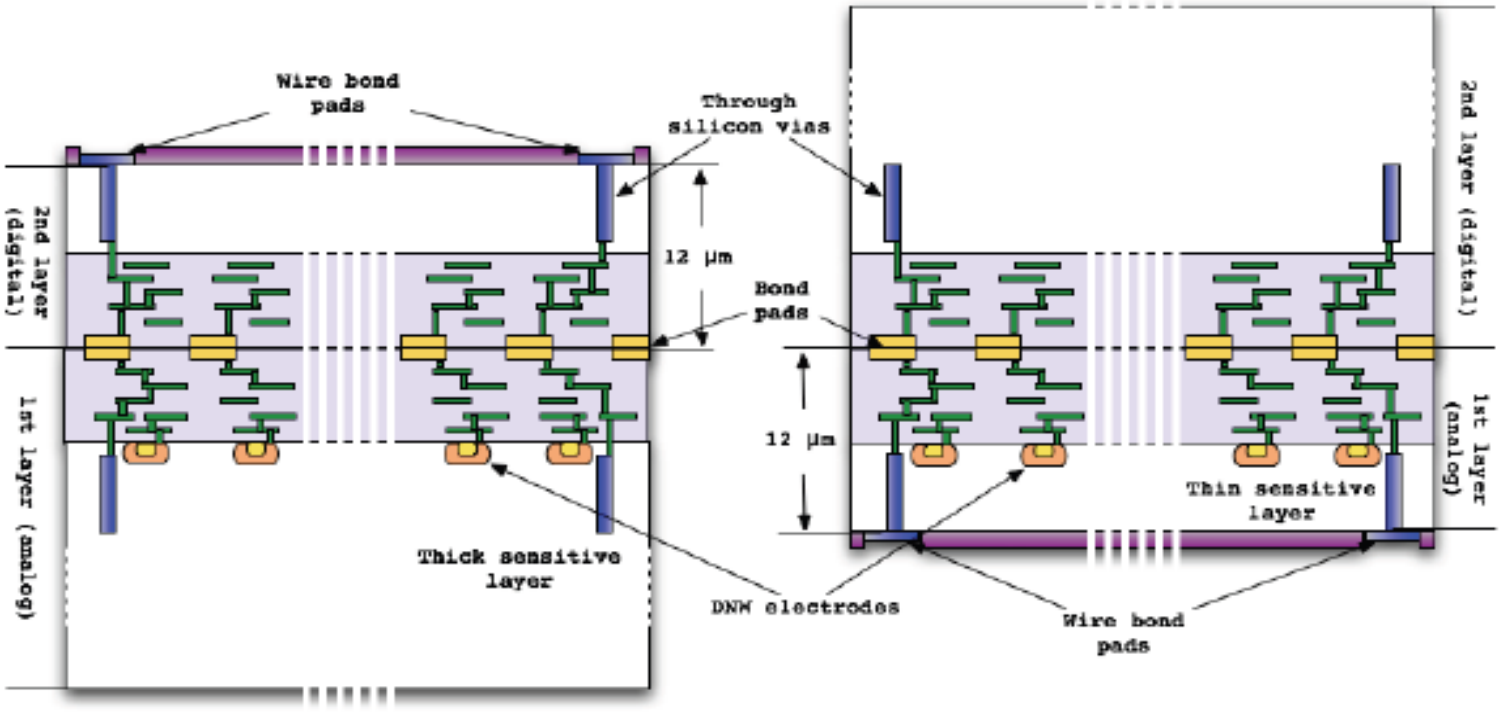


Another extension of 3D pixel technology from HEP to photon science and medical applications

NEW ideas from VIPIX (PV,MI):

In the 2-tier, face-to-face structure of Tezzaron /Chartered devices, 2 chips for each subreticule are obtained, one with a thick substrate under the DNW sensor, the other one with a sensitive volume about 6 μm thick

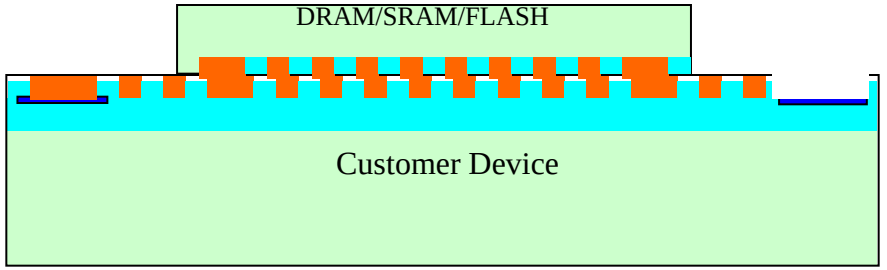
The chip with thin sensitive volume is compatible with applications involving the detection of low/medium energy radiation, for instance from such radioactive sources as **^{3}H ⇒ tritium autoradiography**



New concepts enabled by 3D integration of readout chips

- In a multilayer integrated circuits, a memory could be stacked to store data in small pixels until level 1 trigger is received (multiple hit buffering)

The “killer application” (by Tezzaron)



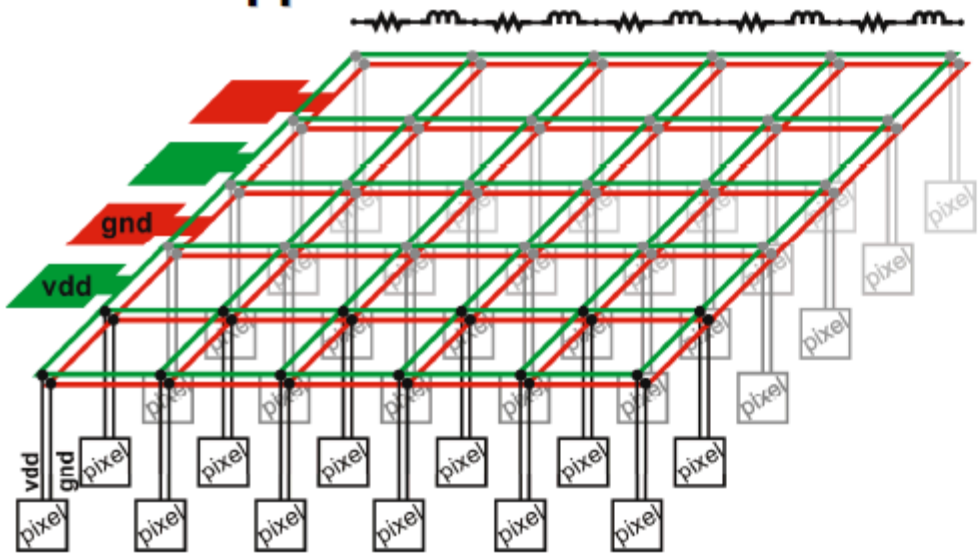
- Better clock distribution, less power needed to move data
- Architecture for on-chip event processing might be devised
- IC designers have to think in a 3D fashion

New concepts enabled by 3D integration of readout chips

VIPS 2010, 22-24 April 2010, Pavia, Italy

Fermilab

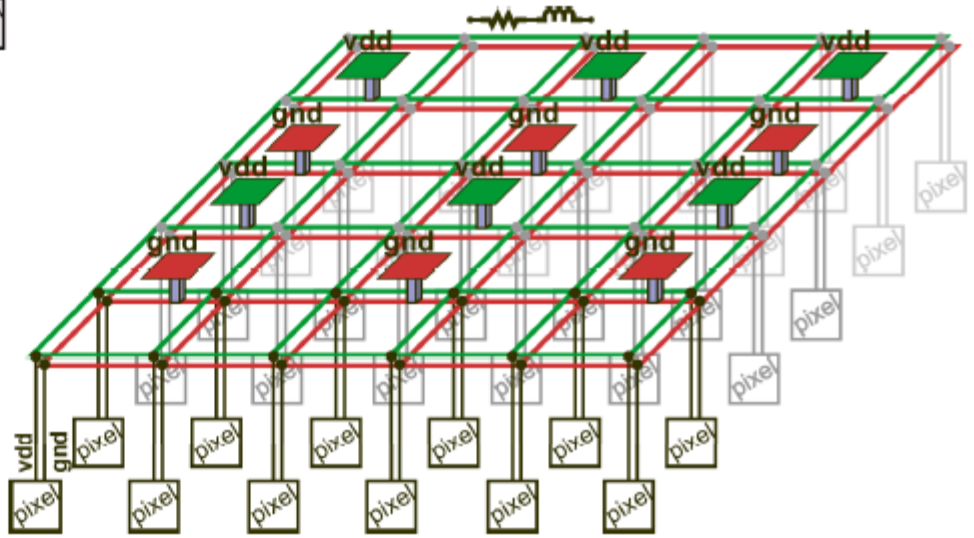
3D-IC opportunities



improvement of power distribution by better power mesh

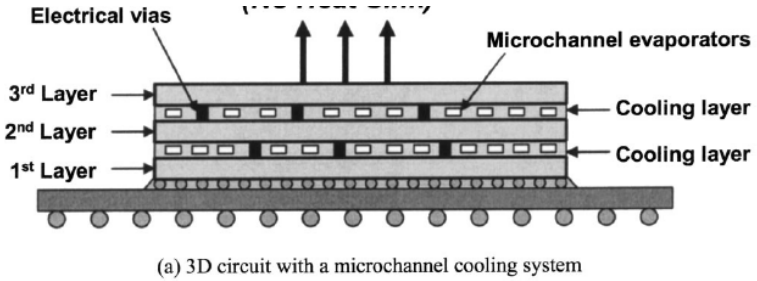
- **2D realizations of pixel ROICs suffer from voltage drops due to resisitivity of power lines and inter-pixel couplings due to their resisitvity**
  - Differences in power supply voltages for pixels close to pads and in the center
  - Use of wide metal paths and multiple layers for minimizing voltage drops

- **3D realization of pixel ROICs allow uniform distribution of power supply pads on the back side of the chip and have them connected to the power distribution mesh using TSVs**
  - Careful planning of TSV access points ot the power mesh is required
  - Pixels from the center and from the periphery are uniformingly supplied
  - Less metal used for power suply distribution = more available for routing



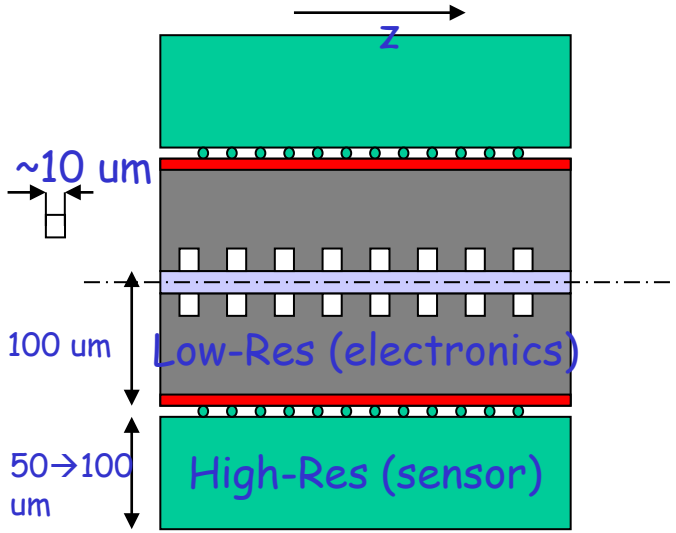
Not only sensors and electronics: the cooling system

- Vertically integrated devices stimulate an innovative approach to cooling systems:
  - Requirements are potentially more severe, since generated power per unit of area available for cooling can increase in a sizable way
  - It is necessary to reduce the impact of the cooling system on the material budget



(a) 3D circuit with a microchannel cooling system

- Microchannel cooling
  - Conservative solution: microchannels in the mechanicla support of the sensors
  - Innovative solution: microchannels in the silicon wafers with front-end electronics



Status and perspectives of vertical integration in our field

Interest for 3D vertical integration in the scientific community is rapidly growing, and INFN is playing a major role:

3D-IC consortium

AIDA WP3

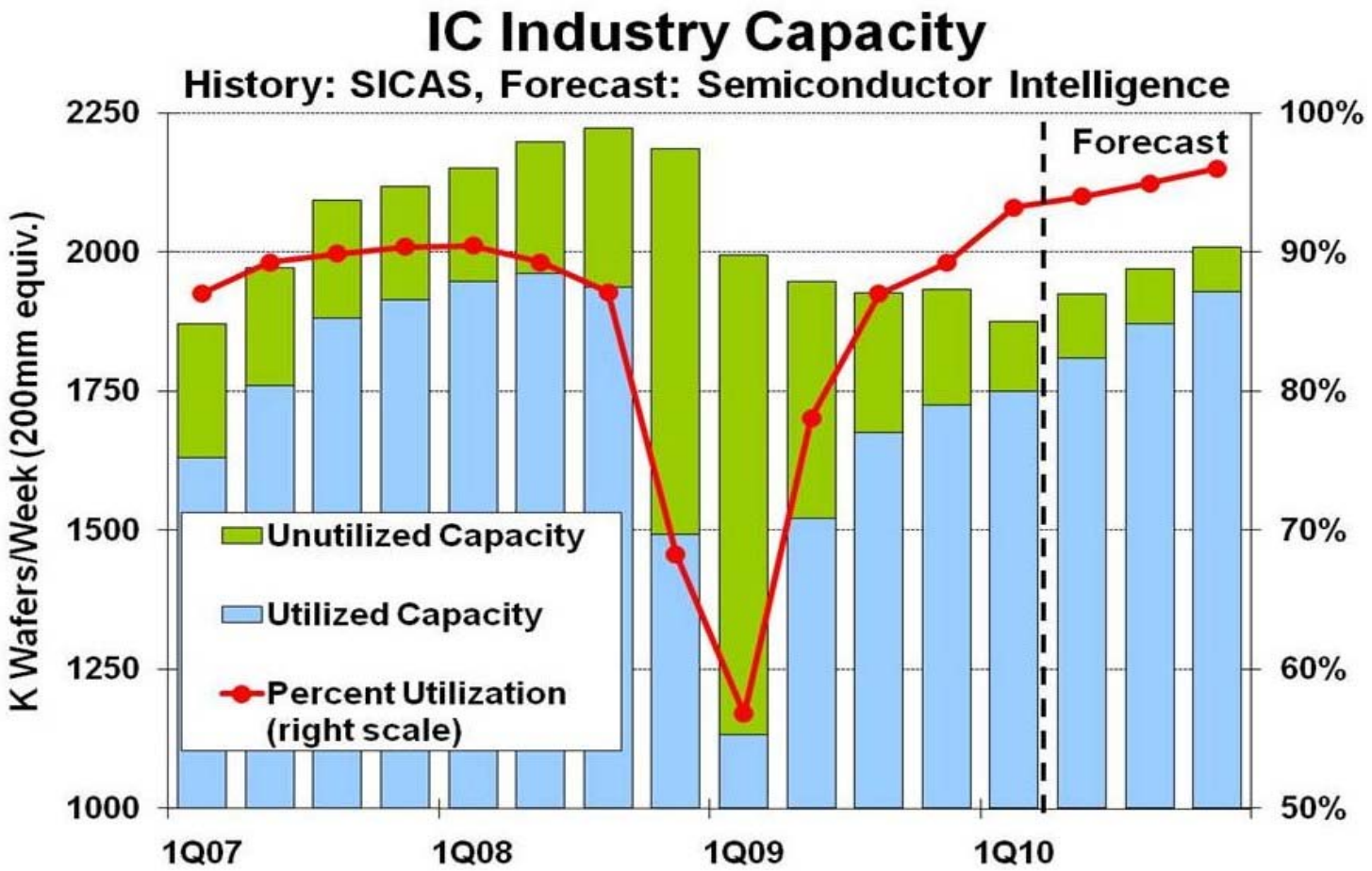
VIPS Facilitation Group

Microelectronics brokers (CMP, MOSIS,..) and 3D MPW runs

3D SOI_KEK consortium, MPI and IZM Munich, FNAL and MIT-LL

The community is working with several 3D vendors, and progress is generally slow

As we knew from the beginning, semiconductor industry is entirely driven by market cycles and big customers, which affects the production schedule of our 3D devices



- From MOSIS (8/2010):

  "IBM has recently indicated that due to capacity constraints, IBM 10LPe (65 nm) runs are being removed from the MPW schedule"

- From CERN (9/2010):

  "we have been informed by the foundry that due to high production workload the fabrication schedule of the CMOS8_MPW1 (IBM 130 nm) is delayed".

The second 3D-IC run: technology changes

Recent Developments for Future Runs:

- Chartered to stop TSVs on 8 inch 130 nm CMOS wafers for the foreseeable future
- Chartered agrees to process wafers from FEOL through M4
- Tezzaron will have TSVs added outside the foundry, from M4 down into the substrate and complete the BEOL processing including the bond interface metallization
- Implication is that space will need to be left open on M1-M4 for the vias to pass through.
- Future potential benefit will be that wafers from other foundries (also with mixed technologies, e.g. 65 nm, SiGe,…) can use the Tezzaron 3D process.
- In Europe, the run will be handled by CMP.

V. Re

3D-IC Consortium

- ✓ In late 2008 a large number of international laboratories and universities with interest in High Energy Physics formed a consortium for the development of 3D integrated circuits (web page: http://3dic.fnal.gov) hosted by Fermilab
- ✓ Multi-Project Wafer runs allow to share the price by sharing the reticle area (prototype fabrication, low volume productions: some hundreds to hundred thousands parts)
- ✓ **First step: MPW runs in the Tezzaron/Chartered 3D technology**

- ✓ Consortium **presently** comprised of 17 members from 7 countries

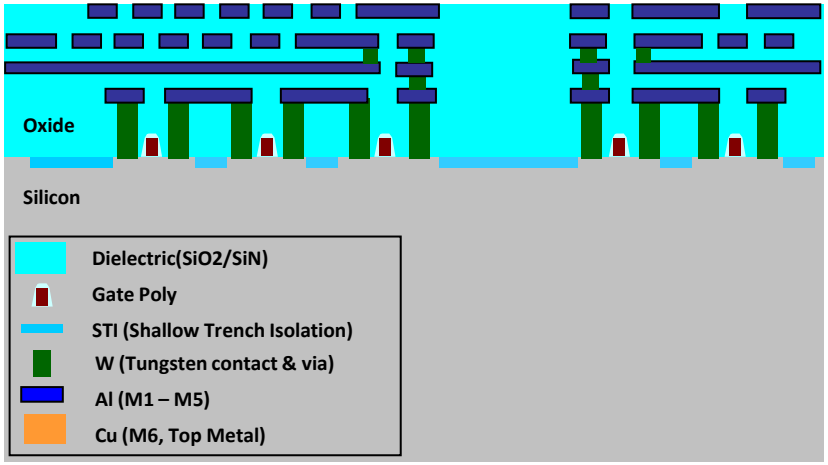
- ✓ Fermilab, Batavia
- ✓ University of Bergamo
- ✓ University of Pavia
- ✓ University of Perugia
- ✓ INFN Bologna
- ✓ INFN Pisa
- ✓ INFN Roma 3
- ✓ CPPM, Marseilles
- ✓ IPHC, Strasbourg
- ✓ IRFU Saclay
- ✓ LAL, Orsay
- ✓ LPNHE, Paris
- ✓ CMP, Grenoble
- ✓ University of Sherbrooke
- ✓ University of Bonn
- ✓ AGH University of Science &Technology, Poland
- ✓ Universitat de Barcelona

- ✓ Benefits:
  - ✓ Sharing of designs
  - ✓ Development of special software programs
  - ✓ Development of libraries and test structures
  - ✓ Design review
  - ✓ Sharing of results
  - ✓ Frequent meetings
  - ✓ Cost reduction

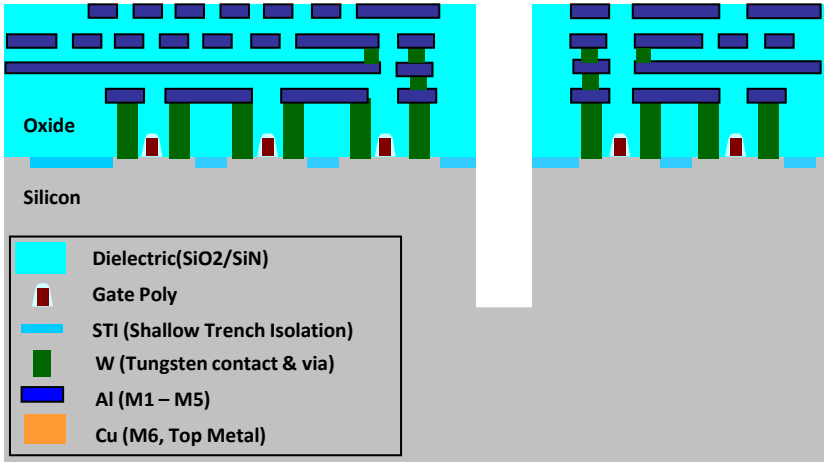
V. Re

New Tezzaron Process Flow using “Near End of Line” TSV

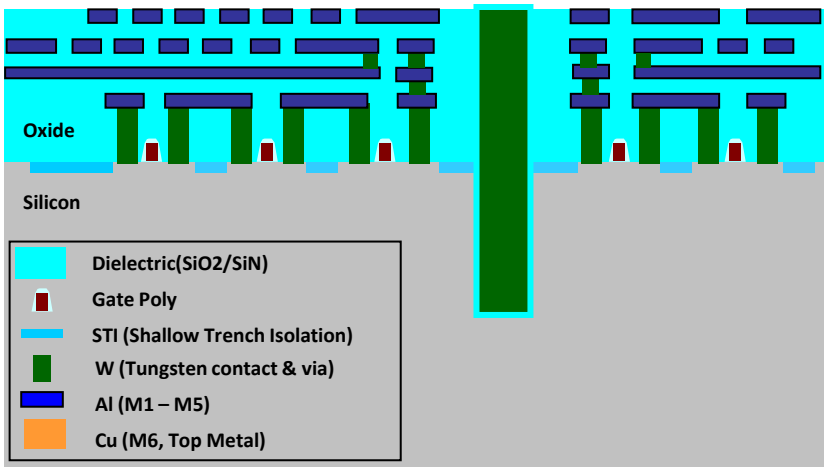
CNRS – INPG – UJF



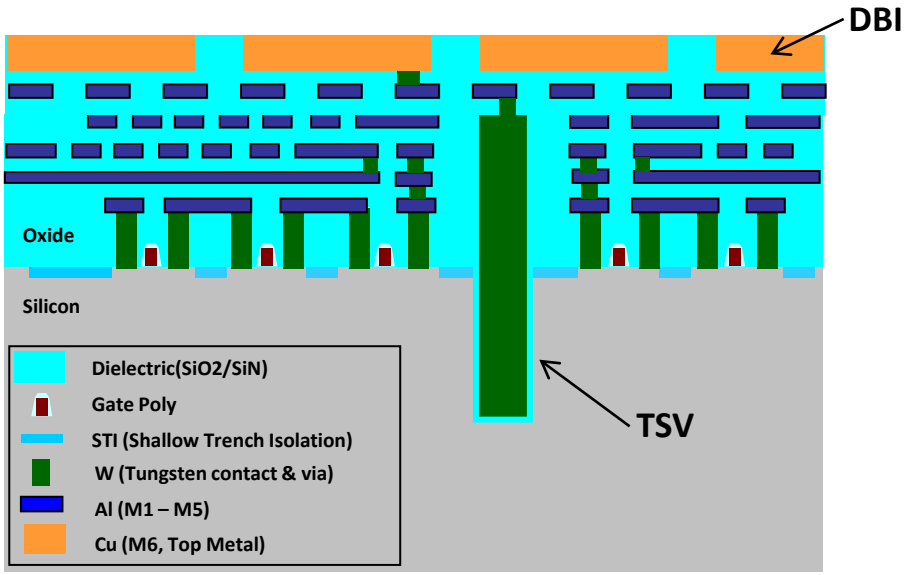
1- Standard CMOS process stopped at MET4



2- Deep etching (DRIE)



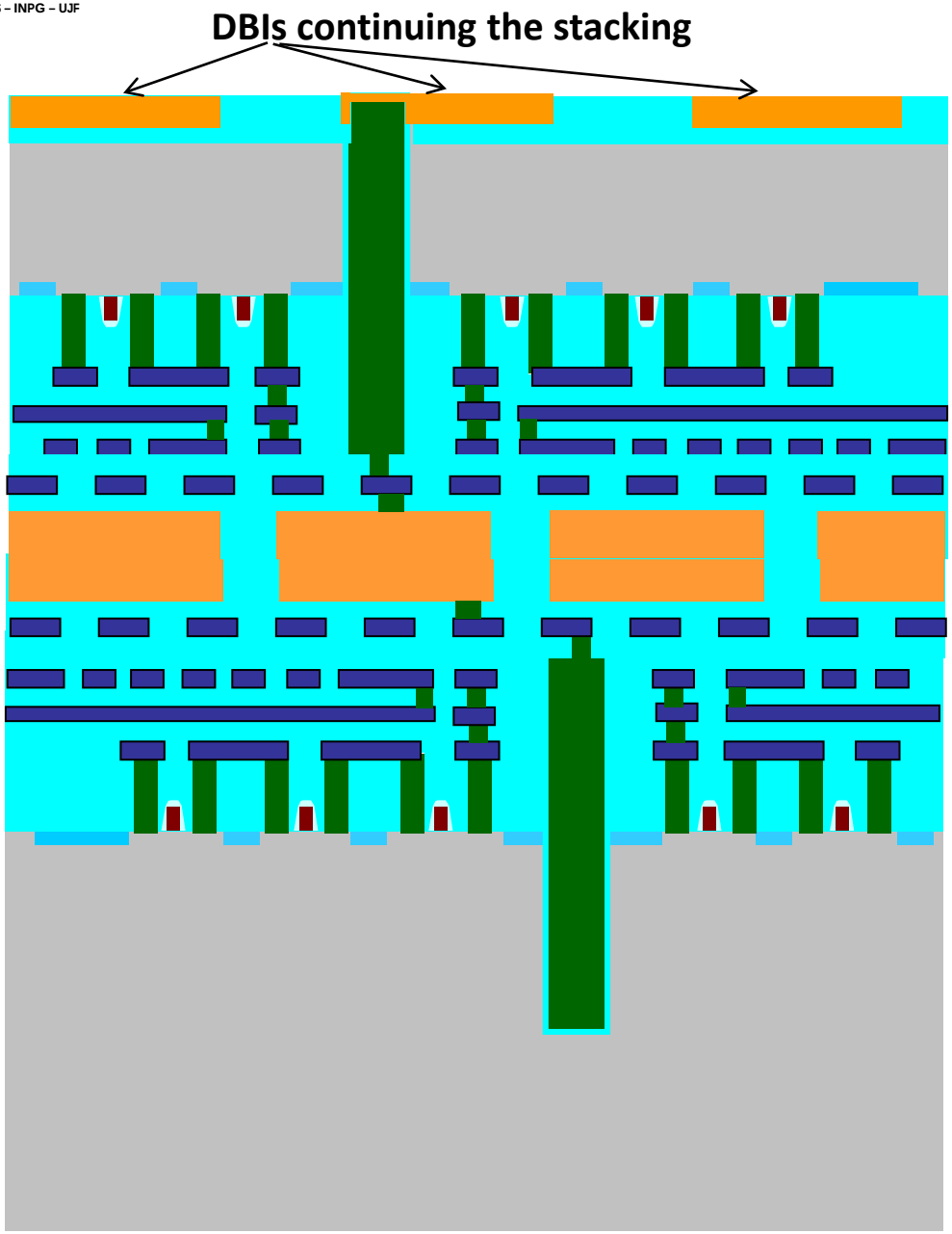
3- Dielectric isolation and TSV formation

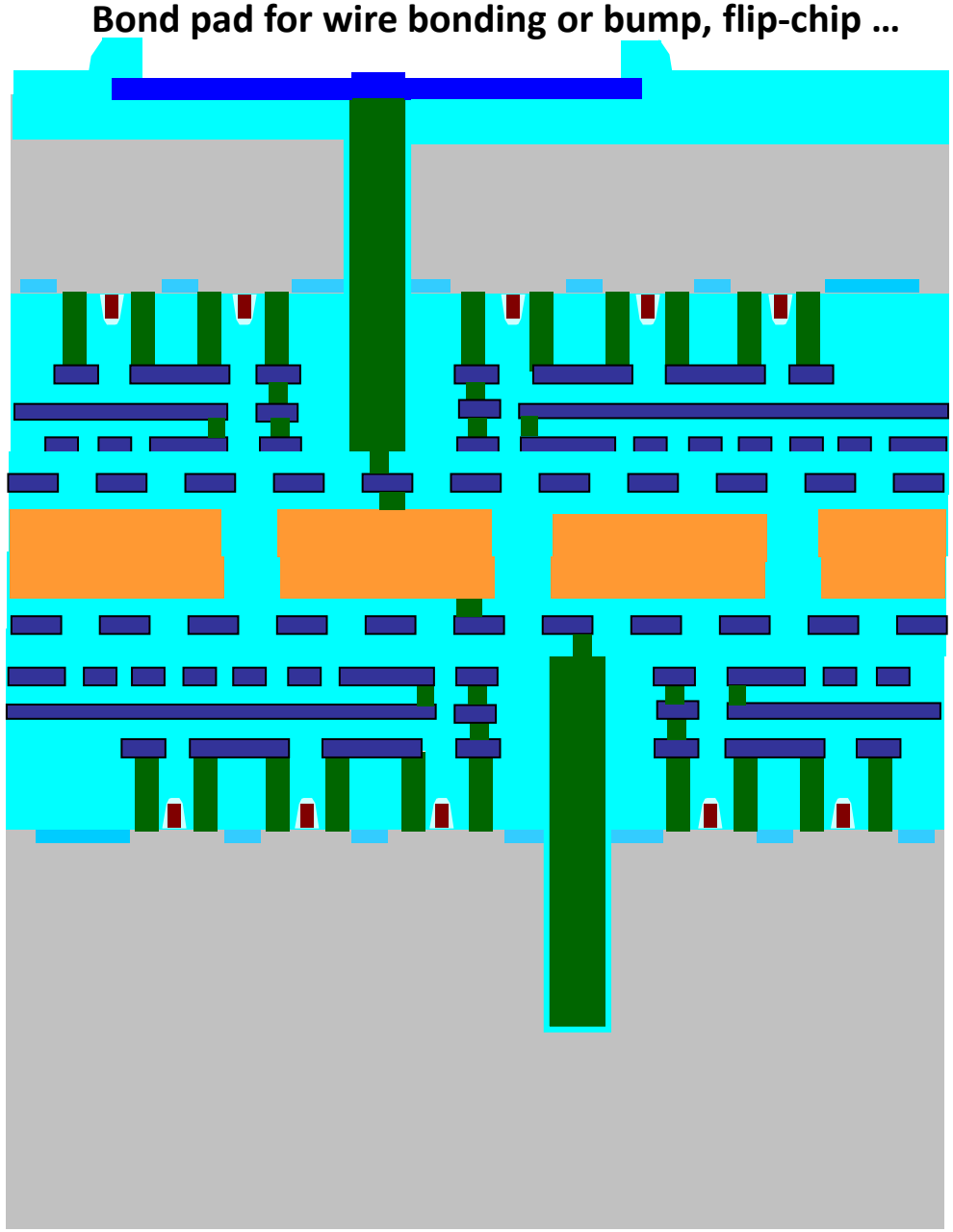


4- Continue BEOL with Via4 / M5 / Via5 / M6

New Tezzaron Process Flow using “Near End of Line” TSV

CNRS – INPG – UJF





Conclusioni

- Lo sviluppo delle tecnologie microelettroniche verso l'integrazione verticale 3D genera delle opportunità molto interessanti

- Le tecnologie di integrazione verticale sono una novità assoluta per la nostra comunità e avranno un impatto rilevante sui rivelatori nei futuri esperimenti di fisica delle alte energie, oltre che in applicazioni mediche e photon science

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8) SOI Pixel Collaboration. http://rd.kek.jp/project/soi/.
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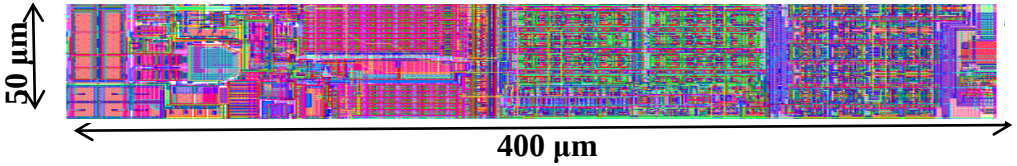
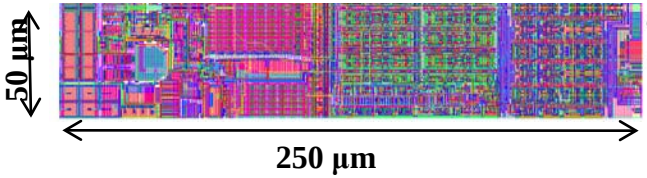
Backup slides

Hybrid pixel detectors (Atlas example)



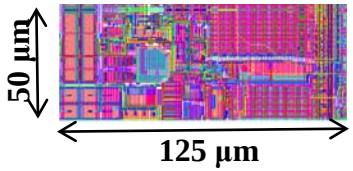
FE-I3 CMOS 250 nm

Done : ATLAS



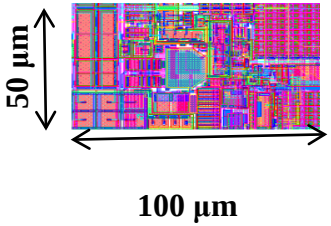
FE-I4 CMOS 130 nm

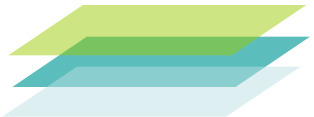
Design



Drastic pixel dimension reduction (*cost effective compared to smallest technologies ?*)

Thought





4 sides buttable structures

New mechanical possibilities

Dream ?

Why hybrid-pixel-like MAPS

- Modern VLSI CMOS processes (130 nm and below) could be exploited to increase the functionality in the elementary cell

  $\Rightarrow$ sparsified readout of the pixel matrix.

- Data sparsification could be an important asset at future particle physics experiments (ILC, Super B-Factory) where detectors will have to manage a large data flow

- A readout architecture with data sparsification will be a new feature which could give some advantages with respect to existing MAPS implementations

  $\Rightarrow$ flexibility in dealing with possible luminosity and background changes during the experiment lifespan, decouple modularity from readout speed

- An ambitious goal is to design a monolithic pixel sensor with similar readout functionalities as in hybrid pixels (sparsification, time stamping)

3D Vertical Integration: the Italian VIPIX collaboration

- **"Pixel systems for thin charged particle trackers based on vertical integration technologies" - VIPIX**
  (INFN Pisa, Pavia, Bologna, Trieste, Trento, Perugia, Roma3, Torino)

- Members of the CMOS-3DIT Consortium (FNAL-IN2P3-INFN)

Main goals of the VIPIX collaboration:

1. **Interconnection between 2 (or more) CMOS layers,**
   a) **Deep N-Well MAPS are evolving towards vertical integration.** A design with a 2 tier structure (sensor&analog tier + digital tier) is pursued to improve performance (smaller pitch, higher efficiency, increased pixel functionalities)

2. **Interconnection between a CMOS readout electronics chip (2D or 3D) and a fully-depleted high resistivity sensor**
   a) with bump bonding (standard, but low pitch may be needed)
   b) with a vertical integration technique (low material budget, more advanced)