FAST FRONT-END ELECTRONICS

Part I: Fast sampling circuits

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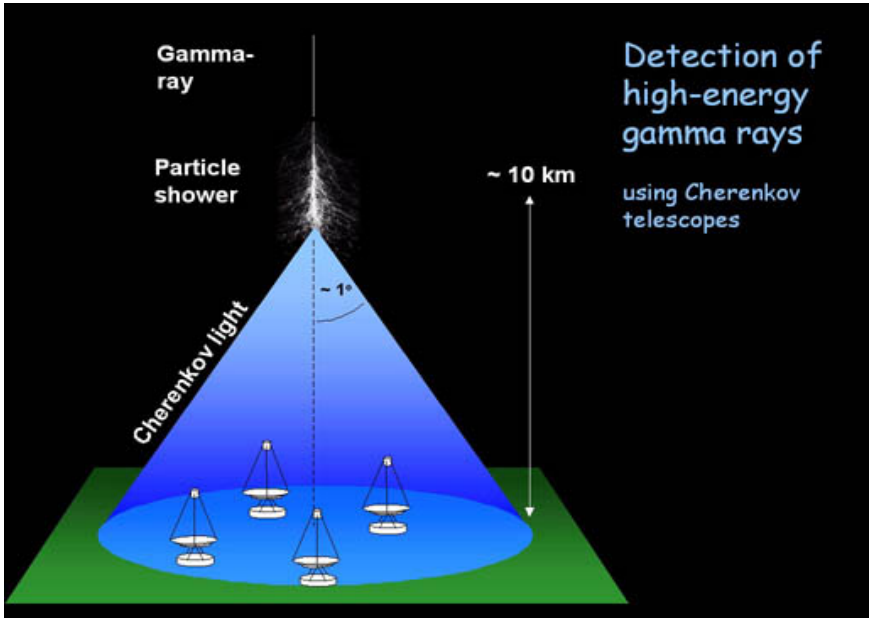
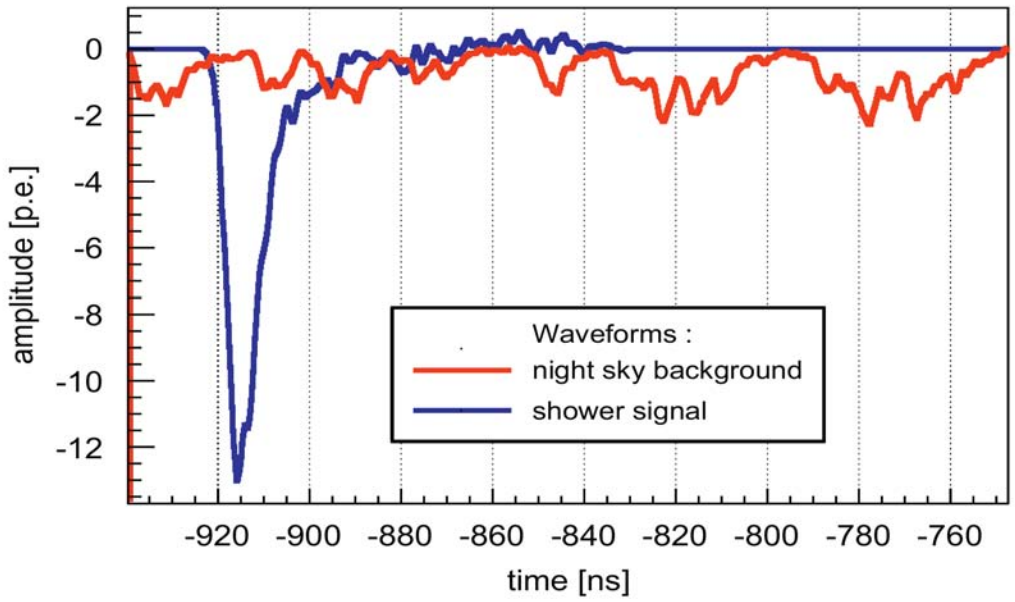
Lectures contents

- **Front-end electronics**
  - Circuits reading a signal from a detector and sending data out after some preliminary elaboration;
  - Multi-channel systems implemented in the form of custom VLSI circuits.
- **Fast:**
  - Circuits capable of sampling rates > 1 GHz.
  - Circuits capable of events rate > 100 kHz.
- **Today topics:**
  - Very fast sampling and digitization circuits;
  - Examples from the open literature.
- **Tomorrow topics :**
  - High event-rate and low power circuits;
  - Case studies based on direct experience.

Where very fast sampling is needed?

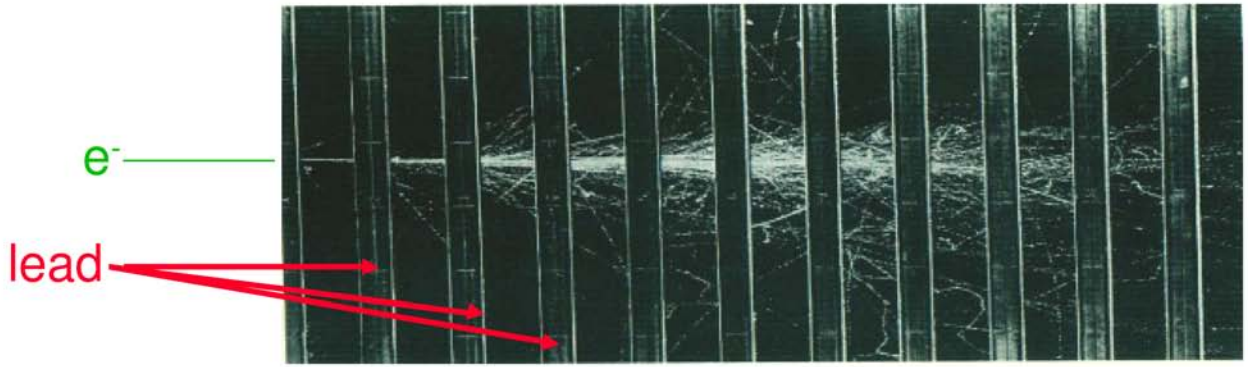
Imaging Cherenkov Telescope Arrays





Something even more exotic....

#1. UHE event will induce an e/γ shower:



Askaryan effect

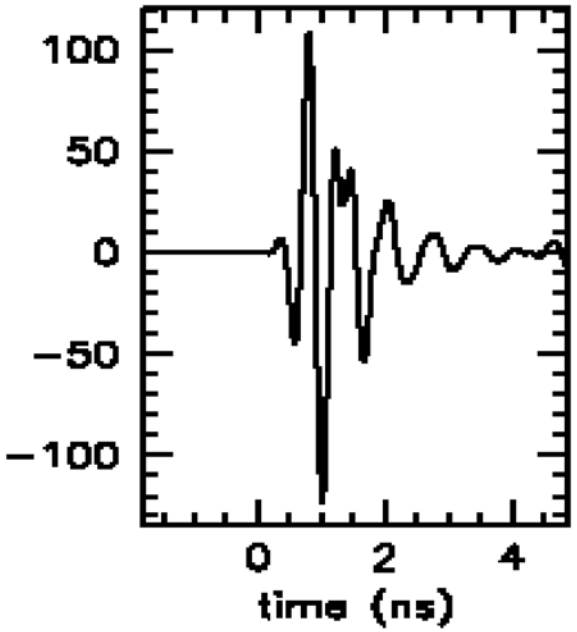
In electron-gamma shower in matter, there will be 20% more electrons than positrons.

Compton scattering: $\gamma + e^-_{(at\ rest)} \rightarrow \gamma + e^-$

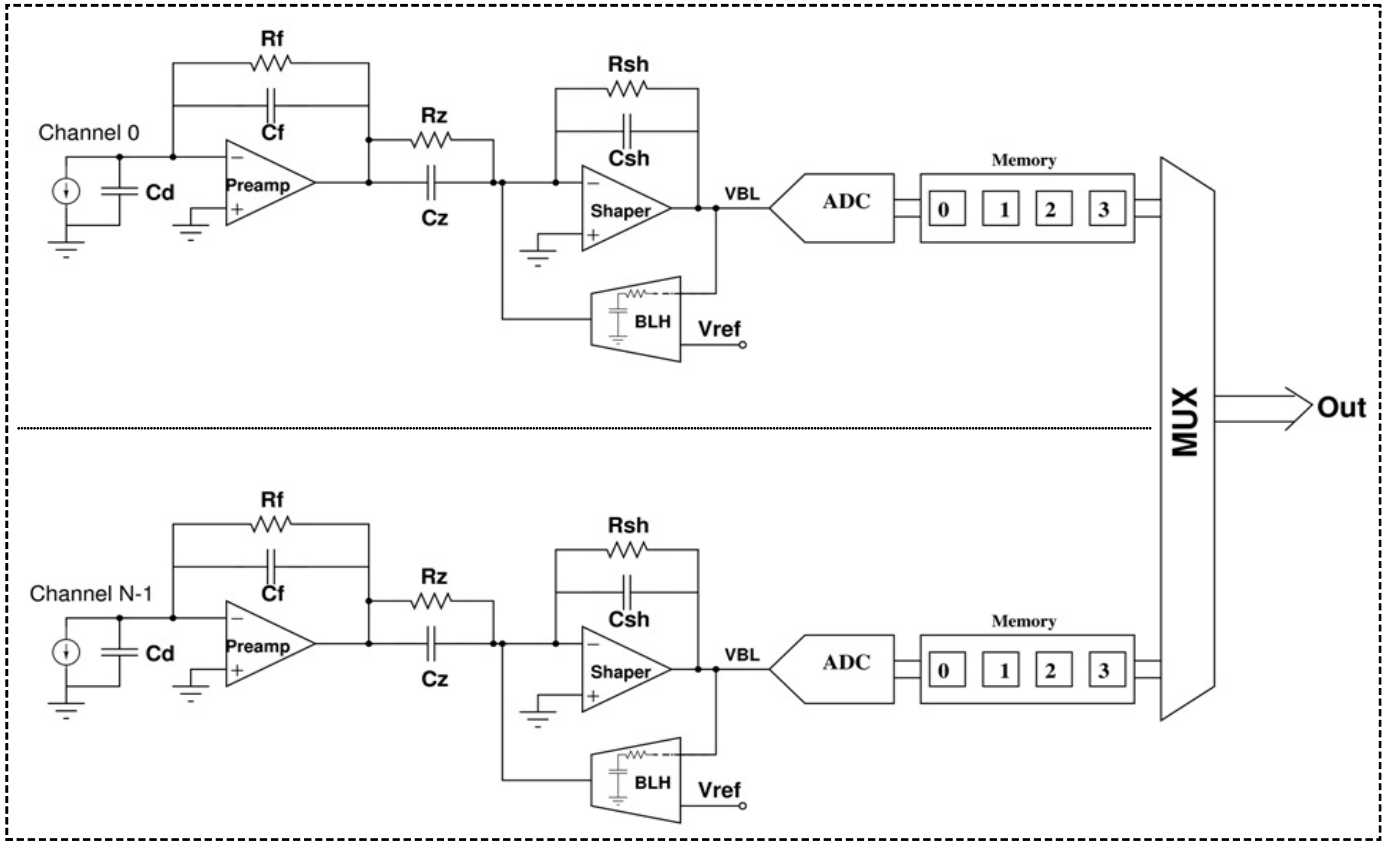
Positron annihilation: $e^+ + e^-_{(at\ rest)} \rightarrow \gamma + \gamma$

#2. Excess charge moving faster than *c/n* in matter emit Cherenkov Radiation

$\lambda >> R_{Moliere}$ (microwaves), coherent $\Rightarrow$ $P \propto N^2$

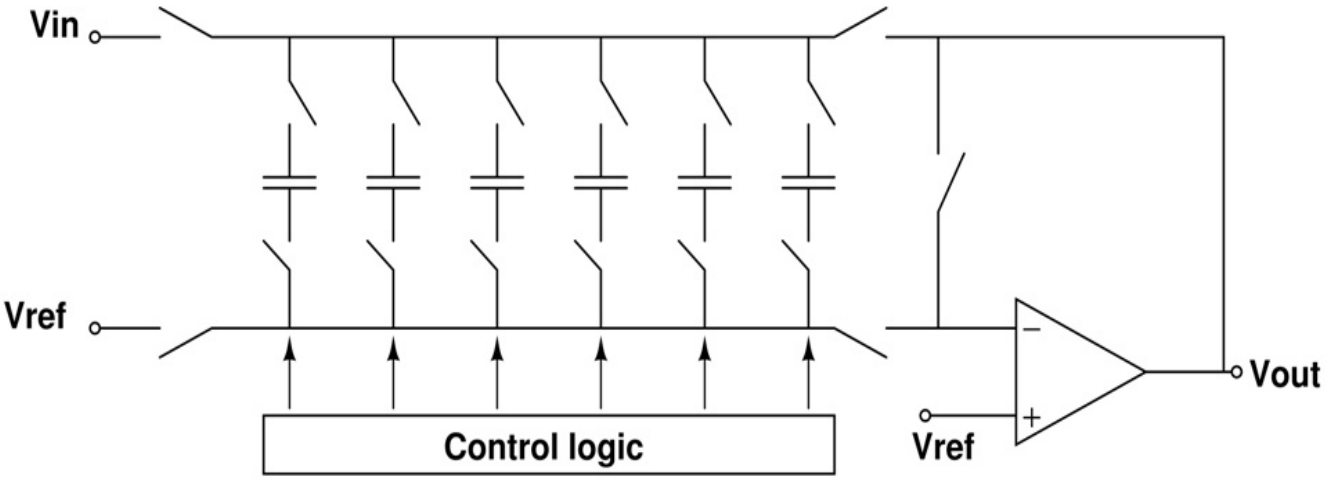


The “ideal” front-end

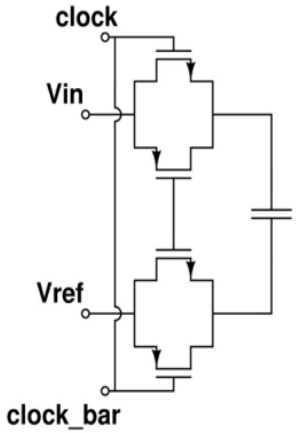


- Early digitization immediately after the front-end amplifier;
- Transfer also the information to the back-end and do the signal selection on FPGA, where selection algorithms can be easily changed/upgraded.
- Transmission bandwidth required for a 64 channel chip sampling continuously at 100 MHz and 8bit resolution: 51.2 Gbit/sec...

Analog memories



a)

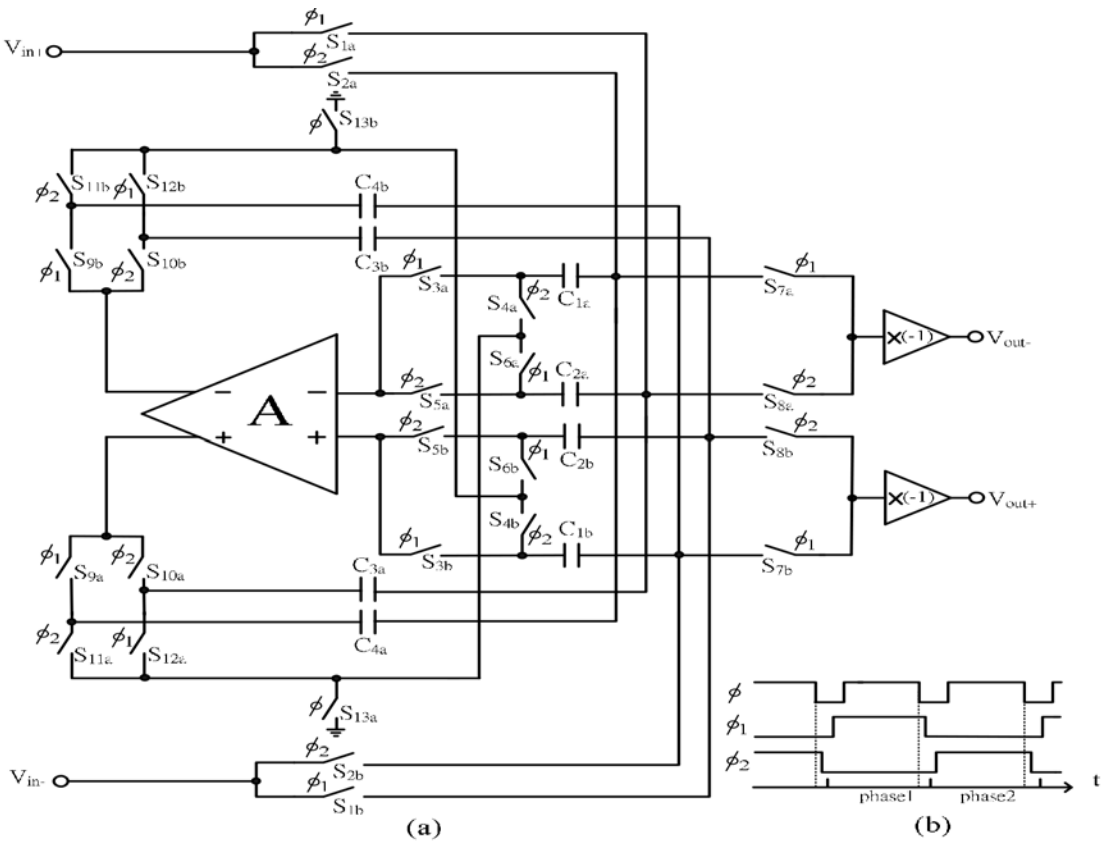


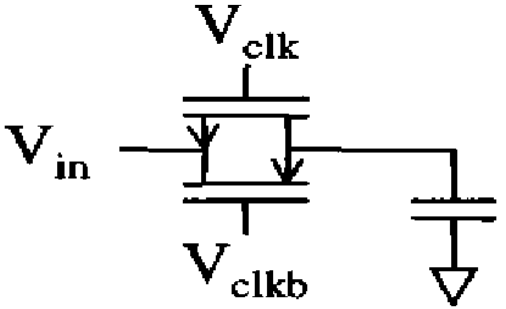
b)

- Decoupling sampling and digitzation/transmission....
- Sampling the analog voltage on a capacitor.
- Sampling is fast and cheap: fast transients can be captured and digitized only if needed;
- More segments can be used to allow arrival time derandomization.
- AM can be combined slower on chip ADCs or with powerful state-of-the art commercial components located off-chip.
- Timing circuit often implemented with shift registers

Popular since the early days of ASICs in particle physics

Different ways of sampling





Typical sampling cells in an analogue memory for HEP

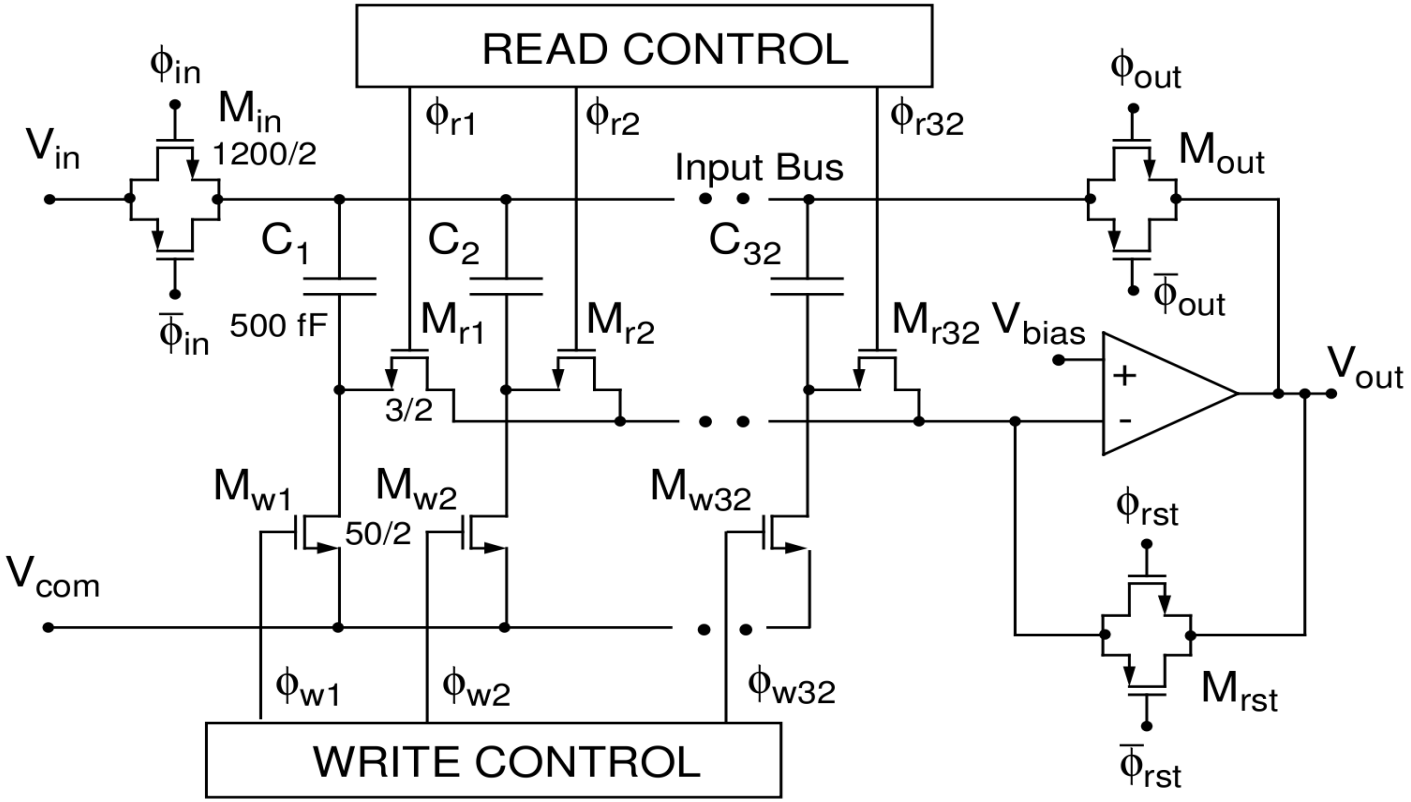
T. S. Lee et al., Proceedings of IEEE ISCAS 2005
6.7 mV, 10 bit linearity.

➔ In detector applications we need large dynamic range but requirements on linearity are less stringent (1% is usually already a good figure);

➔ Complexity of sampling/digitization circuitry tends to grow exponentially with linearity requirements...

Waveform sampling at high frequencies

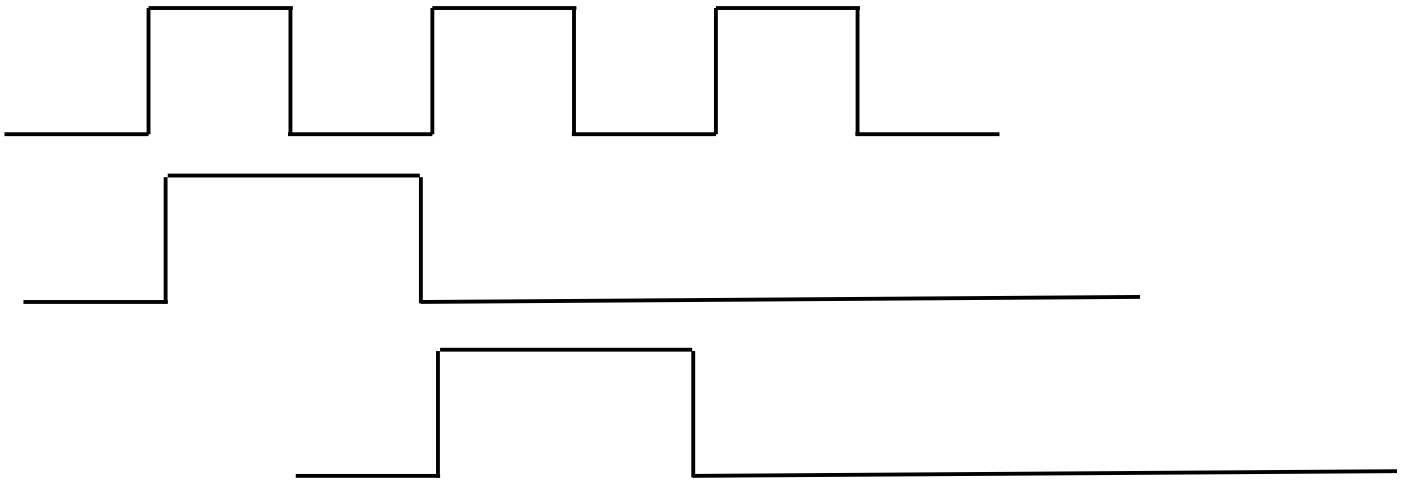
"*A 700-MHz Switched-CapacitorAnalog Waveform Sampling Circuit*"
G. Haller and B. Wooley, JSSC, April 1994.

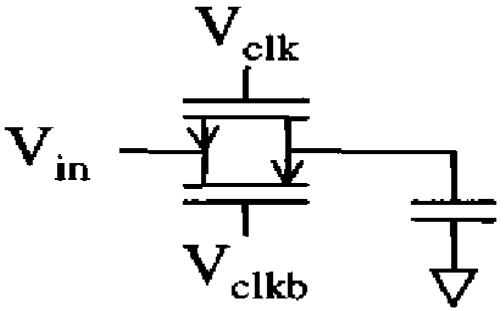


- Replacing the shift register with a delay line to control the write pointer;
- Distance between sampling times defined by delays of digital gates instead of clock;
- Technology: 2 μm, 5 V with poly-poly capacitors.

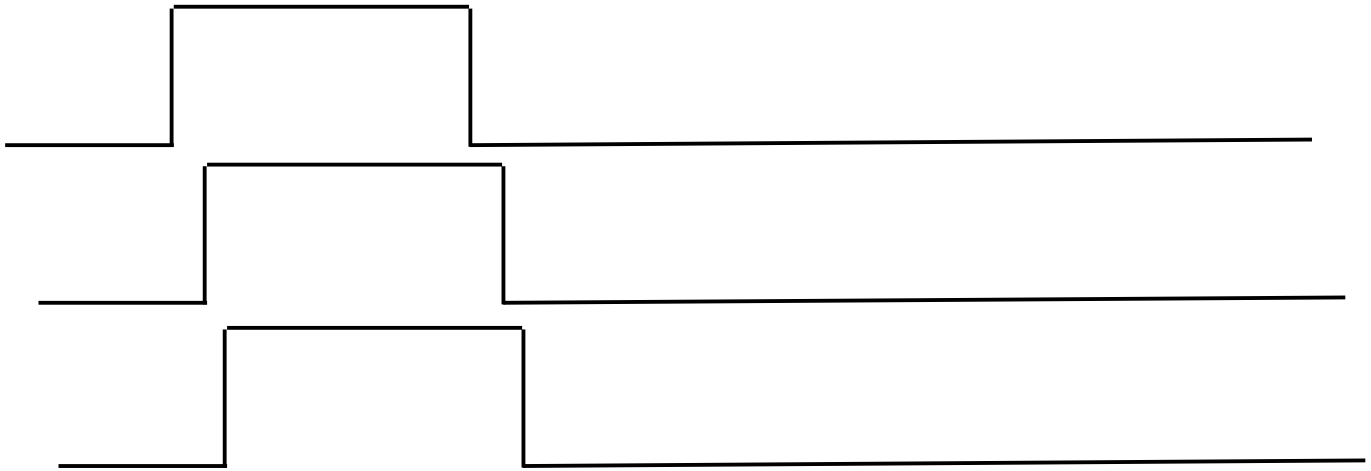
700 MHz sampling rate with 2 mW of power per channel!

Control of the sampling switches





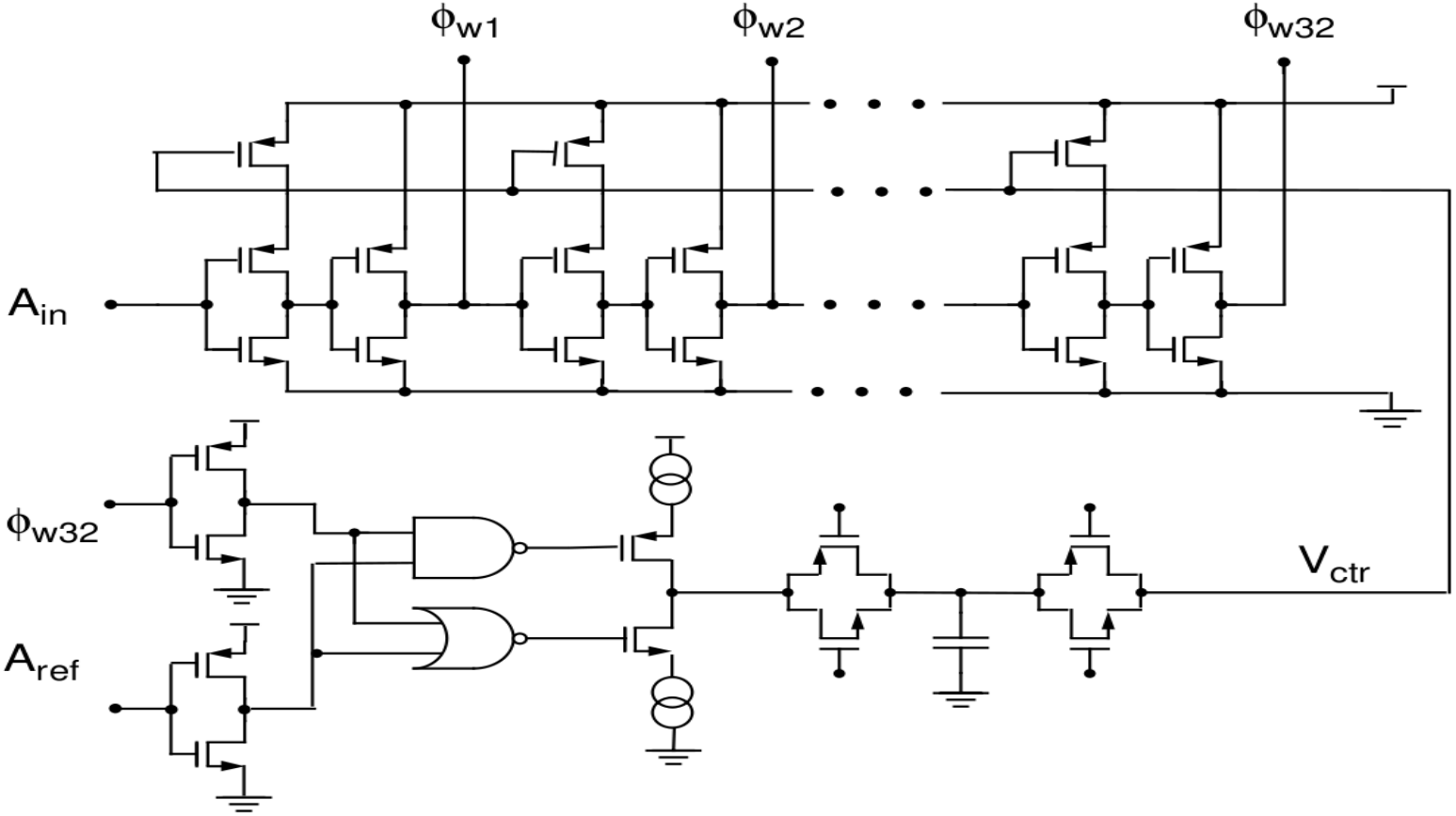
a) Shift registers: time between samples=Tclock



a) Delay line: time between samples=Tdelay

Detail of Haller's sampling circuit

"A 700-MHz Switched-CapacitorAnalog Waveform Sampling Circuit"
G. Haller and B. Wooley, JSSC, April 1994.



- Issues with delay lines: uniformity between timing sampling, changing with temperature...
- Chain of starved inverter with feed-back

Where are we now with modern deep submicron CMOS technologies?

Analog memories in deep submicron: perspectives

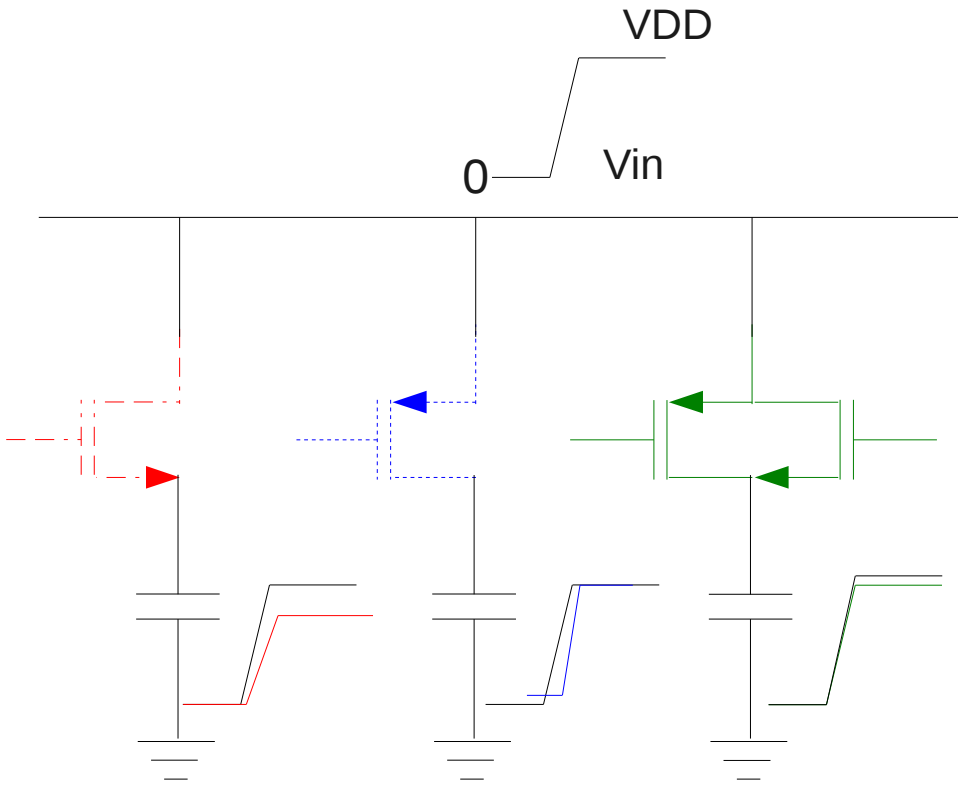
- Deep submicron CMOS technologies offer very fast digital gates.
- Typical gate delay is 50 ps for a 130 nm process.
- Potential for sampling speed in the order of 20 GHz or more.
- Read-out/digitization speed will be of course much slower...
- Capture of very fast transient and possibility of applying powerful DSP processing offline or online with FPGAs.
- Amplitude and good (100 ps...) time resolution in one shot.

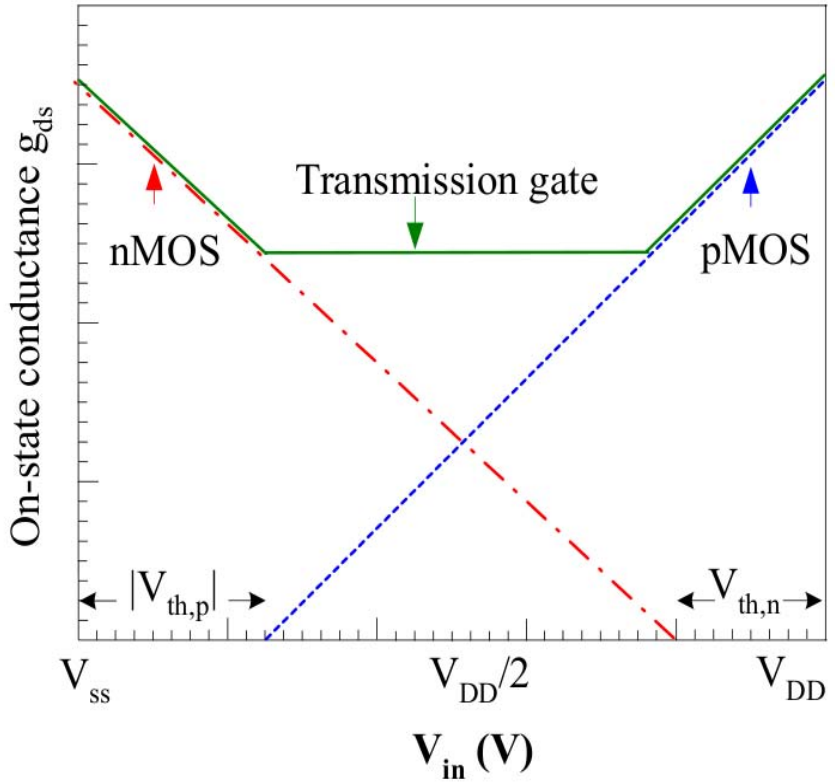
But...

- Deep submicron CMOS technologies operate with low supply voltages
  - ➔ From 3.3 V in 0.35 μm to 1 V in 90 nm.
  - ➔ Need of almost rail-to-rail operation to have acceptable dynamic range.
- Poly-to-poly capacitors not available in deep submicron. Need to find alternatives.

Analog memories in deep submicron: switches

- Use of CMOS switches in the signal path for reasonable dynamic range;
- Even in this case keeping a conductive path can be challenging.

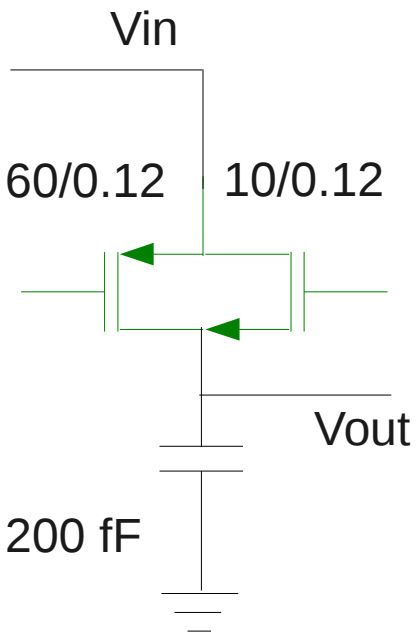


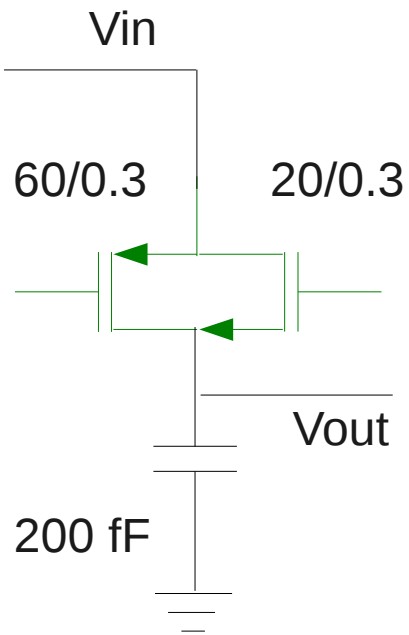


- Non uniform switch resistance across the signal path leads to harmonic distortion.

Sampling cells in 0.13 µm CMOS

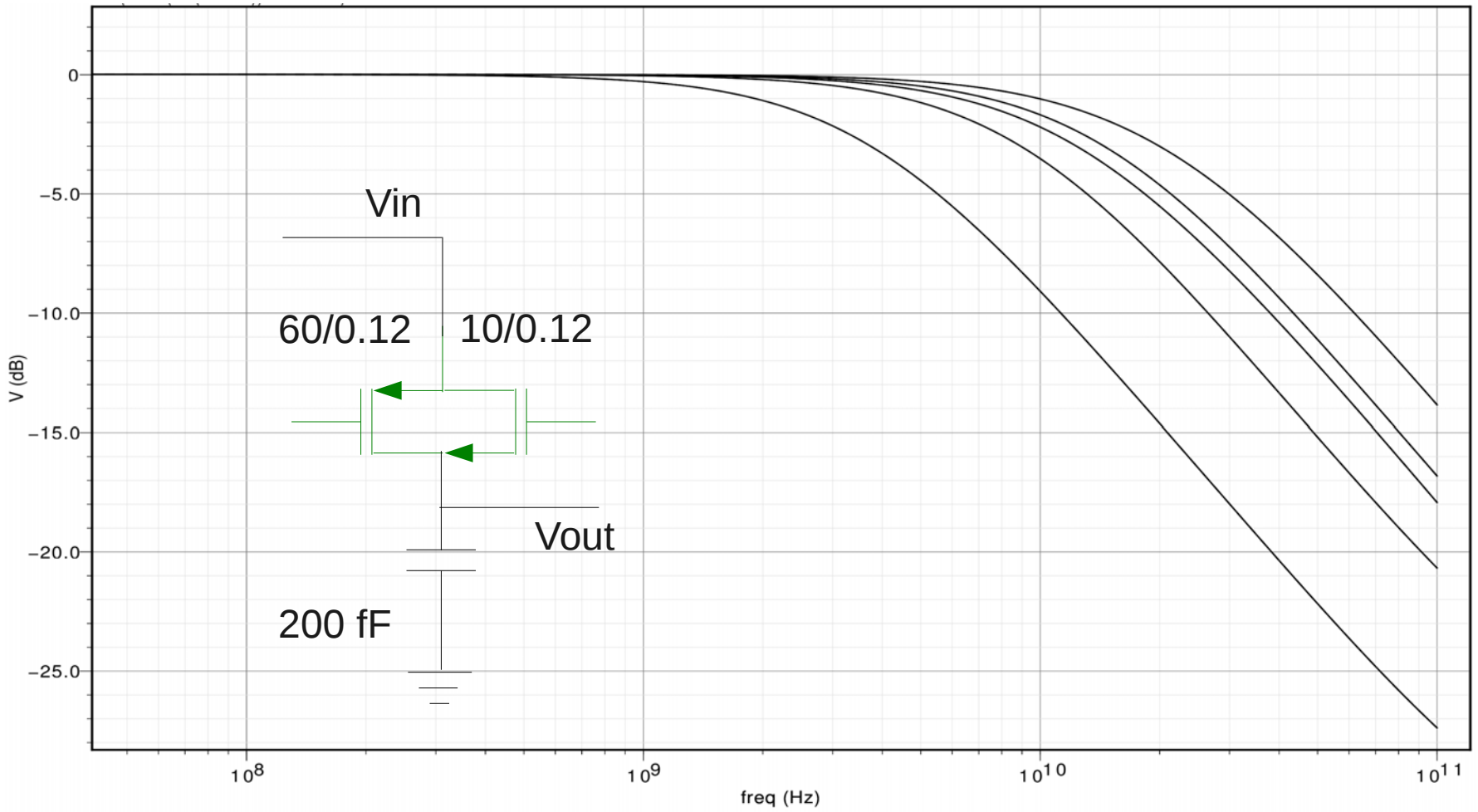
- Two different set of switches considered with same W and different L;
- Bandwidth measured as a function of the input dc level;
- Simulation with typical mean condition @ 27 C.





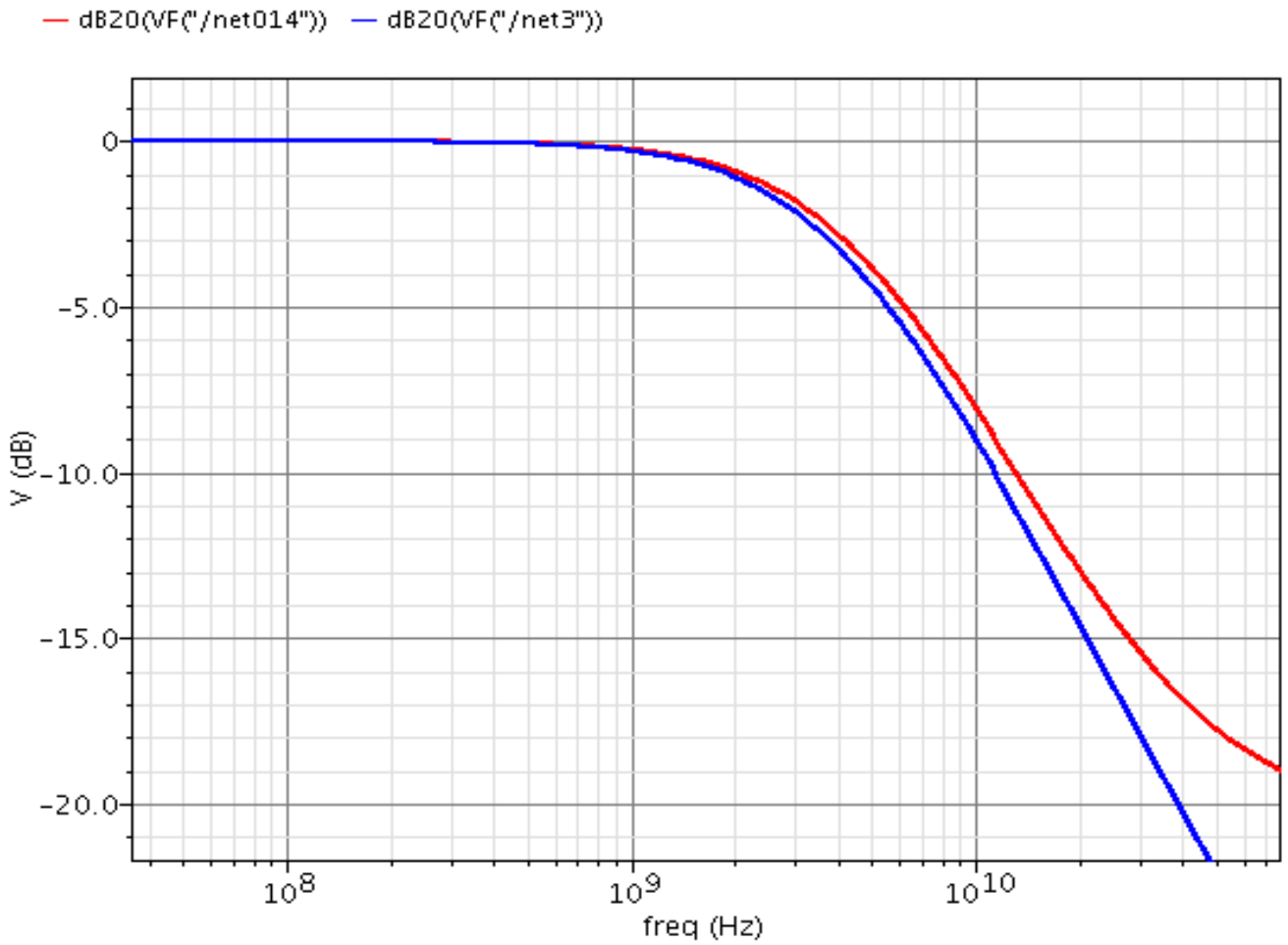
Example of bandwidth performance

- With simple CMOS switches huge bandwidth variation as a function of signal level.
- Worst point: 0.6 V (middle of dynamic range) => BW= 3.76 GHz
- Best point 0 V (NMOS in full conduction) => BW = 20.6 GHz.



Comparison of different switch size

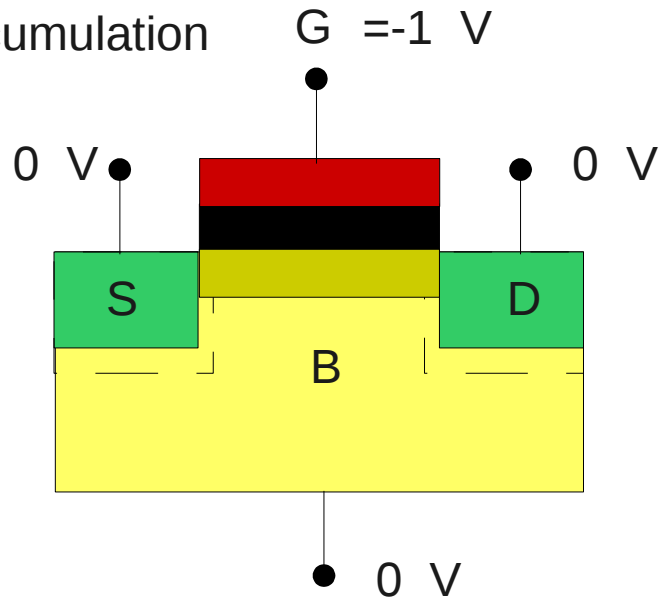
- Red curve: switch size 20/0.3 for NMOS and 60/0.3 for PMOS: bandwidth 4.2 GHz.
- Blue curve: switch size 20/0.12 for NMOS and 60/0.12 for PMOS: bandwidth 3.7 GHz.



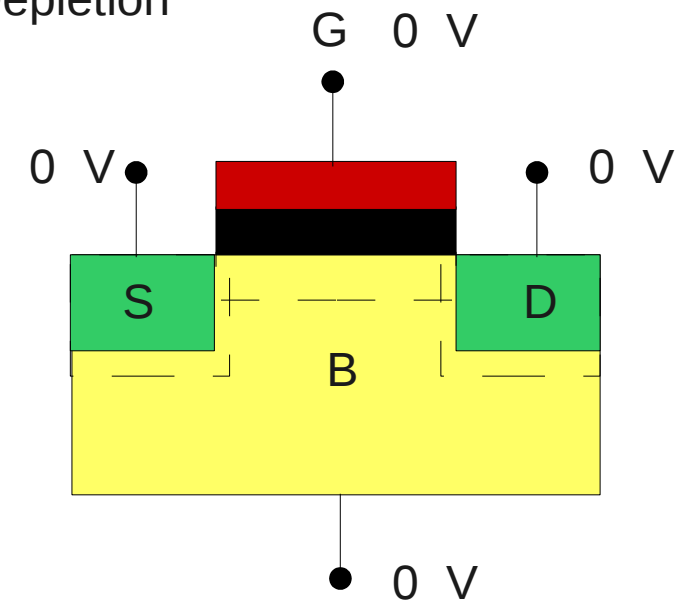
Longer switches conduct better than minimum length one: reverse short channel effect

MOS operating regions: a quick resumé

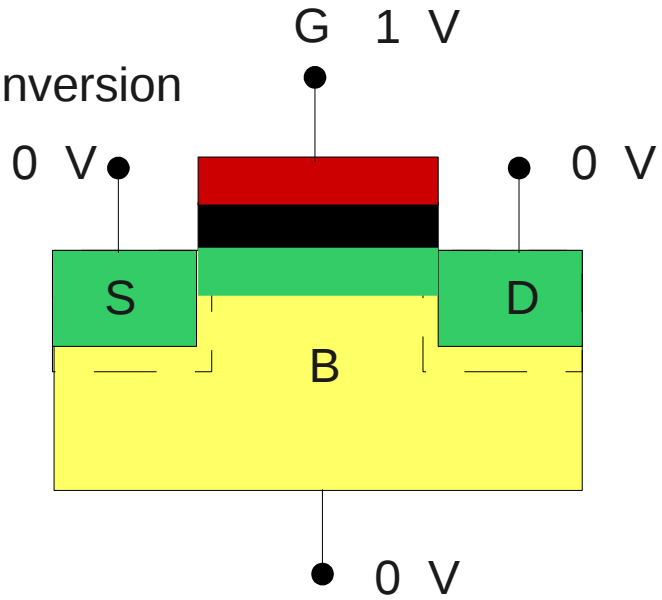
Accumulation



Depletion

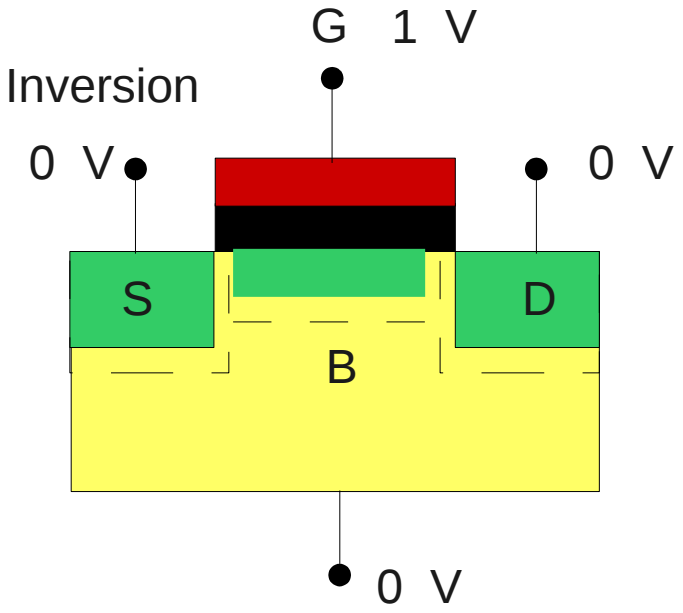


Inversion



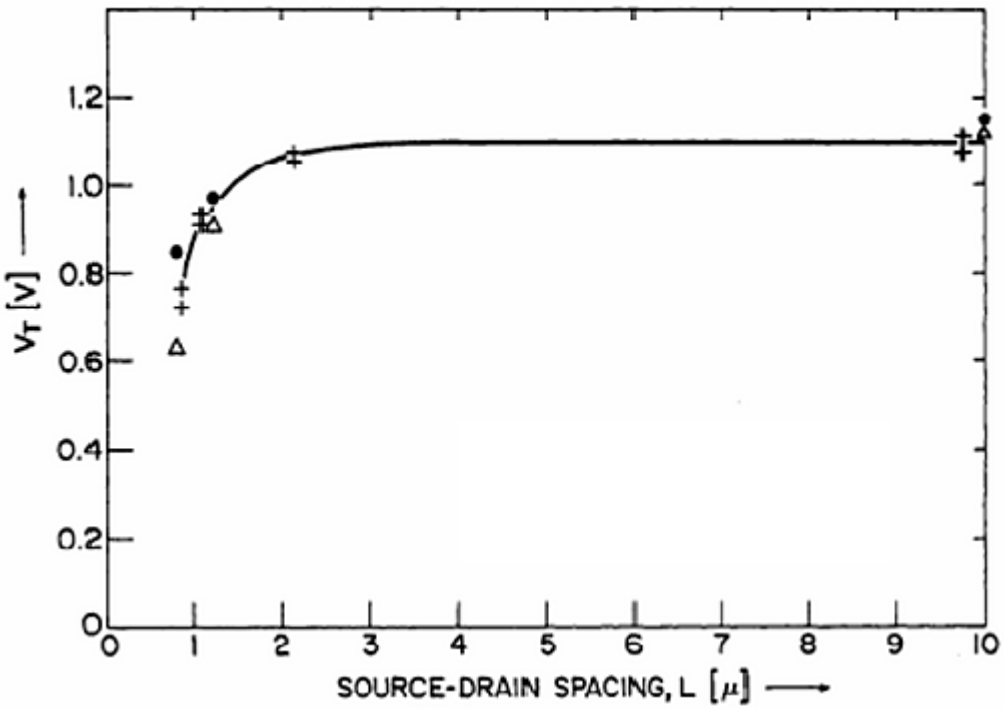
Switch on resistance: $Ron = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$

Standard short channel effect

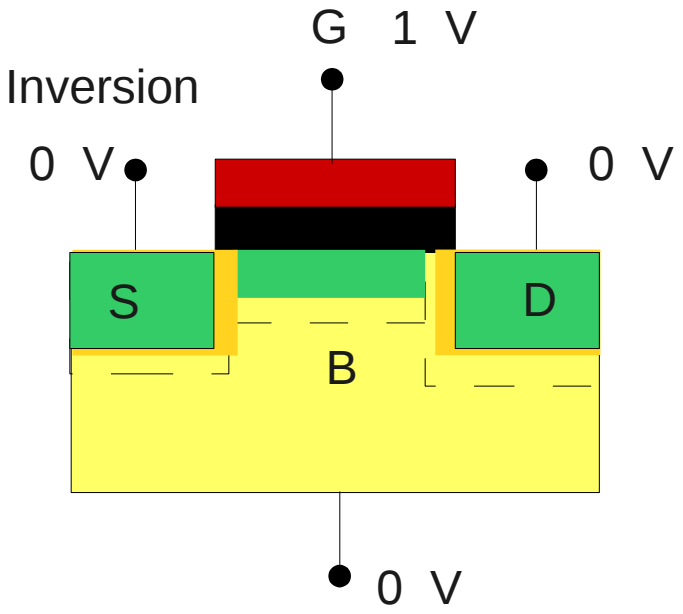


- The gate voltage needs to maintain also the depletion region.
- For short channel device source and drain depletion regions protrude significantly in the channel.
- For the same charge store on the gate, more carriers can be attracted in the channel, since the depletion region is partially supported by source/drain

Example of traditional short channel effect: threshold is lower as channel length is decreased.

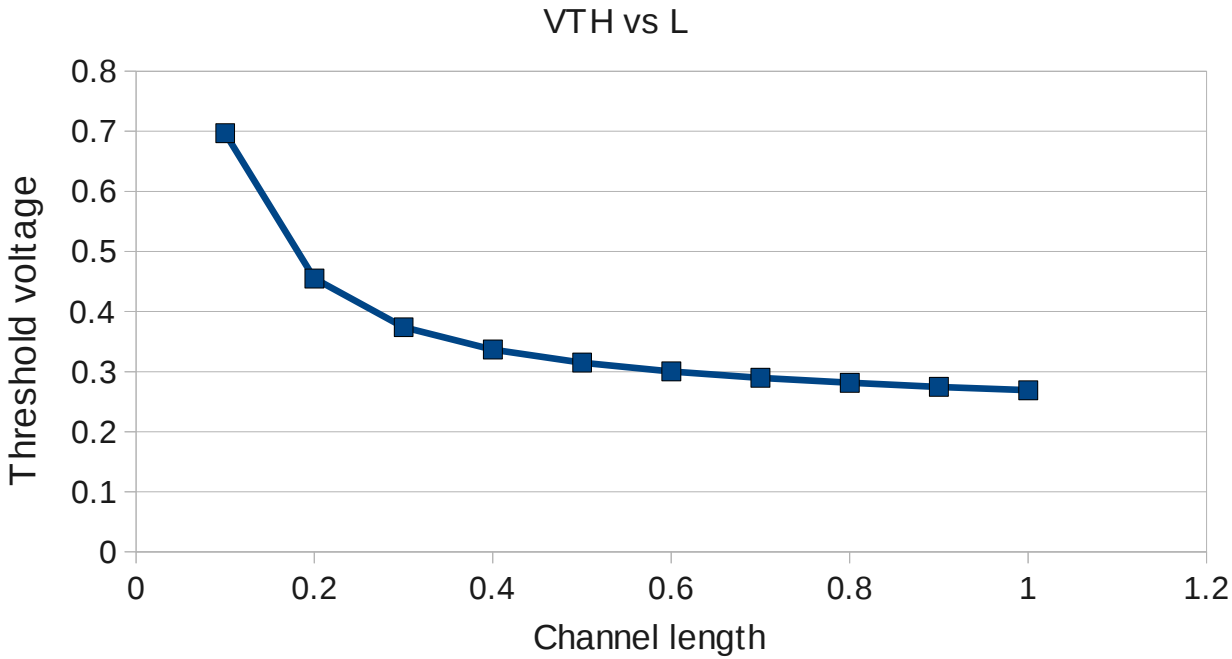


Reverse short channel effect



- To prevent excessive extension of the source-drain depletion region into the regions around the electrodes receive a stronger substrate doping (halo doping).
- When the channel is very short the two regions tend to overlap, the local substrate doping in the channel region is increased and the threshold voltage increases.
- Another reason to keep away from minimum length devices in analog design!

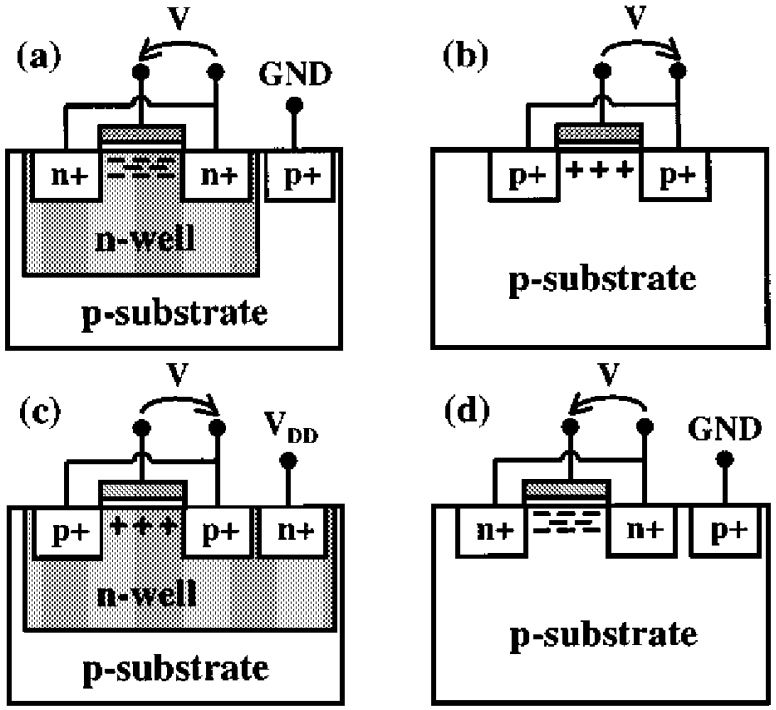
Reverse short channel effect: simulated threshold variation as a function of channel length in a 90 nm CMOS process.

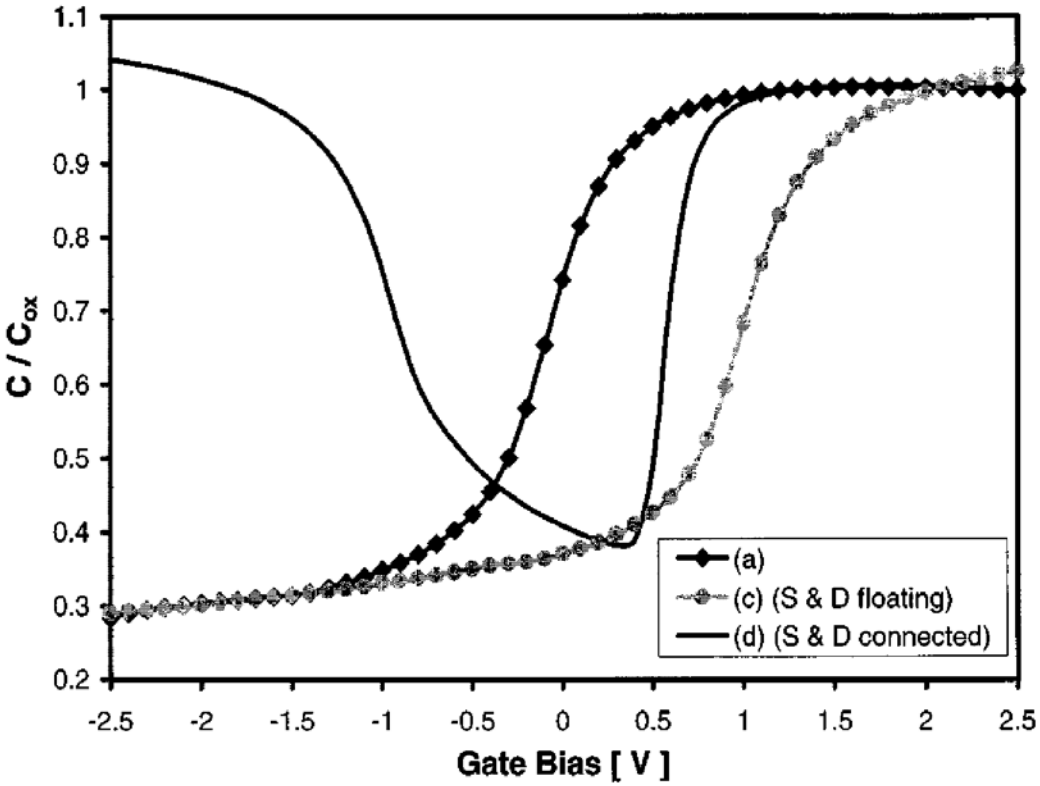


Which capacitor for storage?

- Poly-poly capacitors in general not available beyond 0.35 μm CMOS.
- Alternatives: MOS capacitors, metal-insulator-metal, vertical capacitors.
- MOS capacitors in analogue memories in DST:

G. Anelli, F. Anghinolfi and A. Rivetti: "A Large Dynamic Range Radiation Tolerant Analog Memory in a Quarter Micron CMOS Tecnology", *IEEE TNS, vol. 48, no. 3, June 2001.*

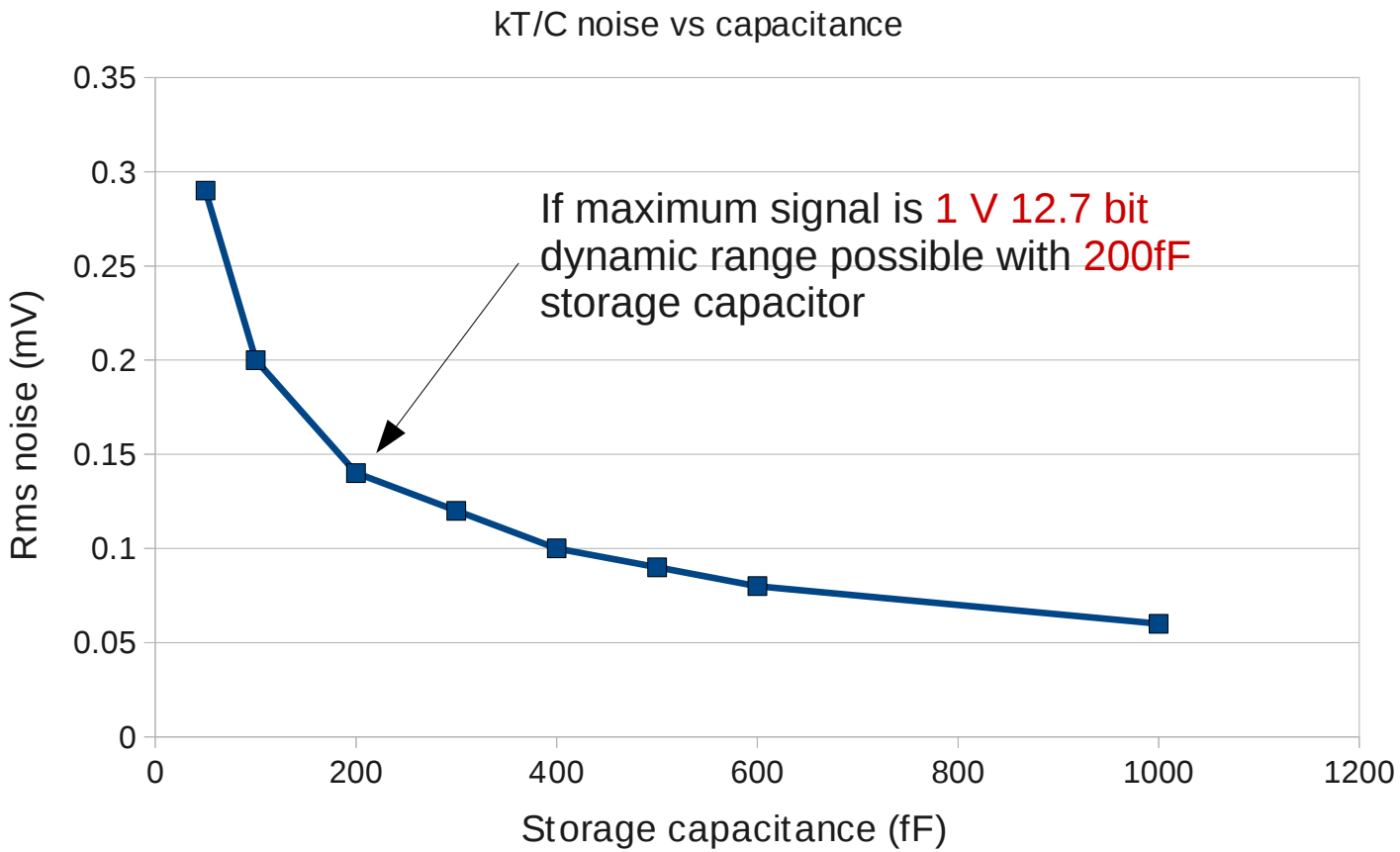




- MOS structures offer high specific capacitance, good for keeping the stored values for long times (but gate leakage might be an issue in very scaled processes).

Which capacitor for high sampling speed (1) ?

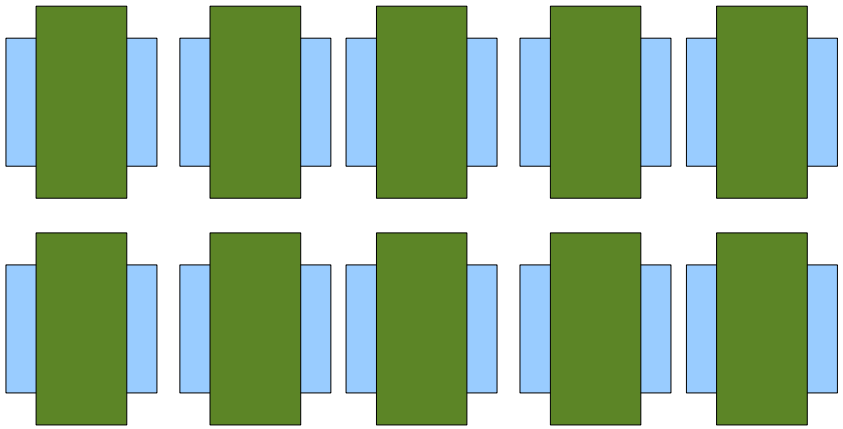
- High input bandwidths require small and fast capacitors.
- What about kT/C noise?

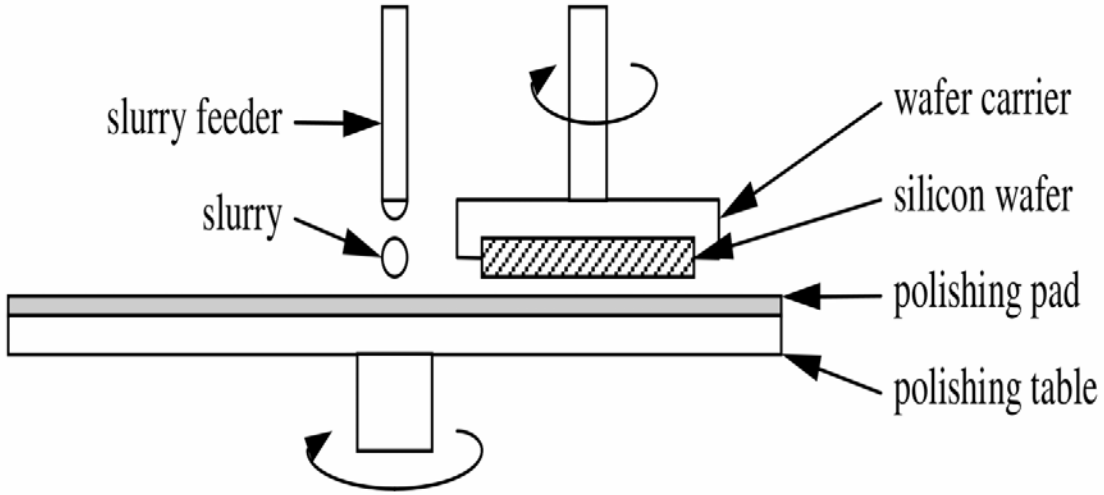


Major concerns in using small capacitors come from leakage and charge injection

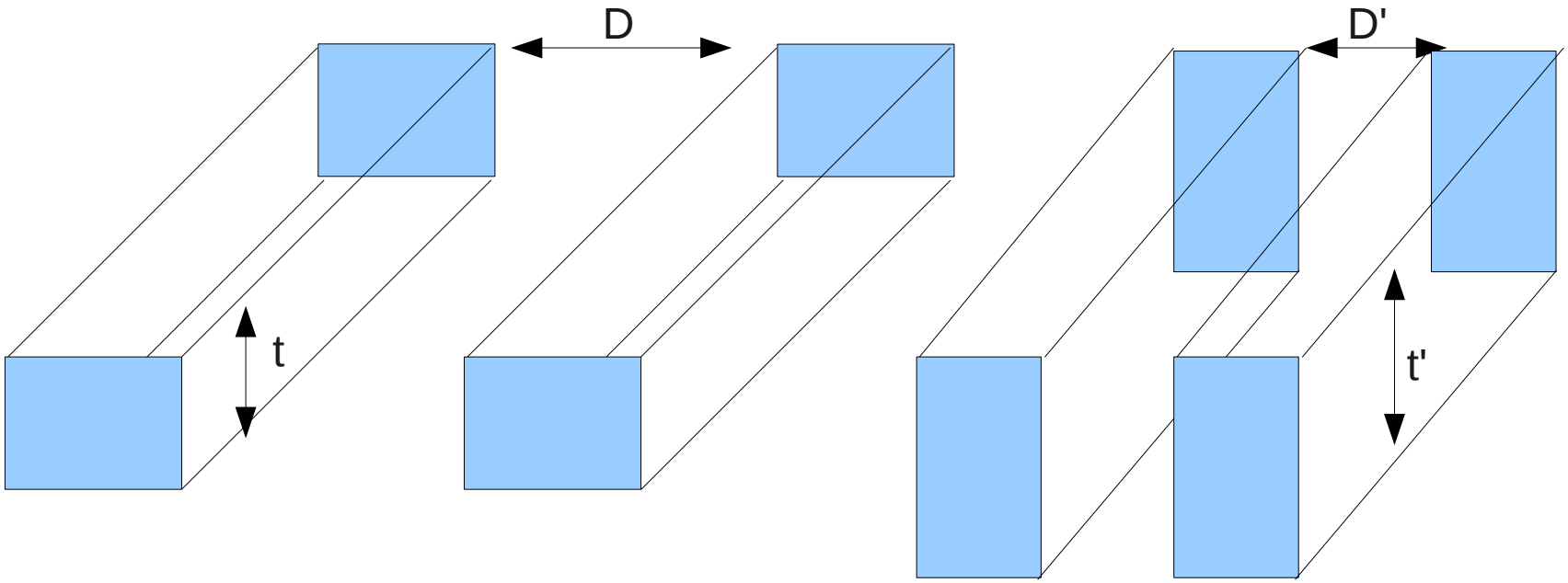
Which capacitor for high sampling speed (2) ?

- In deep sub-micron technologies (from 0.25 µm and beyond) highly linear capacitors are obtained by sandwiching two dedicated metal layers.
- Specific capacitance may range from 0.5 fF/µm^2 to 2 fF/µm^2.
- However, deep sub-micron technologies impose severe pattern density rules for each layer used in chip fabrication (diffusions, poly, metals...)
- To guarantee adequate inter-layer dielectric flatness after chemical-mechanical polishing each pattern should fill the area within a given range.
- This can be a serious issue for front-end chips, which usually implies regular repetition of many channels which tend to overfill selected areas.



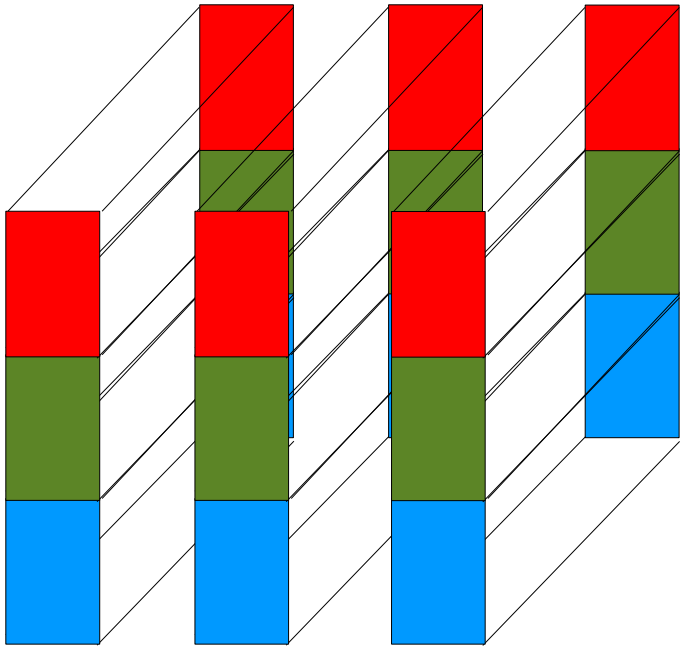


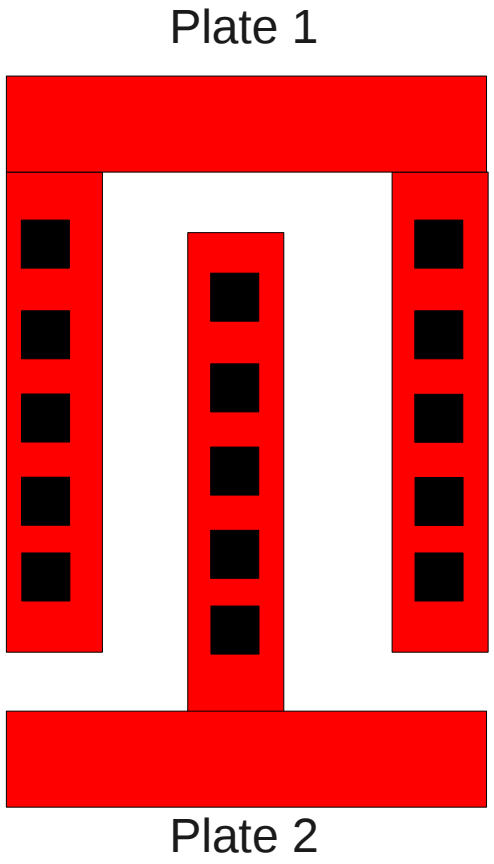
Which capacitor for high sampling speed (3) ?



- Scaling requires also finer pitch interconnects and narrower lines;
- Vertical dimension grows to keep resistance acceptable;
- Vertical capacitance also grows, so RC delays are approximately constant;
- Many metal layers available. Stacking yield reasonable capacitance. (0.5 – 1 fF/μm^2).

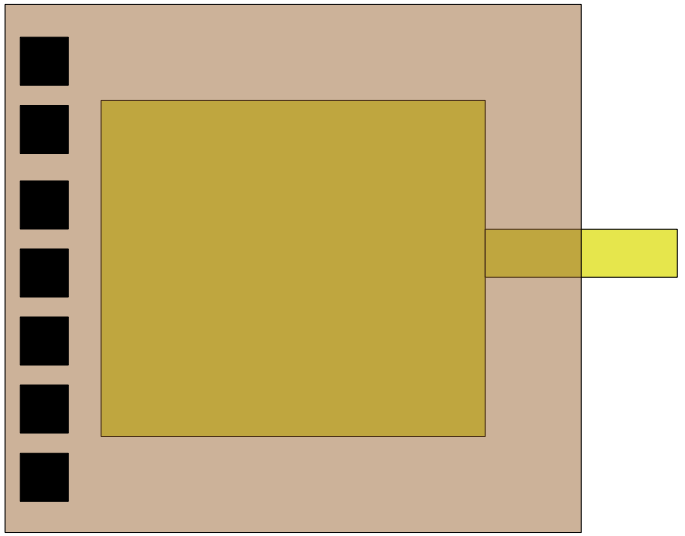
Which capacitor for high sampling speed (4) ?





- Vertical capacitors used native metal, no extra mask required (cost);
- Capacitance density reasonable;
- Metal coverage can be more than 50%;
- There is no a “top” and “bottom” plate: both equally sensitive to parasitic capacitance.

Which capacitor for high sampling speed (5) ?



- Other possibility: “sandwich capacitor”
- Possibility to minimize the parasitic capacitance of one plate;
- As good as the vertical one from the point of view of metal coverage...
- In general, use the one which has been modeled by the foundry (if any!).

“State of the art” high speed waveform digitizers

- A lot of developments on high-speed waveform recorder/digitizer has been made in the framework of High Energy Astrophysics experiments (ICE cube, H.E.S.S, ANTARES, ANITA, AMANDA...)
- Main purpose: capture of fast transient signal from silicon photomultiplies.
- Developments also in the nuclear/particle physic community (MEG experiment at PSI).
- High sampling speed achieved also in non deep-submicron technologies
- However there is a general trend toward 0.25 μm and also 130 nm processes:
- Main motivation for scaling: increase the speed of the analog-to-digital conversion and reduced dead-time.
- In general, high speed waveform digitizers are characterized by:
  - Modest channel number (< 10)
  - Fairly high power consumption (40-150 mW/ch)
  - High dynamic range (12 bits of more)

Some interesting papers

"Waveform Digitization with Programmable Windowed Real-Time Trigger Capability"

- 2 Gs/sec. with 2 GHz bandwidth and on chip ADCs, 0.25 μm CMOS.

W. Huang, S. W. Chiang and S. Kleinfelder, IEEE NSS Conference Record 2009, N13-50

"Design and Performance of the 6GHz Waveform Digitizing Chip DRS4"

- 6 Gs/sec., 40 mW/ch, 850 MHz analog bandwidth, external ADC, 0.25 μm CMOS.

S. Ritt, IEEE NSS Conference Record 2008, N11-8

"The large analog bandwidth recorder and digitizer with ordered readout (LABRADOR) ASIC"

- 3.7 Gs/sec. with 1 GHz bandwidth and on chip ADCs, 0.25 μm CMOS

G. S. Varner et al,m NIMA (583) pp. 447-460.

"A 20 Gs/s sampling ASIC in 130 nm CMOS Technology"

- Target: 20 Gs/sec with on board ADCs.

J. F. Genat et al., TWEPP 2010, Aachen, Germany

online: http://indico.cern.ch/materialDisplay.py?contribId=26&sessionId=15&materialId=slides&confId=83060

Fast sampling: design example (1)

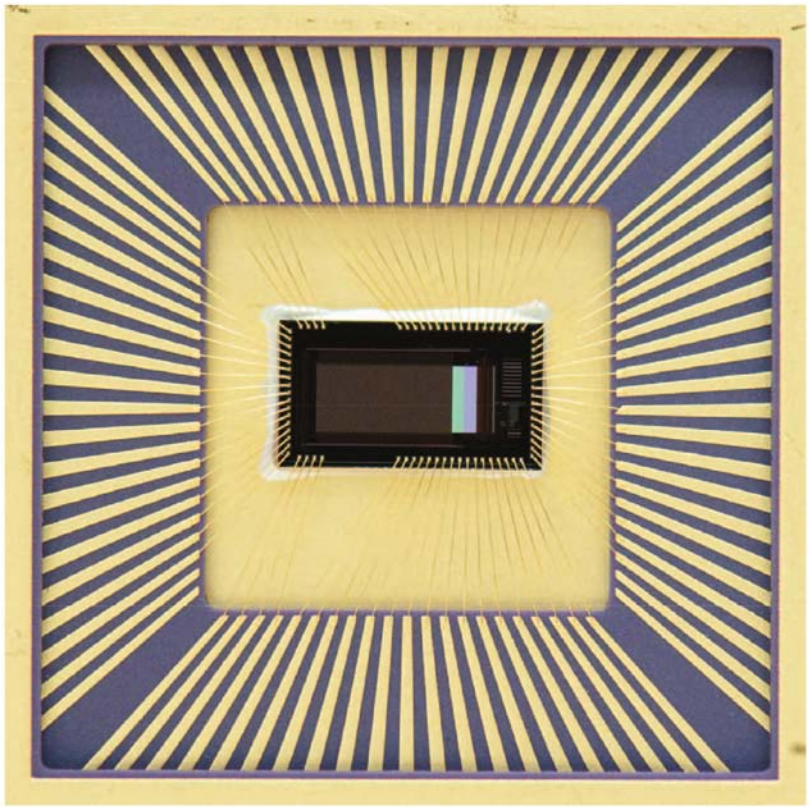
W. Huang, S. W. Chiang and S. Kleinfelder, I

→IEEE NSS Conference Record 2009, N13-50

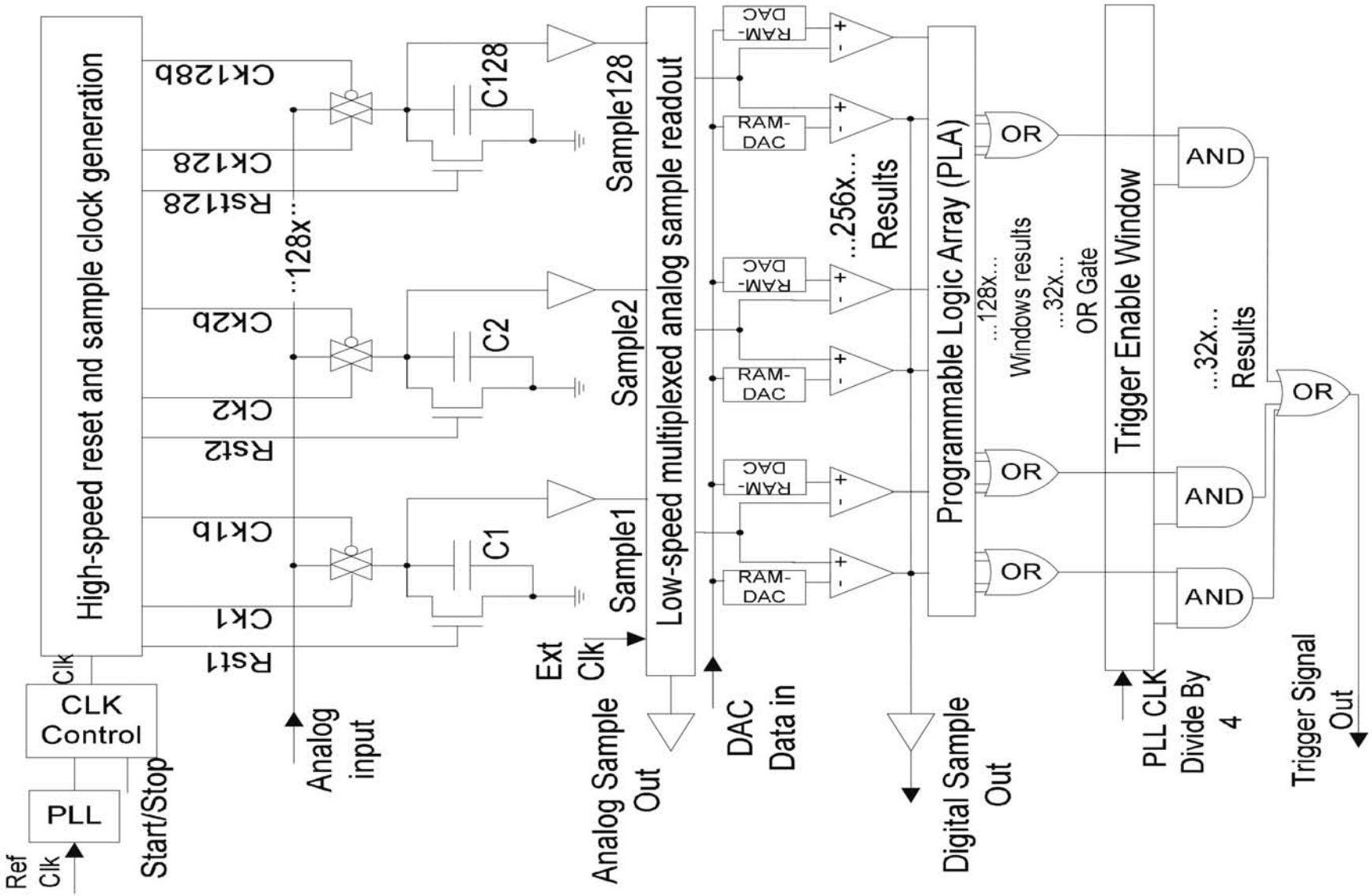
TABLE I. ATWD CHIP PARAMETERS

Parameter	Value
Technology	0.25 um, 5-metal CMOS
Die size	4.9 x 2.7 mm
Prototype package	84-pin LCC (76 active pins)
PLL reference clock frequency	~28 – 33 MHz
PLL output frequency	0.9 – 1.05 GHz
Sample clock rate	1.8 – 2.1 GHz
Phase Noise	< -100 dBc/Hz at 1MHz offset
Number of sample points stored	1 Channel of 128 samples
Storage capacitor -3dB bandwidth	~2.2 GHz at ≤1V , ~1GHz at 1.5V
Input signal range	0.0 – 1.7 V
Comparator gain and bandwidth	60 dB , 100MHz (-3dB)
Trigger decision speed	~7 ns
Fixed pattern noise	12.9 mV, RMS
Temporal noise, all sources	~0.625 mV, RMS

ATWD chip

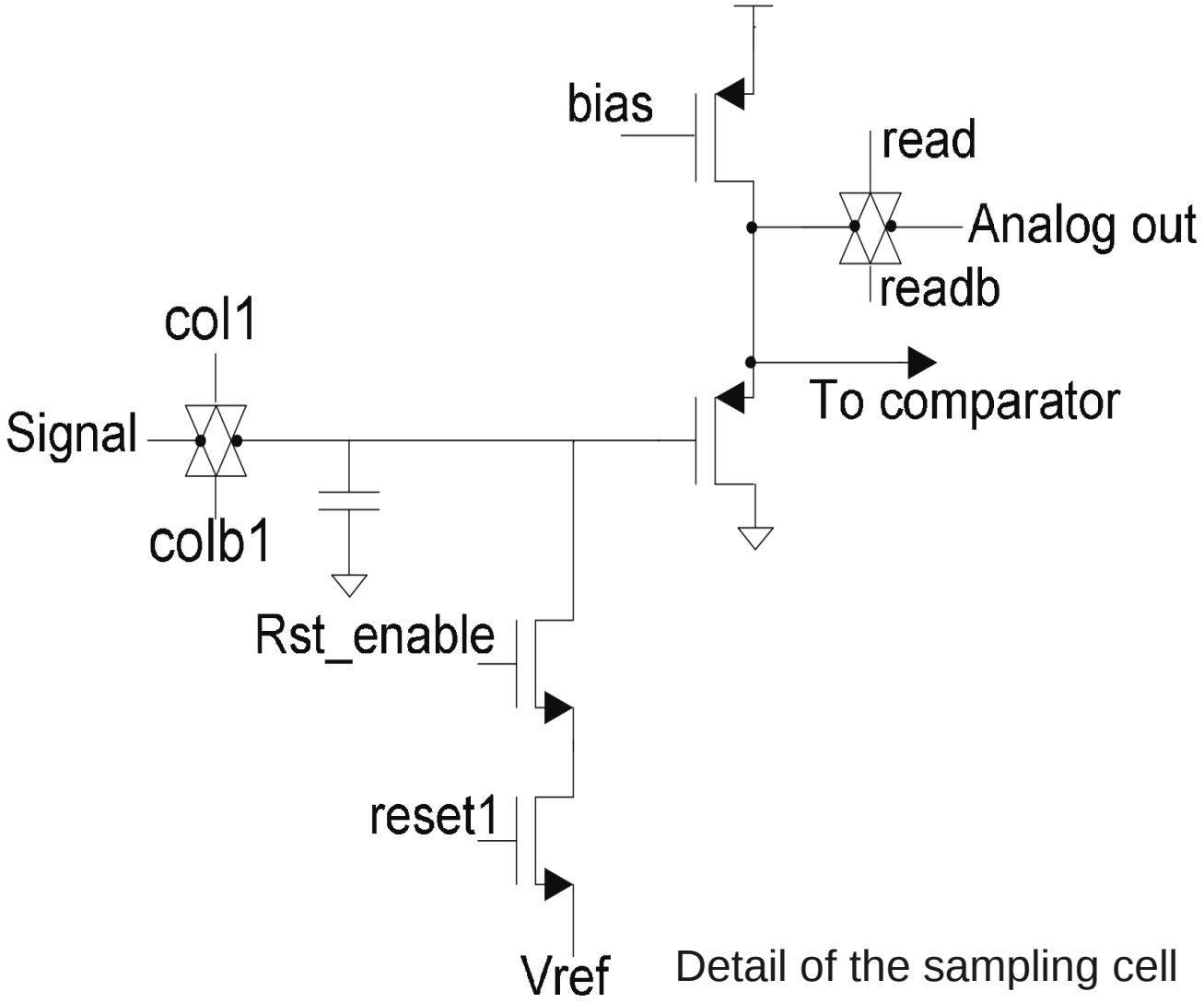


Fast sampling: design example (2)



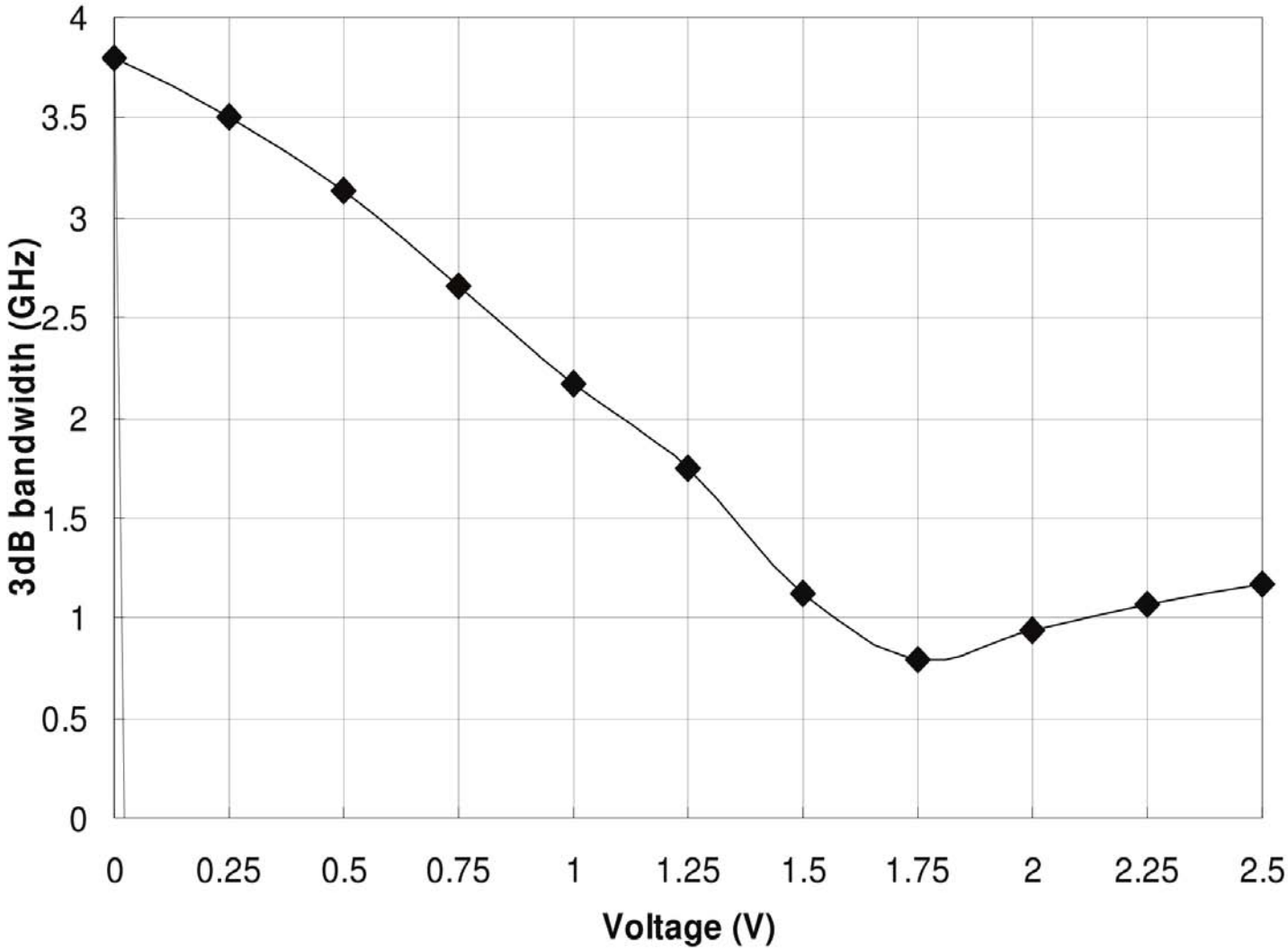
Fast sampling: design example (3)

W. Huang, S. W. Chiang and S. Kleinfelder, IEEE NSS Conference Record 2009, N13-50

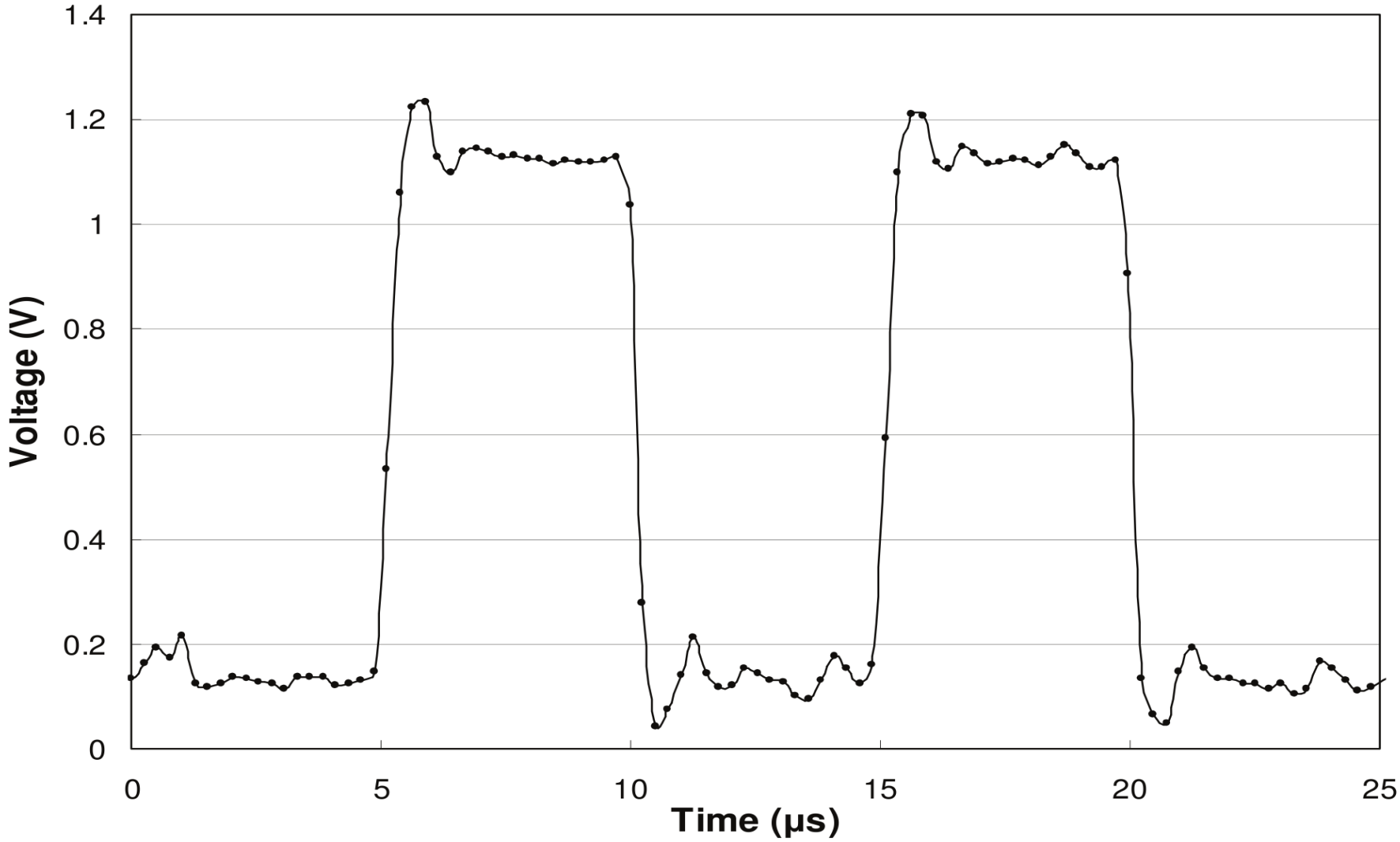


Detail of the sampling cell

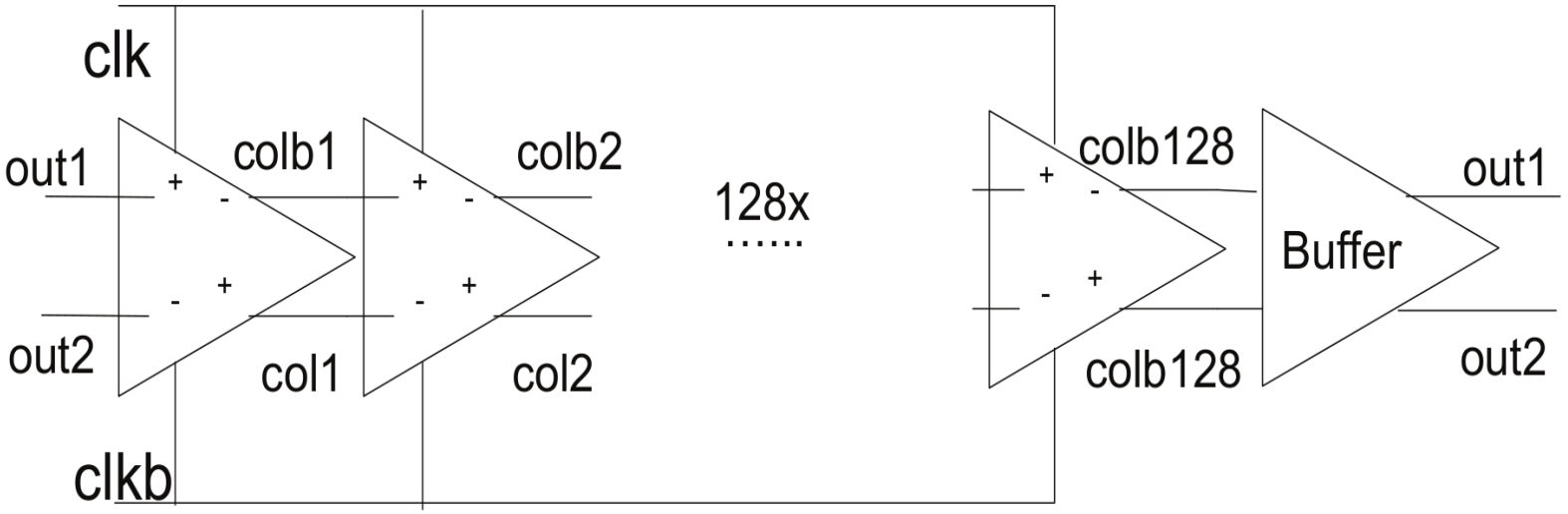
Fast sampling: design example (4)



Fast sampling: design example (4)



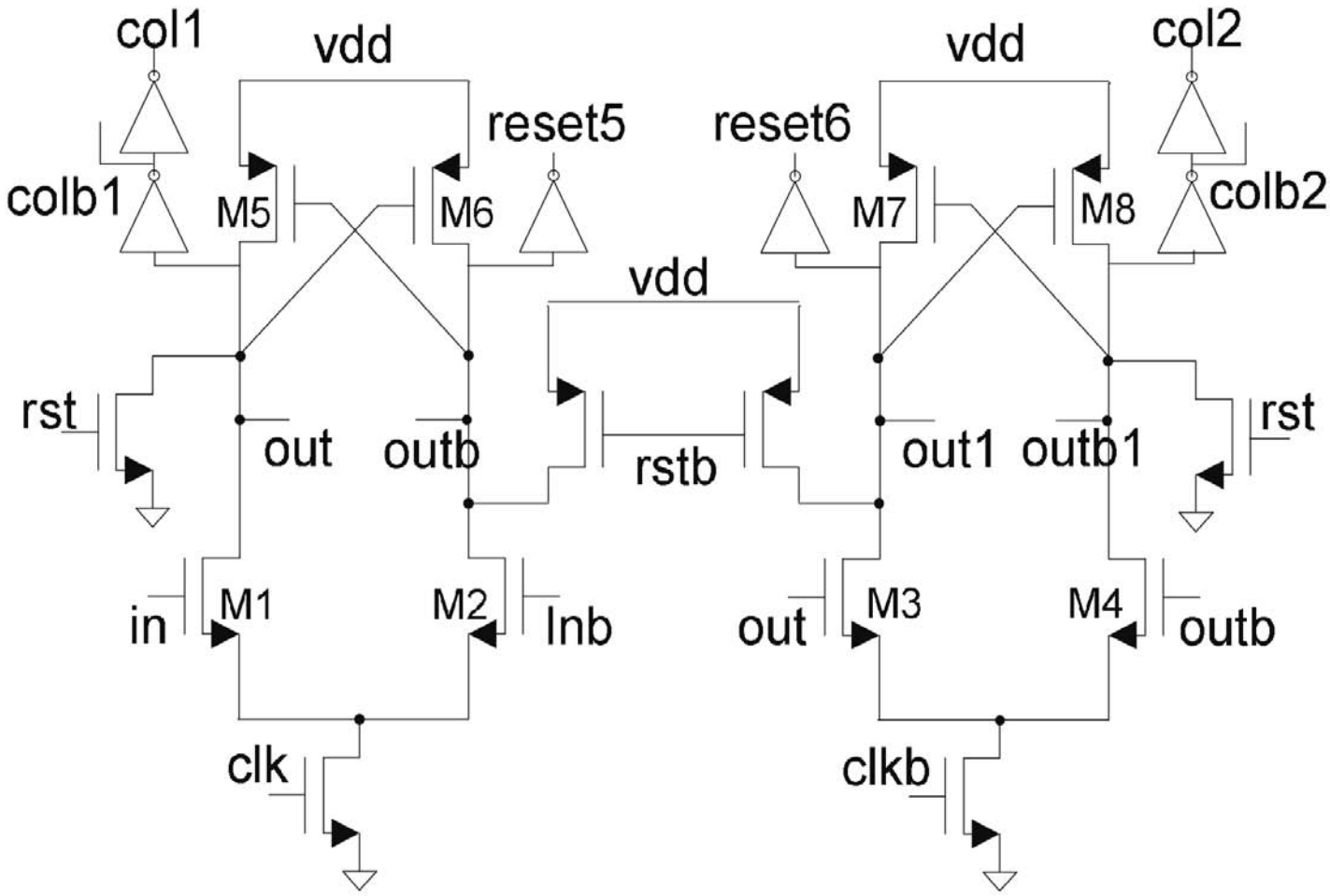
Fast sampling: design example (5)



High speed sampling achieved by:

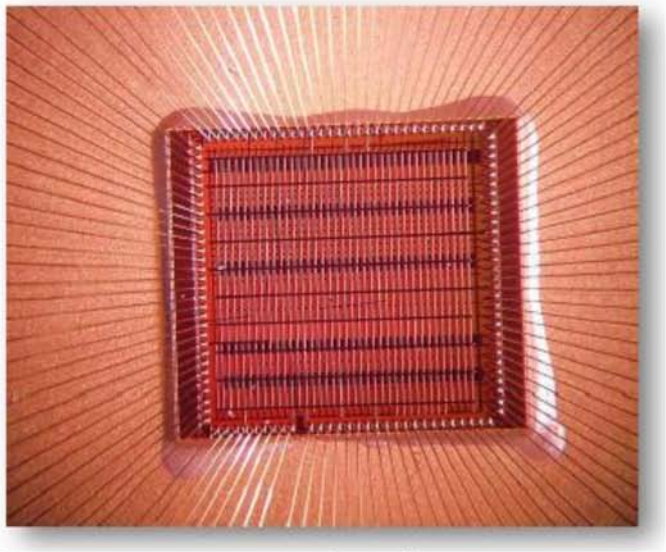
- Multiplying external low clock frequency with an on chip PLL;
- Using a fast shift registers with custom differential master-slave flip-flops;
- Sampling on both clock edges of the high speed clock.

Fast sampling: design example (6)



- High speed differential flip flop for the sampling register.
- Digitization is done on chip with an array of 128 Wilkinson ADC working in parallel.

Waveform Sampler ASIC specs



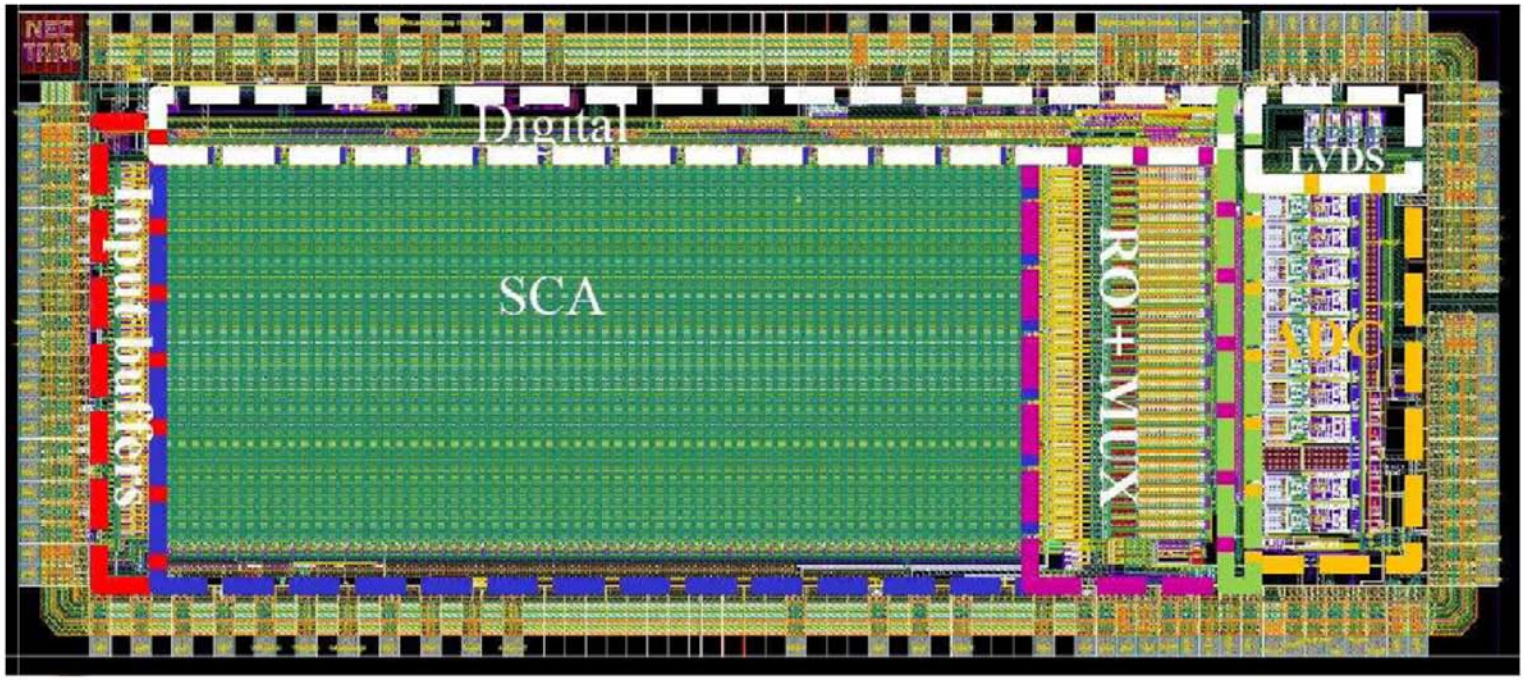
Channels 4 + 1 test
Sampling rate 10-15 GS/s
Analog Bandwidth 1-2GHz
Self and External trigger
Dynamic range 800mV
Sampling window 400ps-800ps (or 8 delay cells)
DLL Timing generator Internal phase comparator and charge pump, external LP filter
DC Input impedance ½ 50Ω internal, ½ external
Conversion clock Adjustable 500MHz 1GHz internal ring oscillator.
Maximum conversion time 8us.
Read clock 40 MHz. Readout time (4-channel) 4 x 256 x 25ns=25.6 µs
Power 40mW/channel
Power supply 1.2V
Process IBM 8RF-DM (130nm CMOS)

New development in 0.35 µm CMOS

NECTAr: New electronics for the Cherenkov Telescope Array

S. Vorobiov [a,*], J. Bolmont [b], P. Corona [b], E. Delagnes [c], F. Feinstein [a], D. Gascón [d], J.-F. Glicenstein [c], C.L. Naumann [b], P. Nayman [b], A. Sanuy [d], F. Toussenel [b], P. Vincent [b]

[a] LPTA, Université Montpellier II & IN2P3/CNRS, Montpellier, France
[b] LPNHE, Université Paris VI & IN2P3/CNRS, Paris, France
[c] IRFU/DSM/CEA, Saclay, Gif-sur-Yvette, France
[d] ICC-UB, Universitat Barcelona, Barcelona, Spain



NECTAr chip specifications

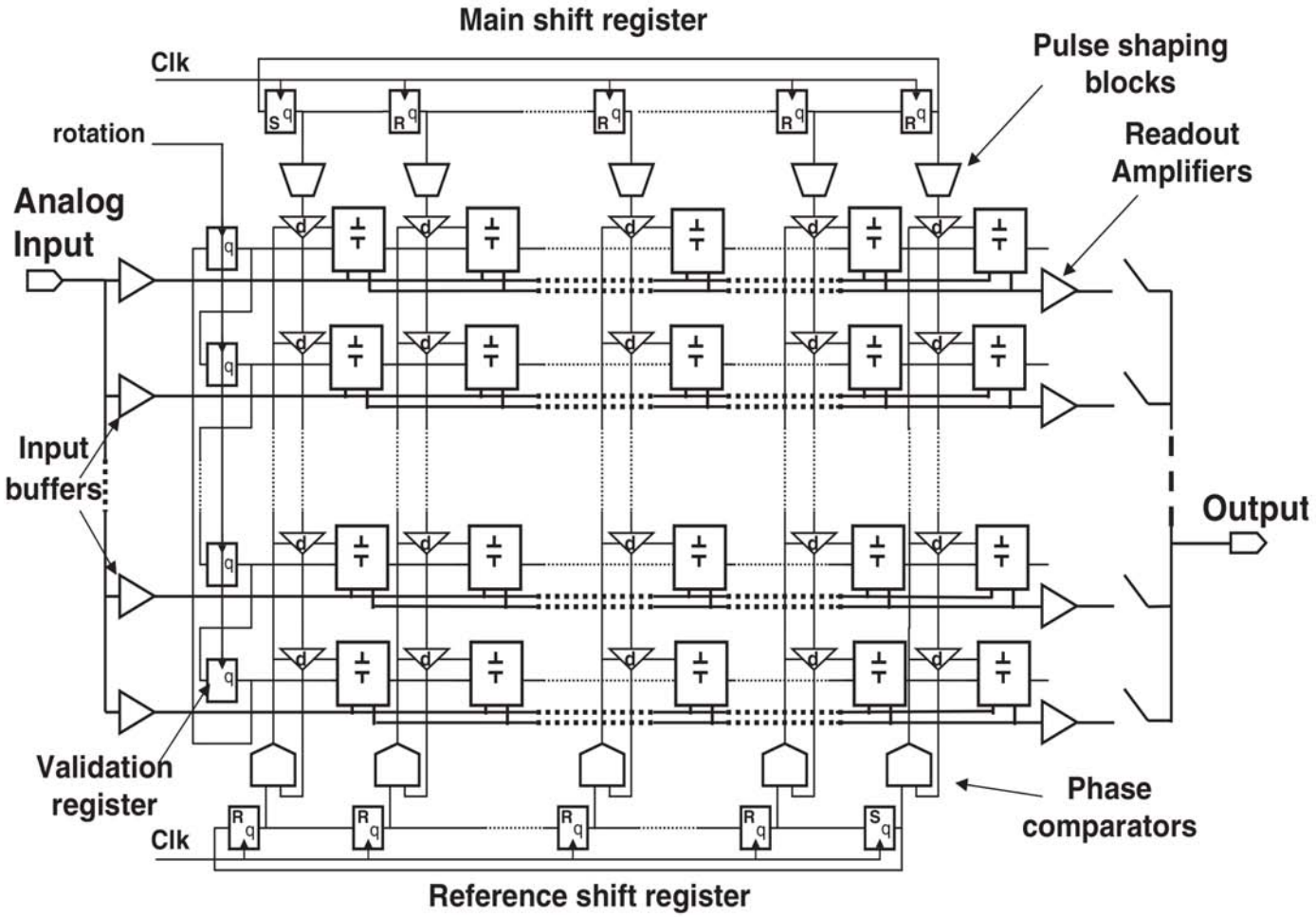
Table 1
Expected NECTAr0 chip performances.

Parameter	Value
Power consumption	300 mW
Maximal signal	2 V
Sampling frequency	0.4–3.2 GHz
Analog bandwidth	0.3–0.5 GHz
Memory depth	1024 samples
Readout freq. (16 samples)	$>$ 800 kHz
Dynamic range	$\sim$ 12 bits
Integral nonlinearity	$<$ 1%
Crosstalk	$<$ 0.3%
Sampling jitter	$<$ 15 ps rms
Number of channels	2 differential ch.
Total noise	0.65 mV rms

High speed digitization is achieved with a shared 12 bit, 25 Ms/sec. ADC.

NECTAr and SAM memory principle

E. Delagnes et al. / Nuclear Instruments and Methods in Physics Research A 567 (2006) 21–26



- Memory cells are arranged in a 16 x 16 matrix
- Samples is 1/fs along the columns and 16/fs along the row.

Timing with high speed waveform samplers (1)

- The full digitization of the signal allows not only the straightforward amplitude measurement, but also timing extraction.
- To achieve very precise time measurement several corrections on the data can be needed.
- However such corrections could be nicely implemented on FPGA.
- Fast waveform sampling does not require TDC.

A nice example:

Nuclear Instruments and Methods in Physics Research A 602 (2009) 438–445

Sub-10 ps monolithic and low-power photodetector readout

L.L. Ruckman, G.S. Varner *

Department of Physics and Astronomy, University of Hawaii, 2505 Correa Road, Honolulu, HI 96822, USA

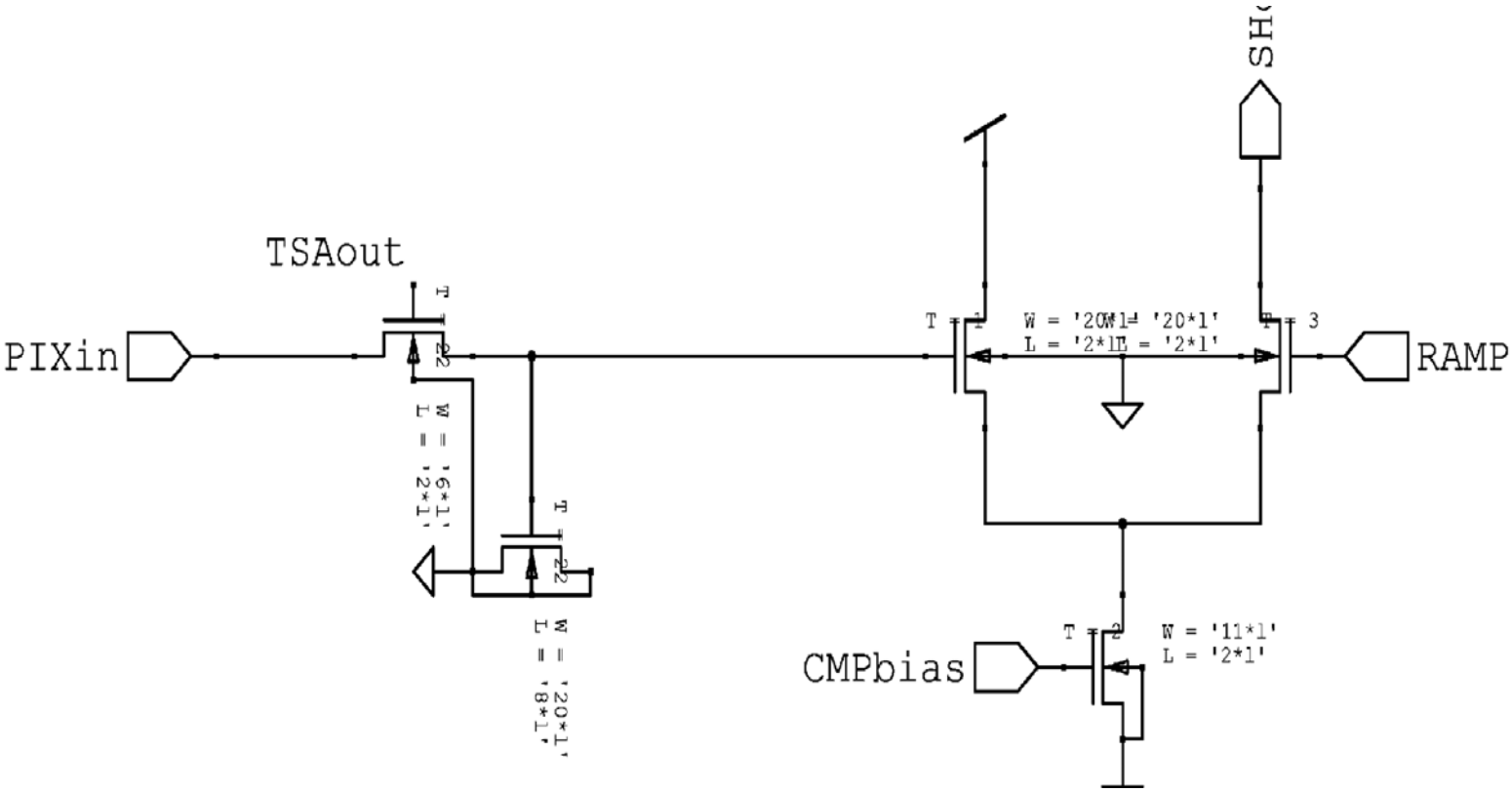
Testing method: split the same signal in two digitizing channels and measure the time difference.

Test done with the BLAB1 (Buffered LABRADOR) chip described in:

Nuclear Instruments and Methods in Physics Research A 591 (2008) 534–545

Timing with high speed waveform samplers (2)

- One of the peculiarity of the BLAB1 chip is its small sampling capacitor (only 14 fF).
- However kT/C noise is still ok! (0.54 mV rms)

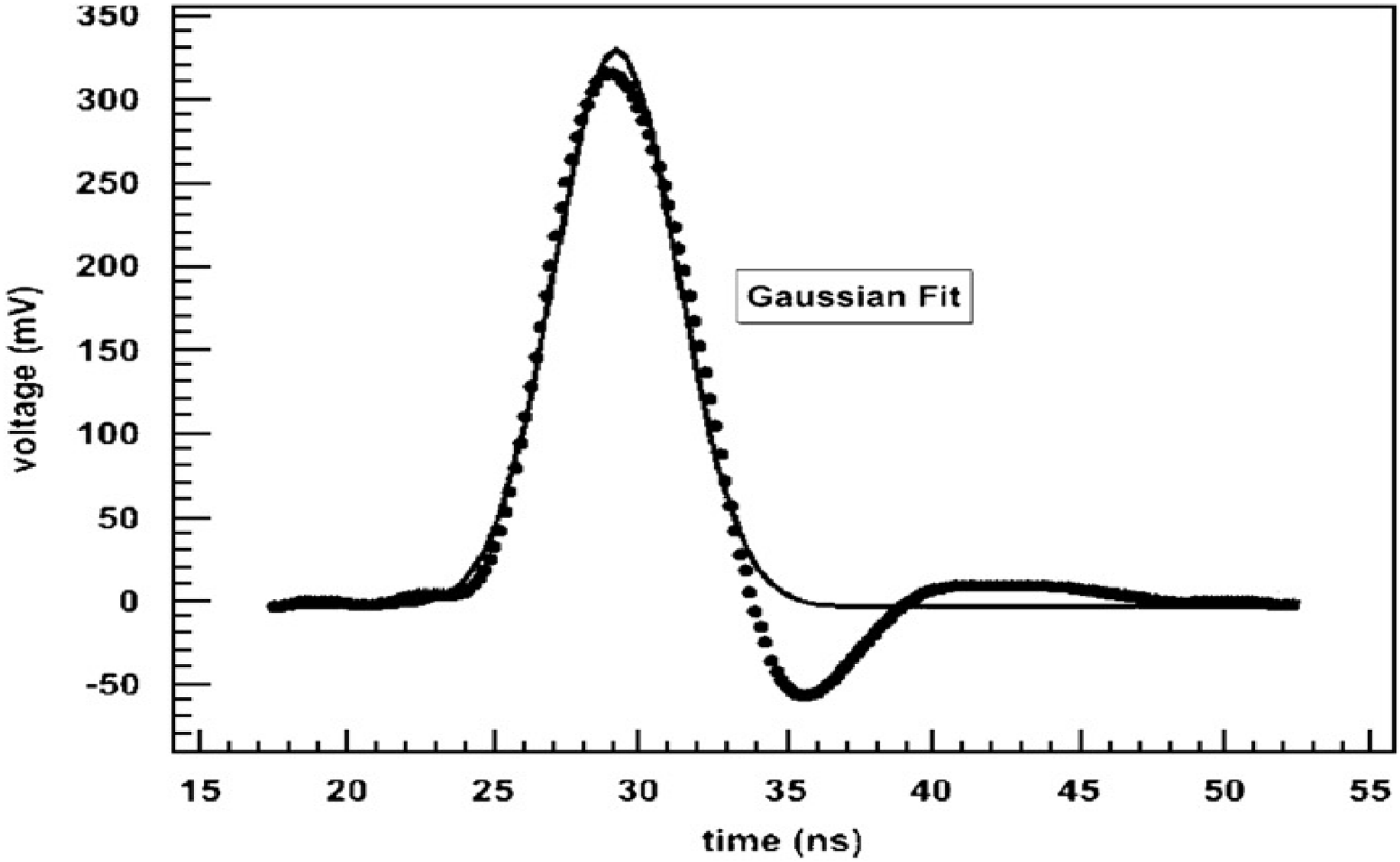


BLAB1 sampling cell

- One comparator per cell
- External capacitor for ramp generation
- External counter for the wilkinson ADC.

Timing with high speed waveform samplers (3)

- Photodector pulse recorde by the ASIC



Timing with high speed waveform samplers (4)

- Raw timing between two channels...Already quite good (76 ps rms)

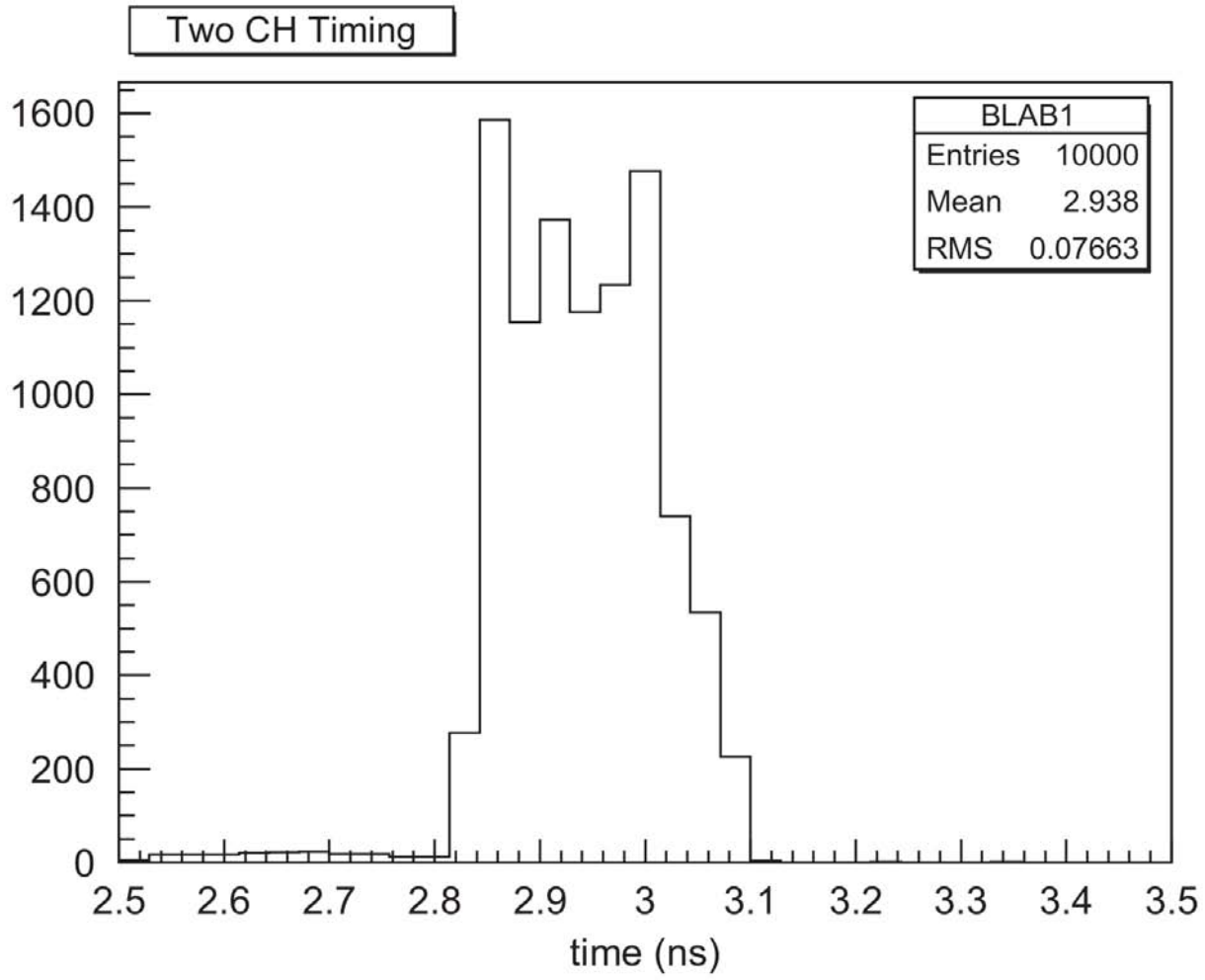
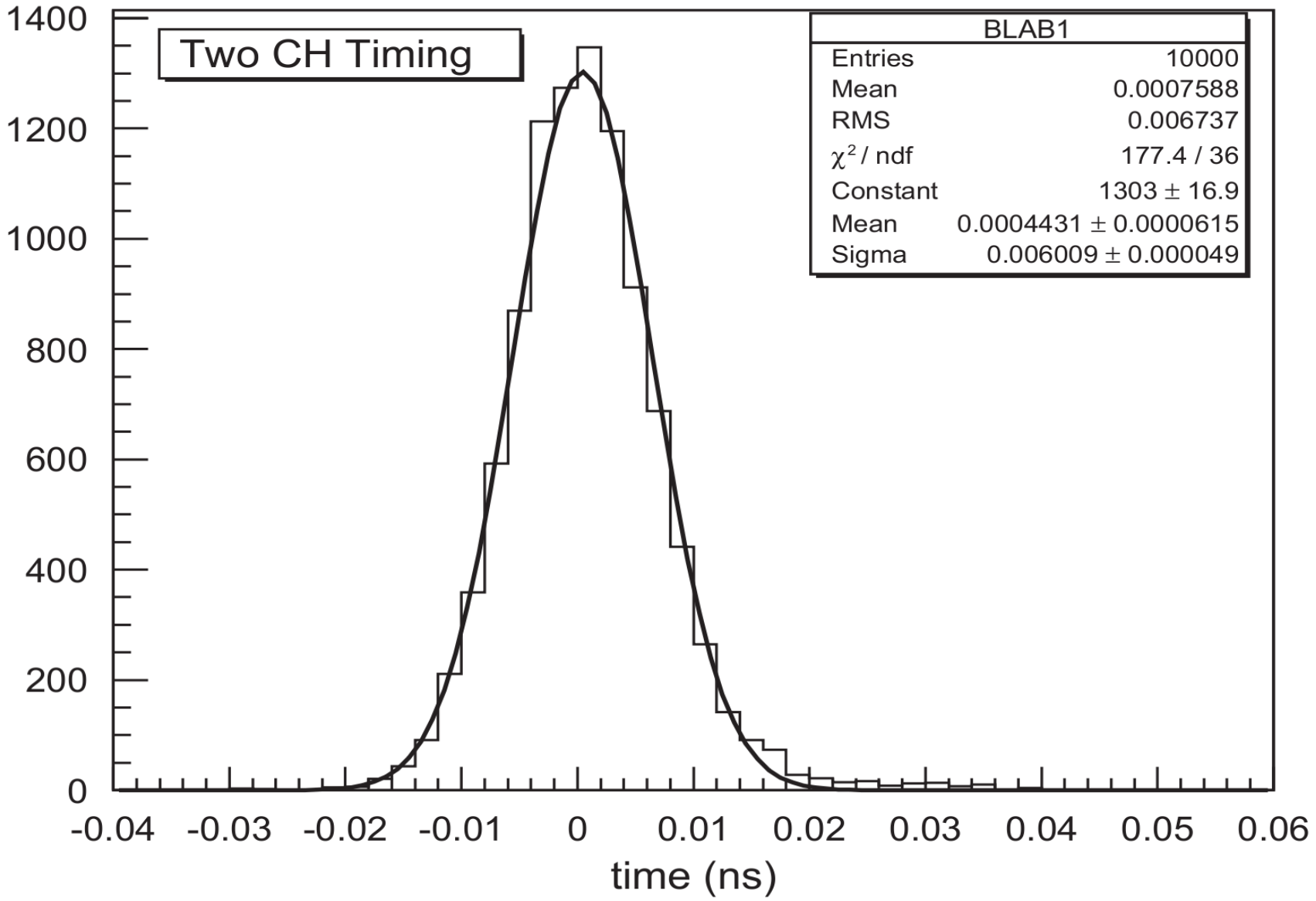


Fig. 13. Raw timing performance after simple timebase correction.

Timing with high speed waveform samplers (5)

- Timing after calibration refinement: 6.7 ps.

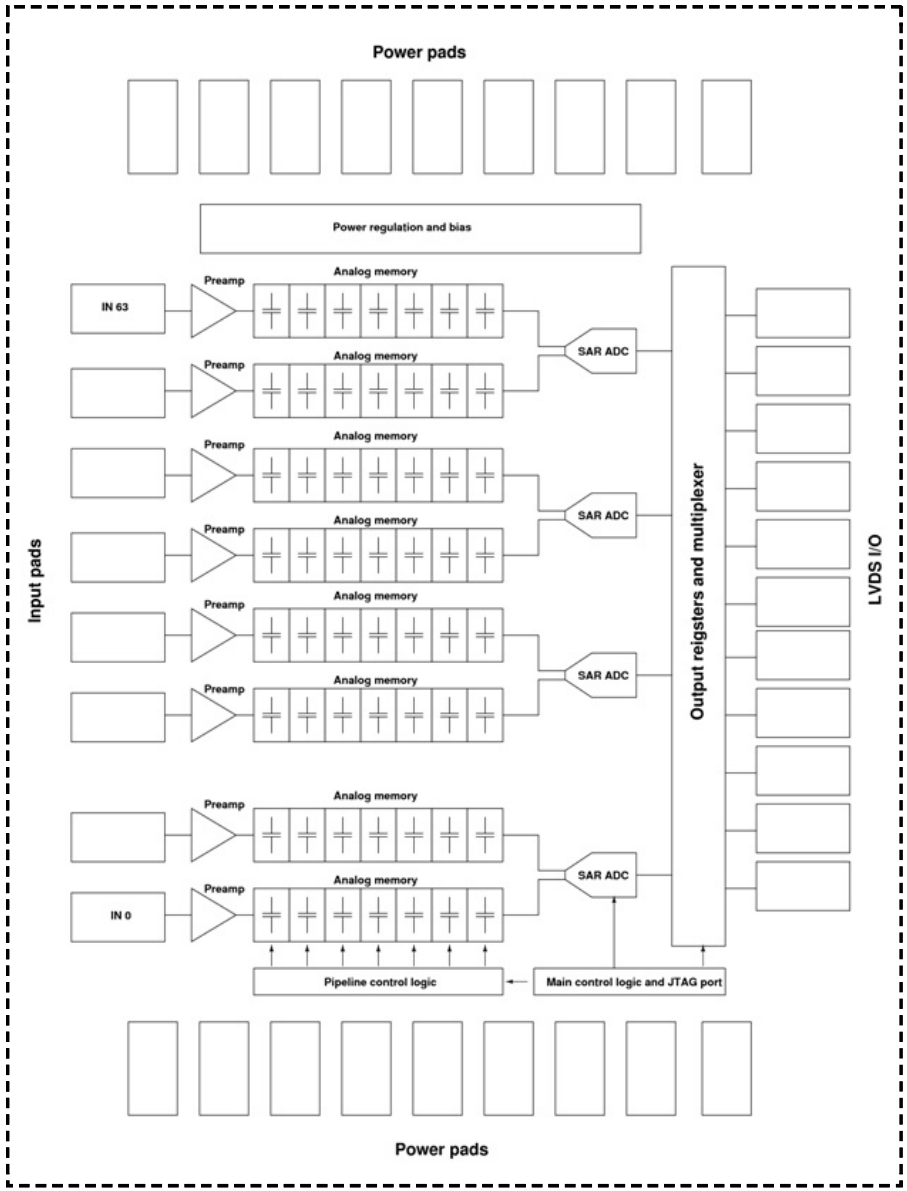


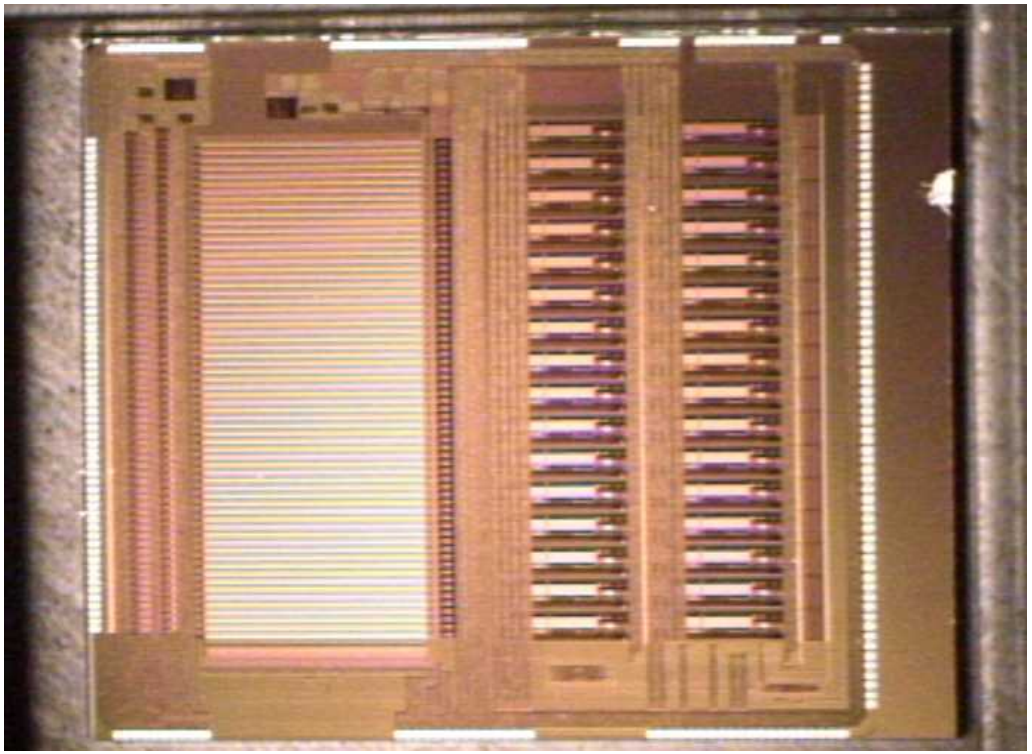
What about ADC?

- Basically, (almost) all the chips seen so far employs Wilkinson ADC for conversion
- However, driven by consumer applications and favored by the evolution of CMOS technology the performance of ADC converter are improving at an impressive speed
- ADC figure of merit: $P/(2^{ENOB} \min(fs, 2ERBW))$, with P=power consumption, fs= sampling frequency, ENOB=effective number of bits.
- State of the art 10 year ago: 9.4 ENOB, 40 Ms/sec, 50 mW, FoM=1.85 pJ/step
- In general not feasible to integrated the ADC after the preamplifier, so analog memories were needed also at relatively low sampling speed (like 40 Ms/sec of the LHC front-ends)

Front-end Electronics for the ALICE SDD

- Preamplifier, Analog Storage and Conversion from Analog to DigitaL (PASCAL)

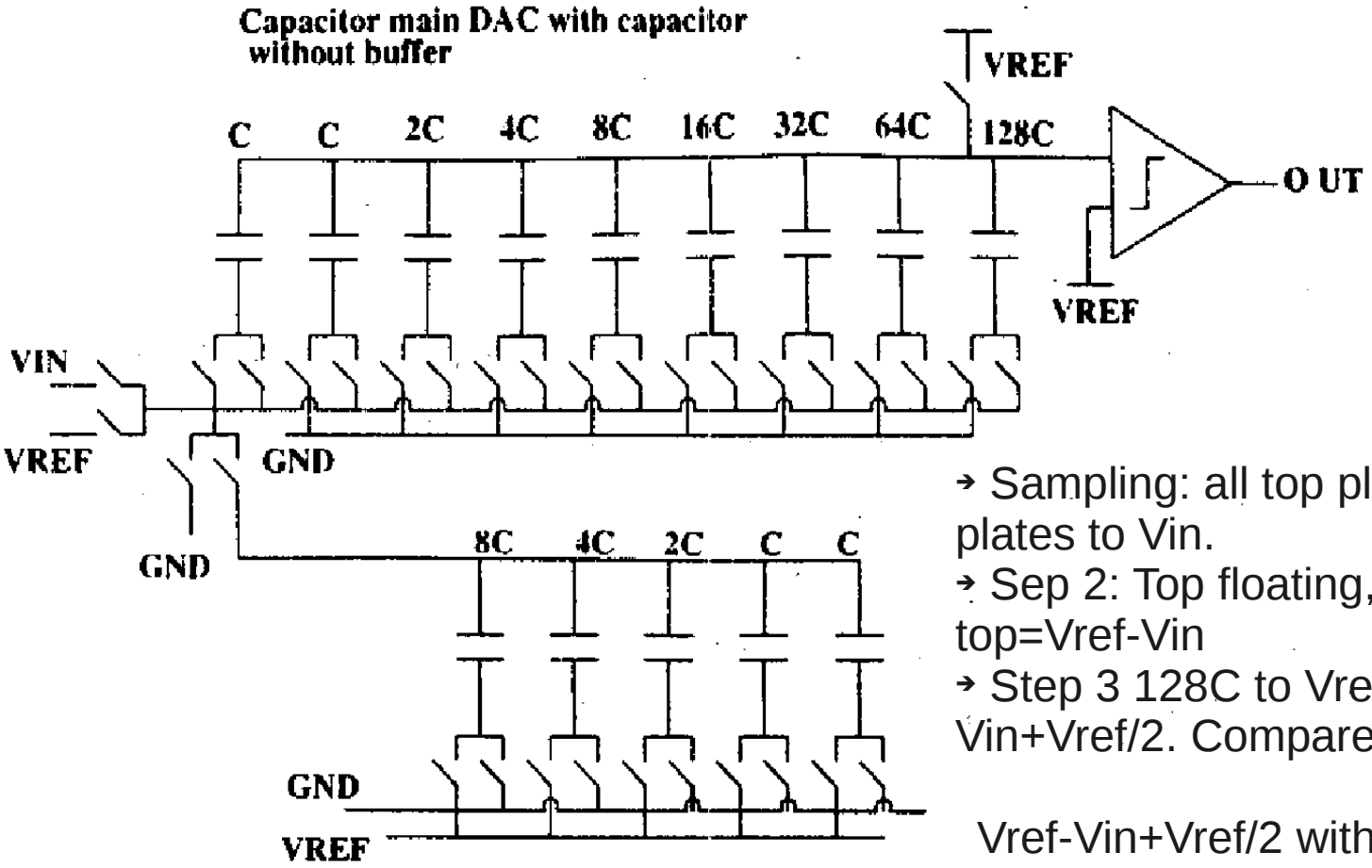




1 cm

CMOS 0.25 µm
Sampling frequency 40 MHz.
Digitization < 1 ms
32 10 bit SAR ADC in two raws

10 years old SAR ADC



- Sampling: all top plates to Vref, all bottom plates to Vin.
- Sep 2: Top floating, bottom to gnd. Voltage on top=Vref-Vin
- Step 3 128C to Vref, voltage on top=Vref-Vin+Vref/2. Compare:

Vref-Vin+Vref/2 with Vref, equivalent to testing: -Vin+Vref/2<0. If yes, swich 64 C to Vref. If no switch 64C to Vref and return 128C to GND, and so on...

40 MHz clock
10 clock cycles for conversion + 2 for sampling
9.1 ENOB at 3.2 Ms/sec, 3 mW, 1.85 pJ/step

State of the art ADC

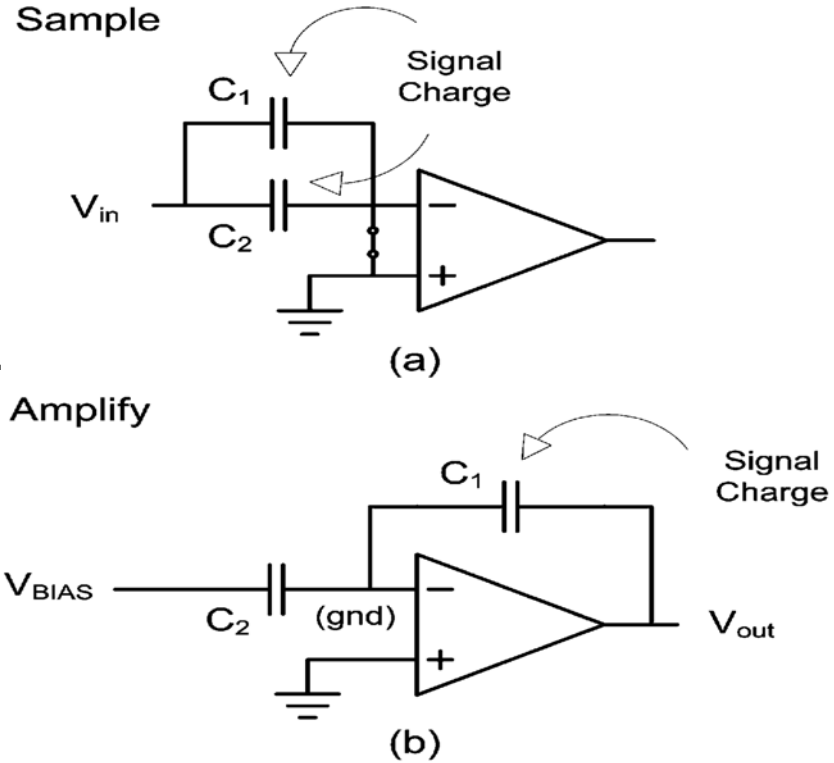
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 4, APRIL 2009 1057

A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Source Follower Residue Amplification

Jason Hu, Noam Dolev, and Boris Murmann, *Member, IEEE*

N stage in cascade.
First stage: compare Vin to Vref
If Vin>Vref, Vout=2(Vin-Vref) Bit=1
If Vin<Vref, Vout=2Vin, Bit=0
Then second stage takes over...

Unfortunately not as simple to implement in practice...
Key point: op-amp used in 2X multiplications require power.



State of the art ADC (2)

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 4, APRIL 2009 1057

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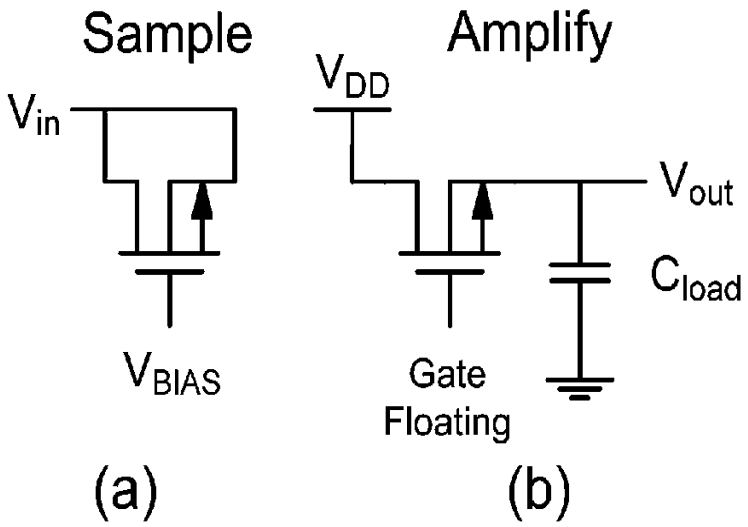
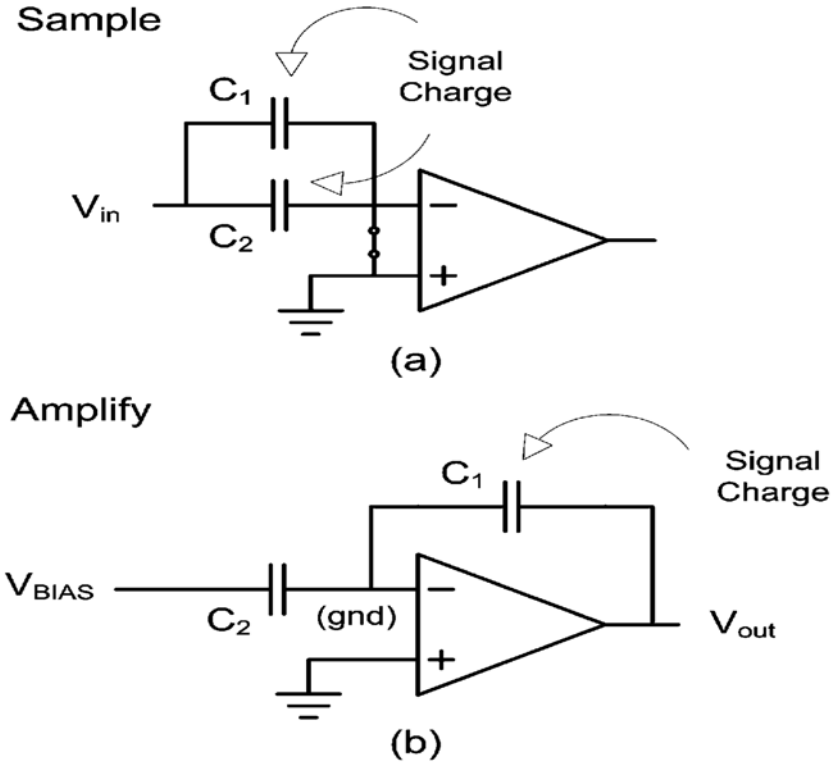
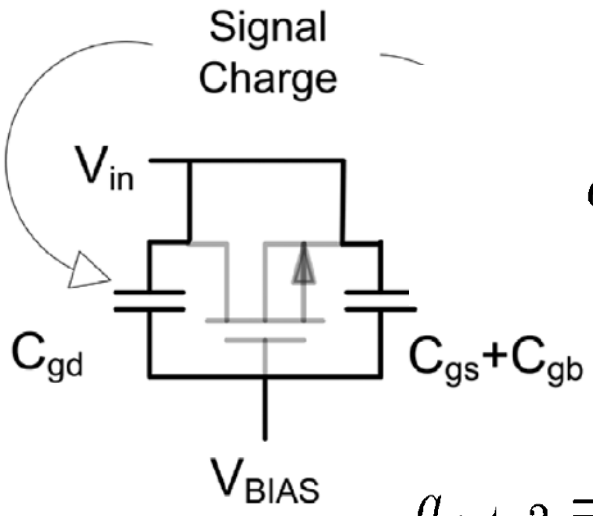




How to replace an op-amp....
FoM 115 fJ/step, 90 nm CMOS

State of the art ADC (3)

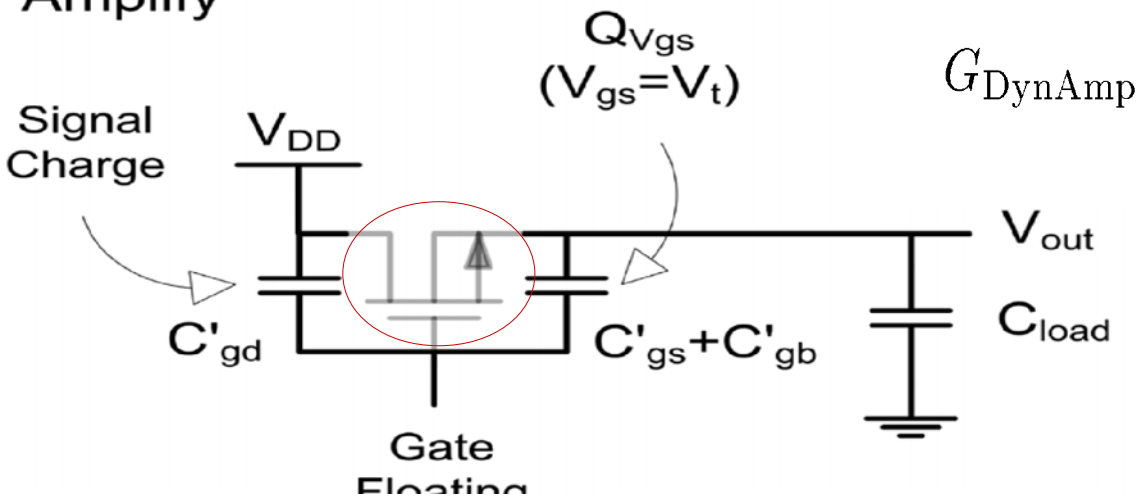
Sample



$$q_{\mathrm{gate1}} = -(C_{\mathrm{gs}} + C_{\mathrm{gd}} + C_{\mathrm{gb}})v_{\mathrm{in}}$$

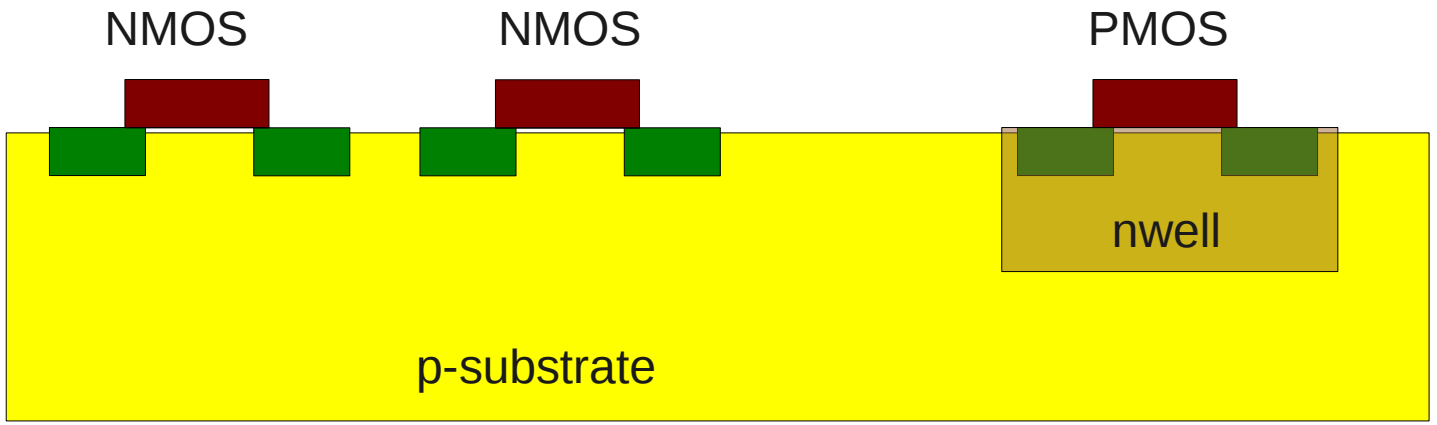
$$q_{\mathrm{gate2}} = C'_{\mathrm{gd}}v_{\mathrm{gd}} = C'_{\mathrm{gd}}v_{\mathrm{g}} = C'_{\mathrm{gd}}(v_{\mathrm{out}} + v_{\mathrm{gs}}) \cong C'_{\mathrm{gd}}v_{\mathrm{out}}$$

Amplify

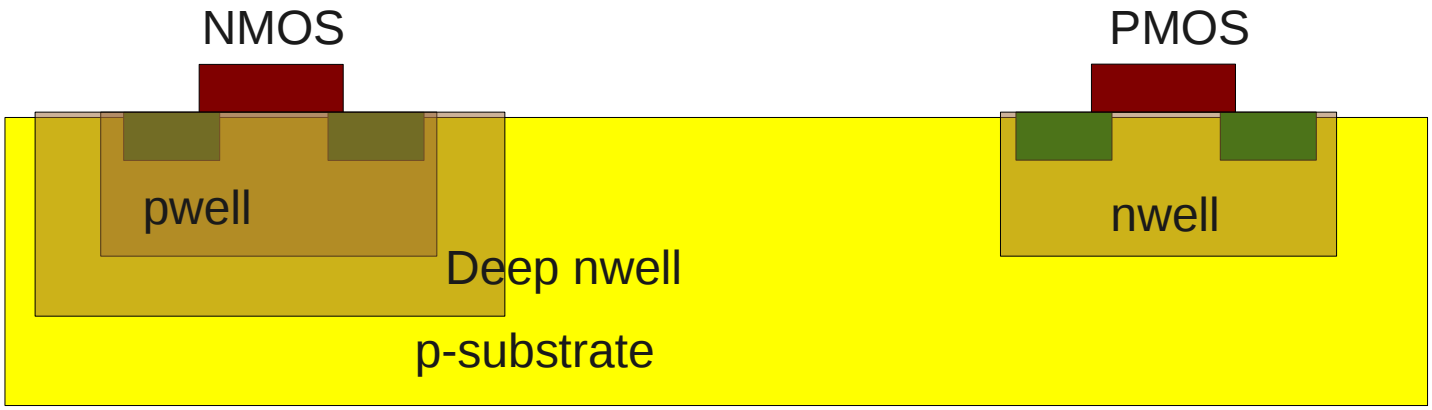


$$G_{\mathrm{DynAmp}} = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} \cong -\frac{C_{\mathrm{gs}} + C_{\mathrm{gd}} + C_{\mathrm{gb}}}{C'_{\mathrm{gd}}}$$

Another feature of DST



Standard nwell process



Triple well possible in very deep submicron processes (0.13 μm and beyond)

First day summary

- Very exciting developments have been done and are in progress in the field of fast waveform digitizers for application in detector read-out;
- At the same time impressive progresses are achieved both in industry an academia in the field of fast an low power ADC;
- Very fast front-end electronics can greatly benefits from deep submicron technology: benefit in increase of sampling frequency and even geater with the decrease of conversion time (and hence dead-time) due to the use of novel fast ADCs;
- With ADC achieving 40-50 Ms/sec and few mW, analog memory are on the other hand being phased-out from medium speed application (50-100 Ms/sec...);
- But: very deep submicron technologies are expensive and ADC design in a very complex business!

FAST FRONT-END ELECTRONICS

Angelo Rivetti – INFN Sezione di Torino

PARTII: Low Power Circuits for High Data Rates

General considerations

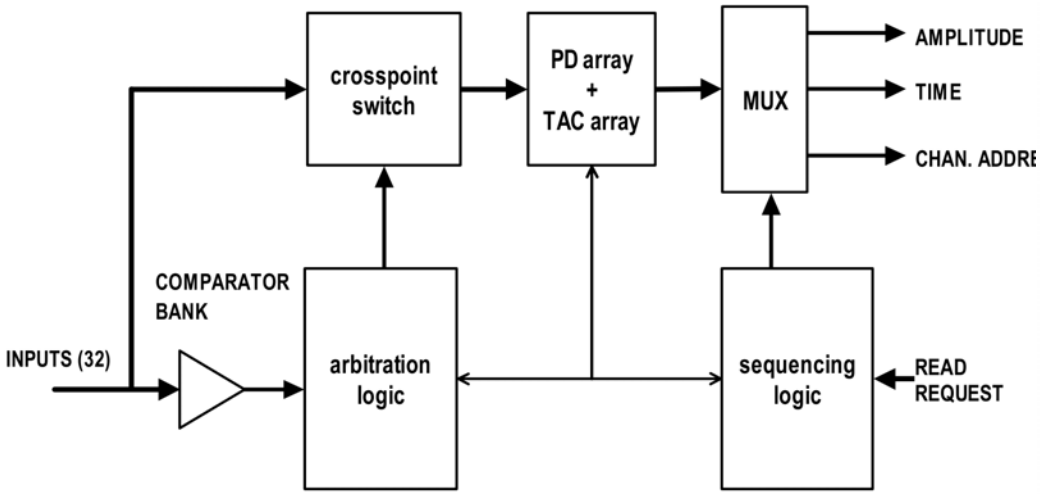
- When the data rate per channel is high (>100 kHz) full waveform sampling and digitization may become impractical.
- Alternative: transfer the minimum of information by pre-processing in the analogue domain;
- Amplitude extraction with peak detectors;
- Timing extraction with TDC.
- Pure binary systems.

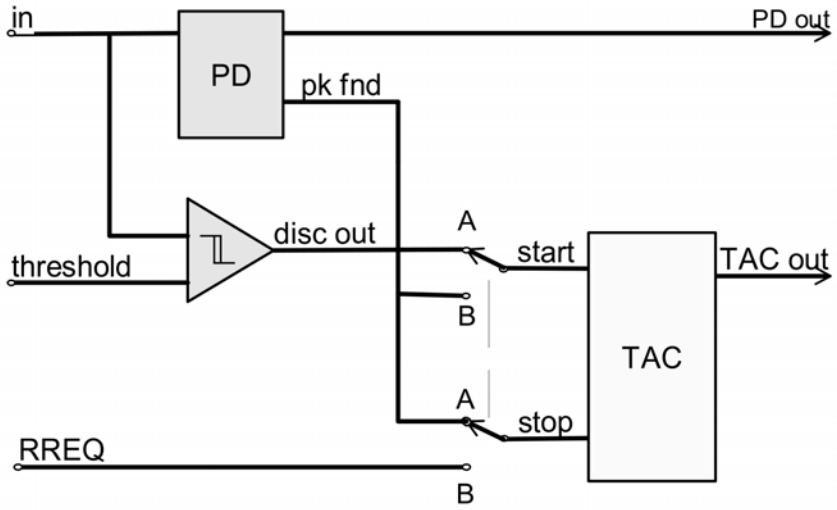
Amplitude and Time Measurements

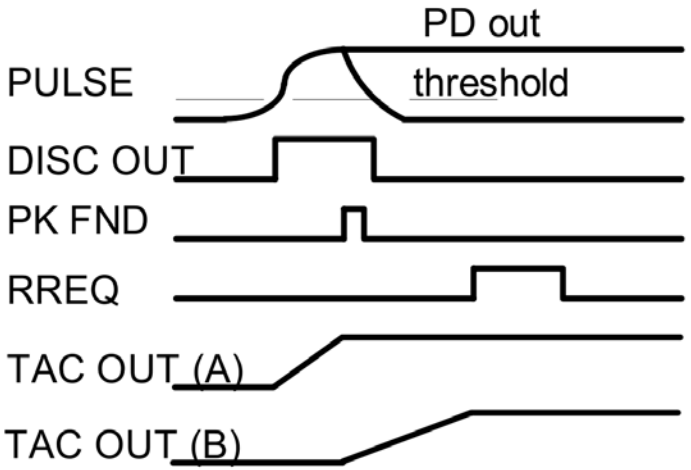
Amplitude and Time Measurement ASIC with Analog Derandomization

G. De Geronimo, P. O'Connor, A. Kandasamy

IEEE NSS-MIC 2002 Conference record

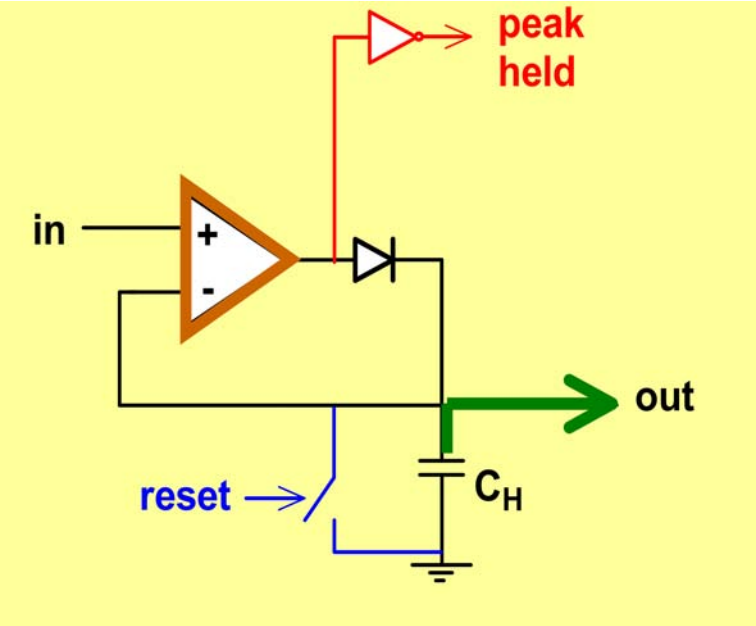


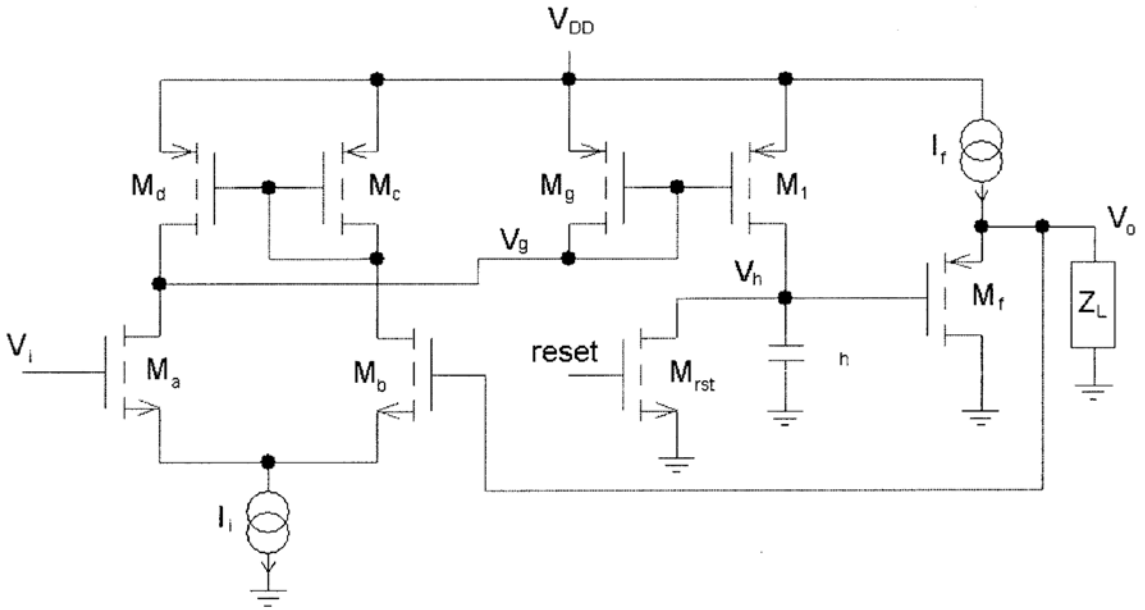




- The arbitration logic route the analog signal to one of the 8 analog processing units.
- Each processing unit consists of a Peak Detector, a main TAC used for timing and a secondary TAC used to set a time-out for the PD.
- The analog outputs of the PD and TAC are mutliplexed on one output and digitized by an external ADC.
- Max rate: 1.6 MHz with 2.2 mW/ch.

Peak detector architectures (1)



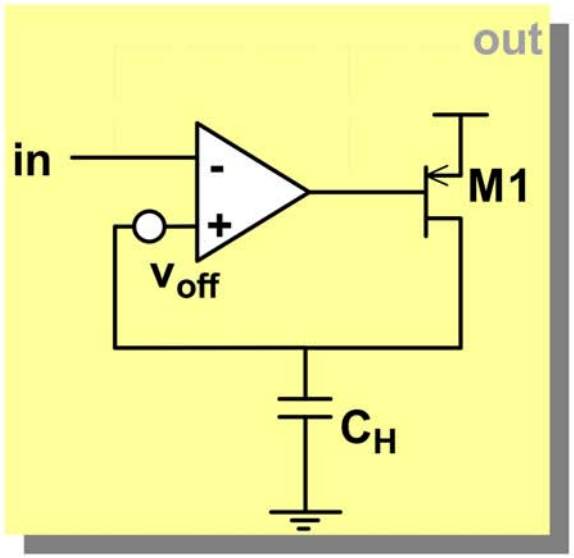


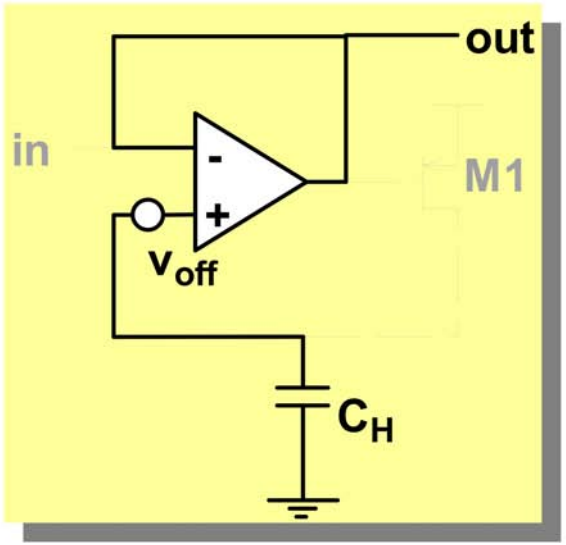
- Principle: introduce a unidirectional element in the feed-back loop of an opamp.
- The voltage on Ch follows the input till to the peak and then stays constant.

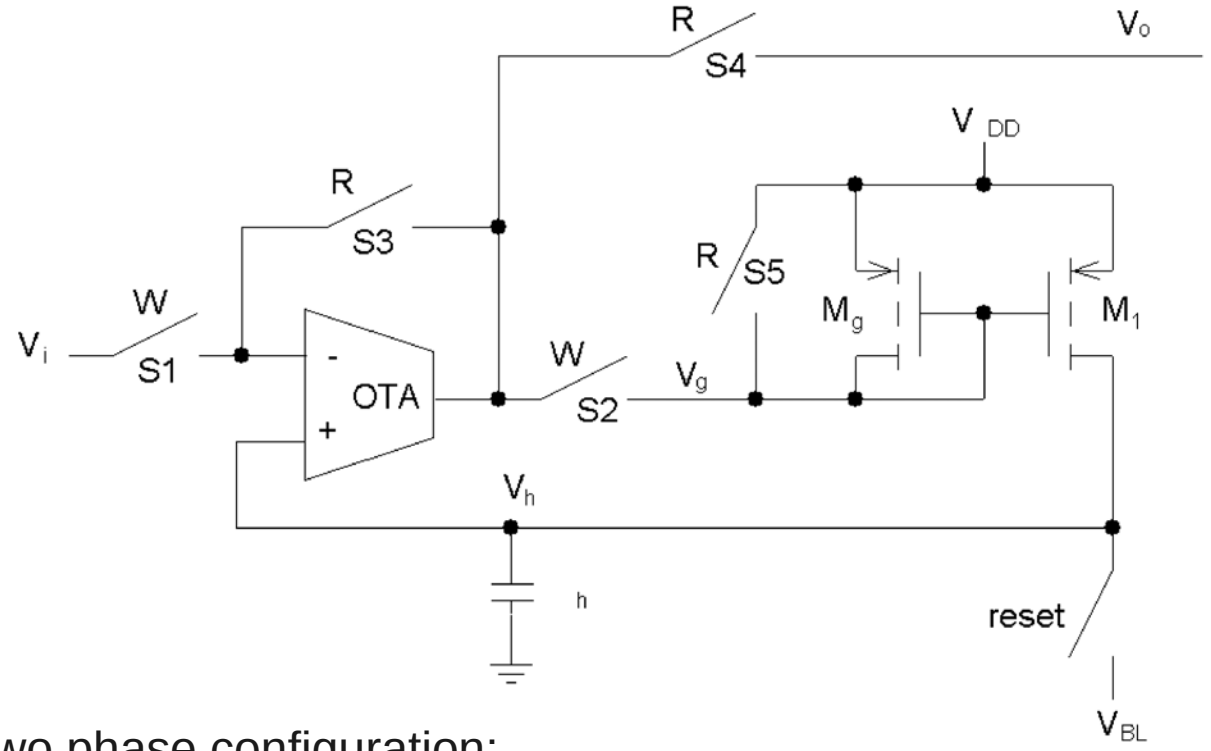
- Single phase peak detector in CMOS

→ Simpler
→ Suffers from op-amp errors

Peak detector architectures (2)







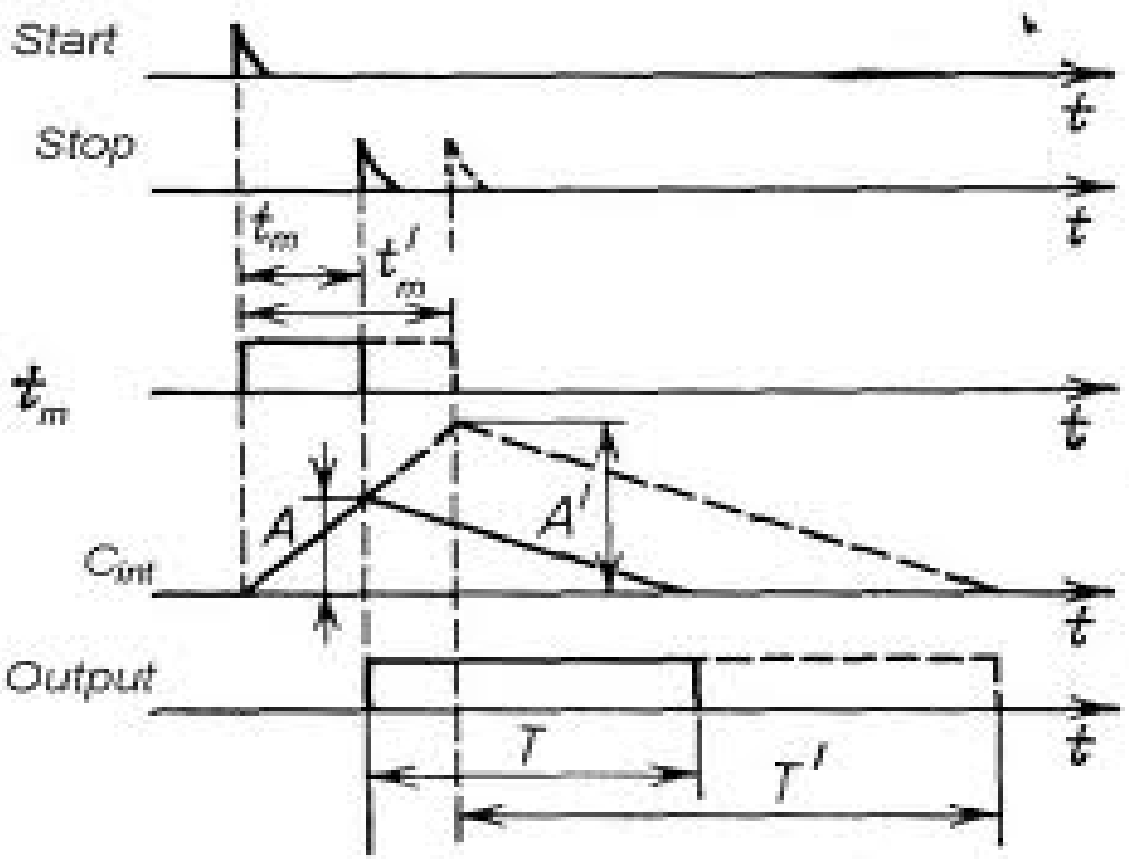
- Two phase configuration:
- ➔ Write phase=conventional peak detectors:
- ➔ Read phase=op-amp used as buffer. Op amp errors cancel

G. De Geronimo, P. O'Connor, A. Kandasamy:

"Analog CMOS peak detect and hold circuits. Part I. Analysis of the classical configuration"

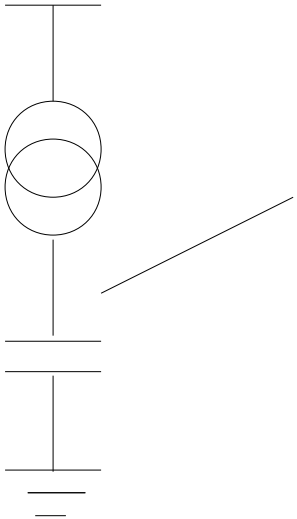
"Analog CMOS peak detect and hold circuits. Part II. The two phase offset free and derandomizing configuration".

Time to Amplitude Converters

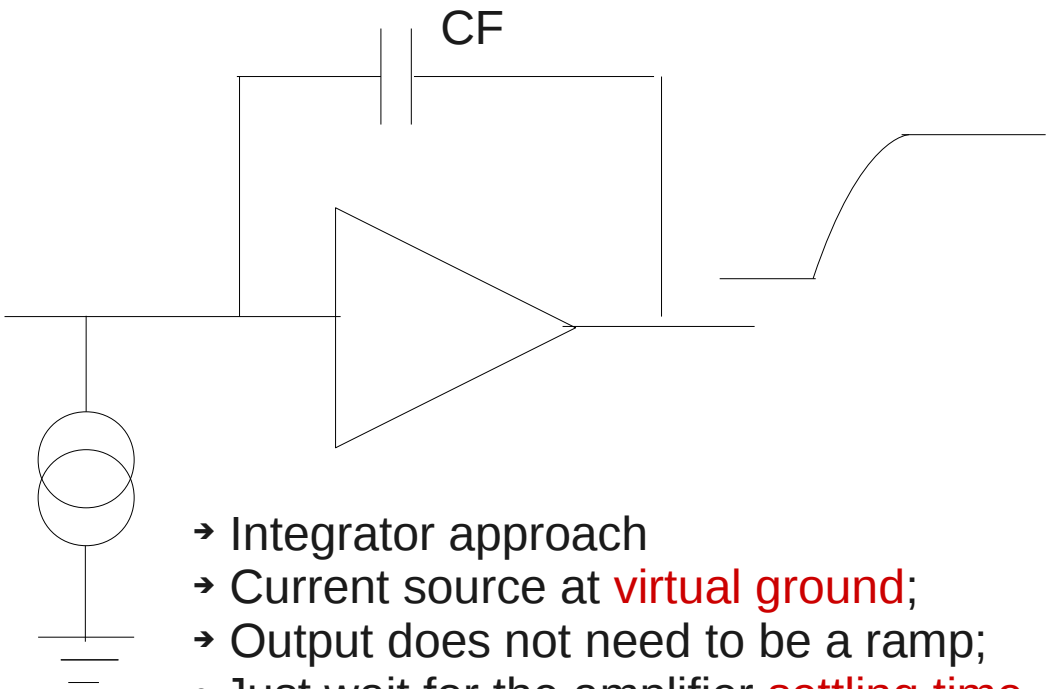


- Principle: charge a capacitor with a constant current source.
- The resulting voltage is proportional to the time difference between the start and the stop pulse.
- Quite an old technique, but still in use, expecially for high resolution...

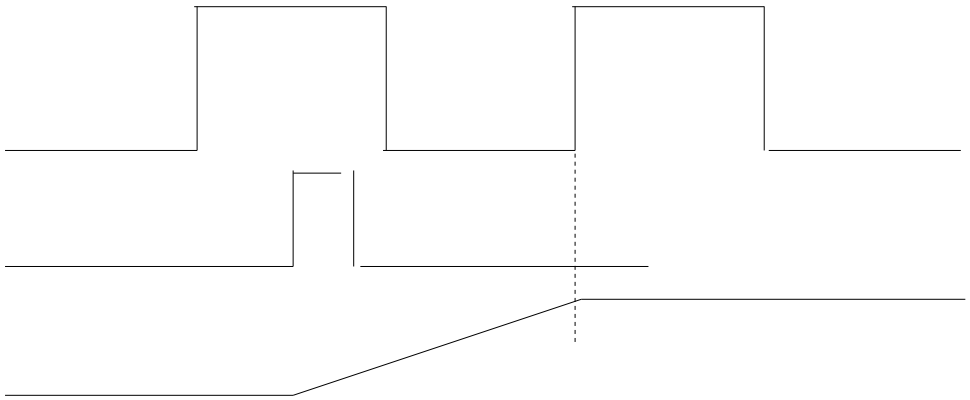
Generating the voltage



- Direct capacitor charge:
  - ➔ Mostly used with discrete implementation or when the capacitor is external.
  - ➔ Current source experience significant voltage variations across its terminal,



- ➔ Integrator approach
- ➔ Current source at virtual ground;
- ➔ Output does not need to be a ramp;
- • Just wait for the amplifier settling time.



- TAC as analog interpolators
  - ➔ A digital counter counts the clock pulses.
  - ➔ The TAC interpolates the time between the signal of interest and a suitable clock edge.

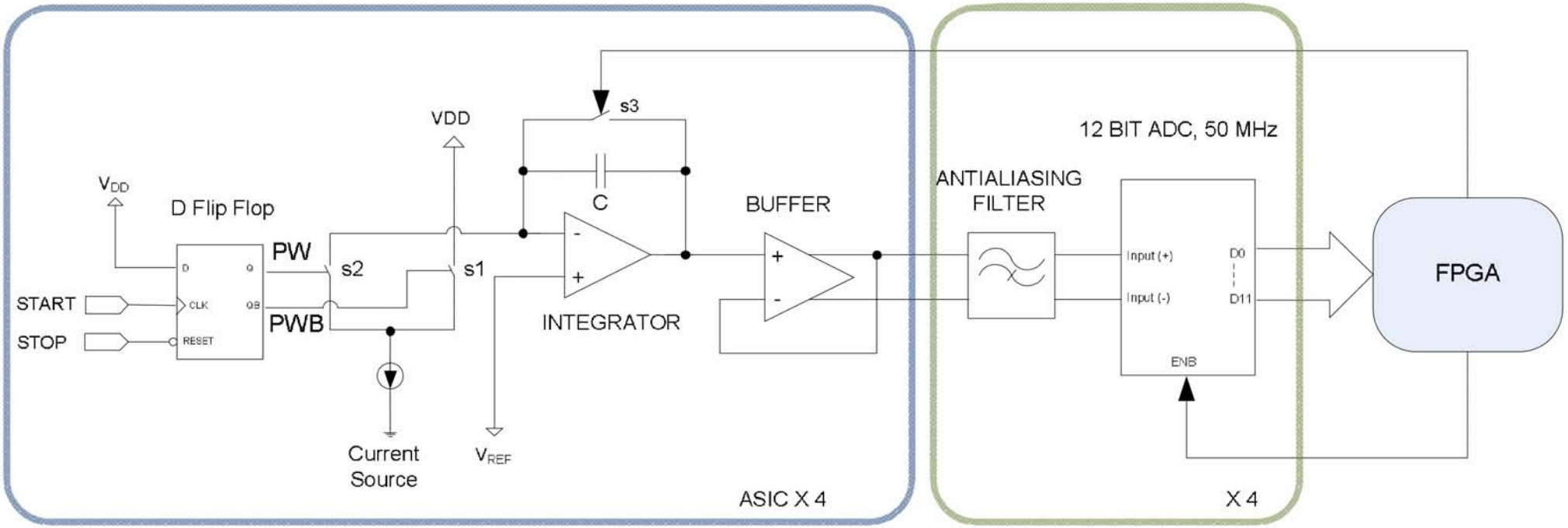
Digitizing the the voltage

2008 International Conference on Design & Technology of Integrated Systems in Nanoscale Era

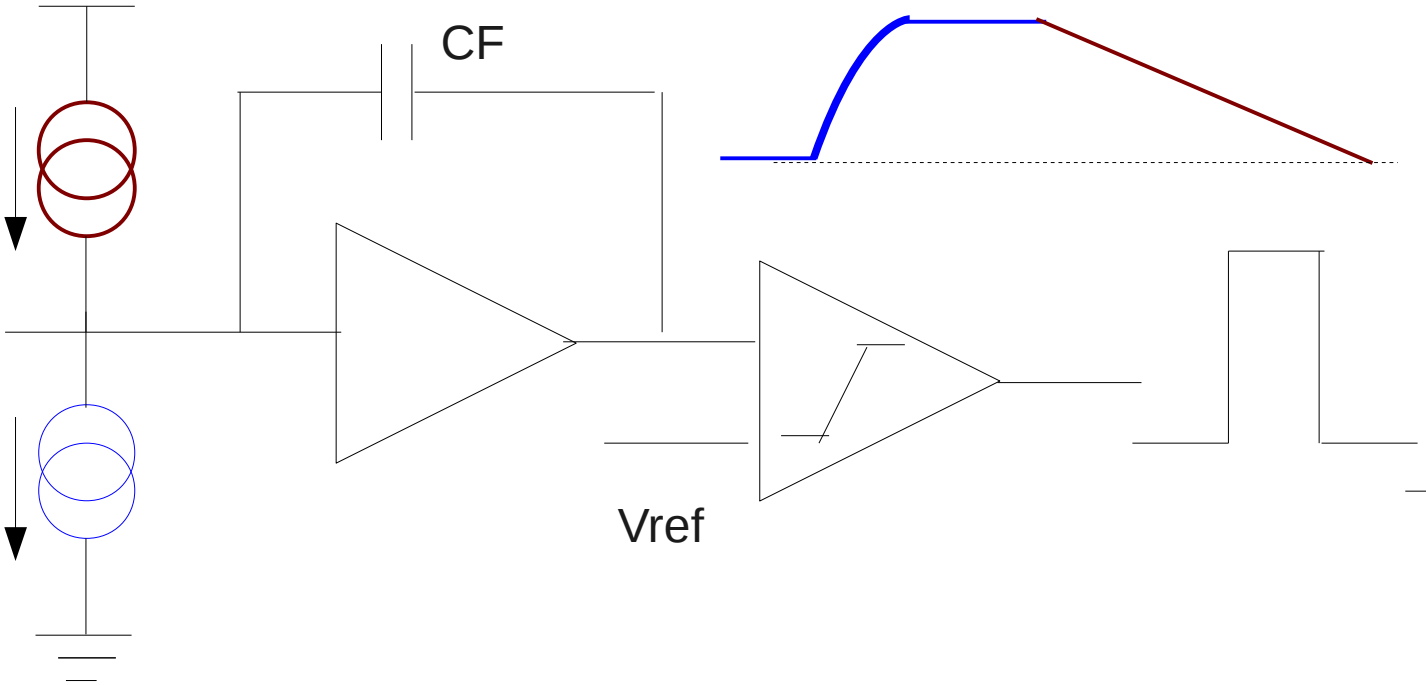
High Precision Time-to-Amplitude Converter for Diffuse Optical Tomography Applications

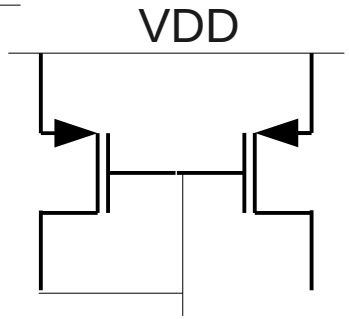
Moez Kanoun, Yves Bérubé-Lauzière, Réjean Fontaine
Department of Electrical and Computer Engineering
Université de Sherbrooke, Sherbrooke, Québec, Canada, J1K 2R1
{Moez.Kanoun}, {Yves.Berube-Lauziere}, {Rejean.Fontaine }@USherbrooke.ca

- In principle, any ADC can do the job

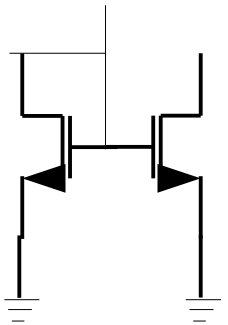


Practice: Wilkinson can be very convenient





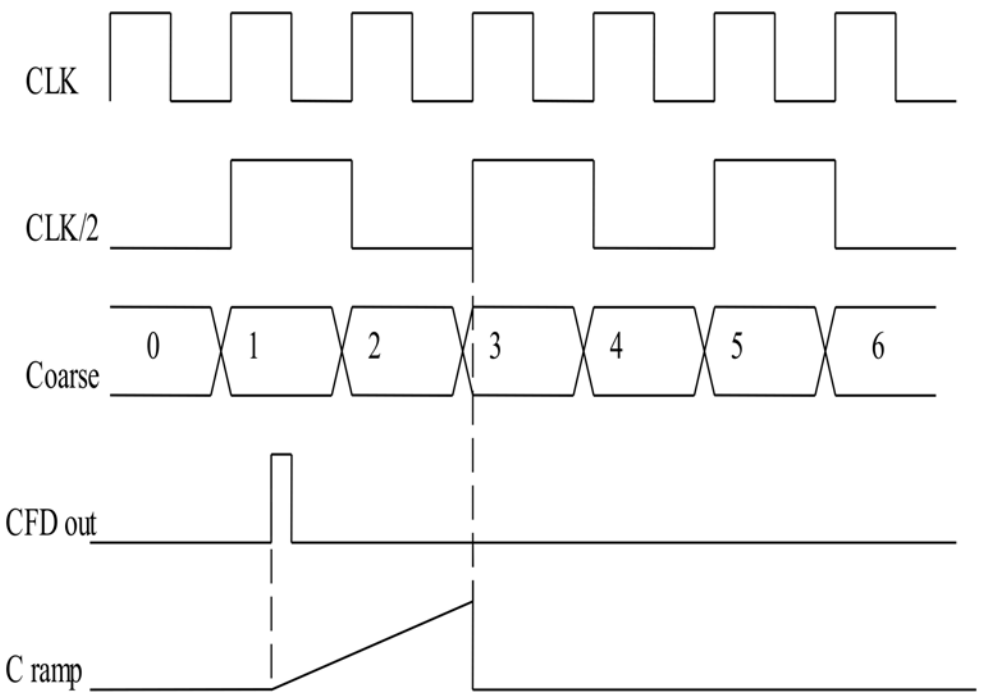
- Example: Main clock to be interpolated: 25 ns
- 8 bit resolution=97.5 ps time bin=> rms resolution: 28.5 ps.
- Counter running at 40 MHz => Ratio between currents 256.
- Dead-time: 6.4 μs.
- Power can be as low as 0.1 mW or less.

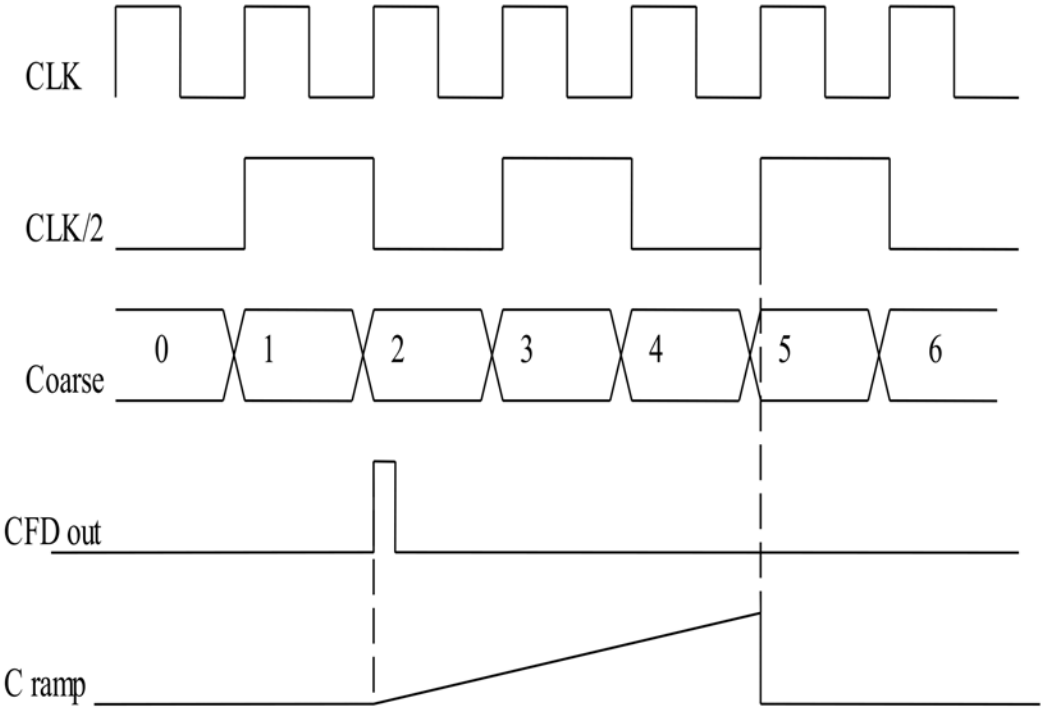


- Issues: Speed, ratio between currents, current source implemenation

Increasing the conversion speed

- Increase the conversion clock!
- This also reduces the ratio between current sources
- For instance, 160 MHz clock yields 4x reduction: from 256 to 64
- Still keep the full scale at 25 ns. Why?

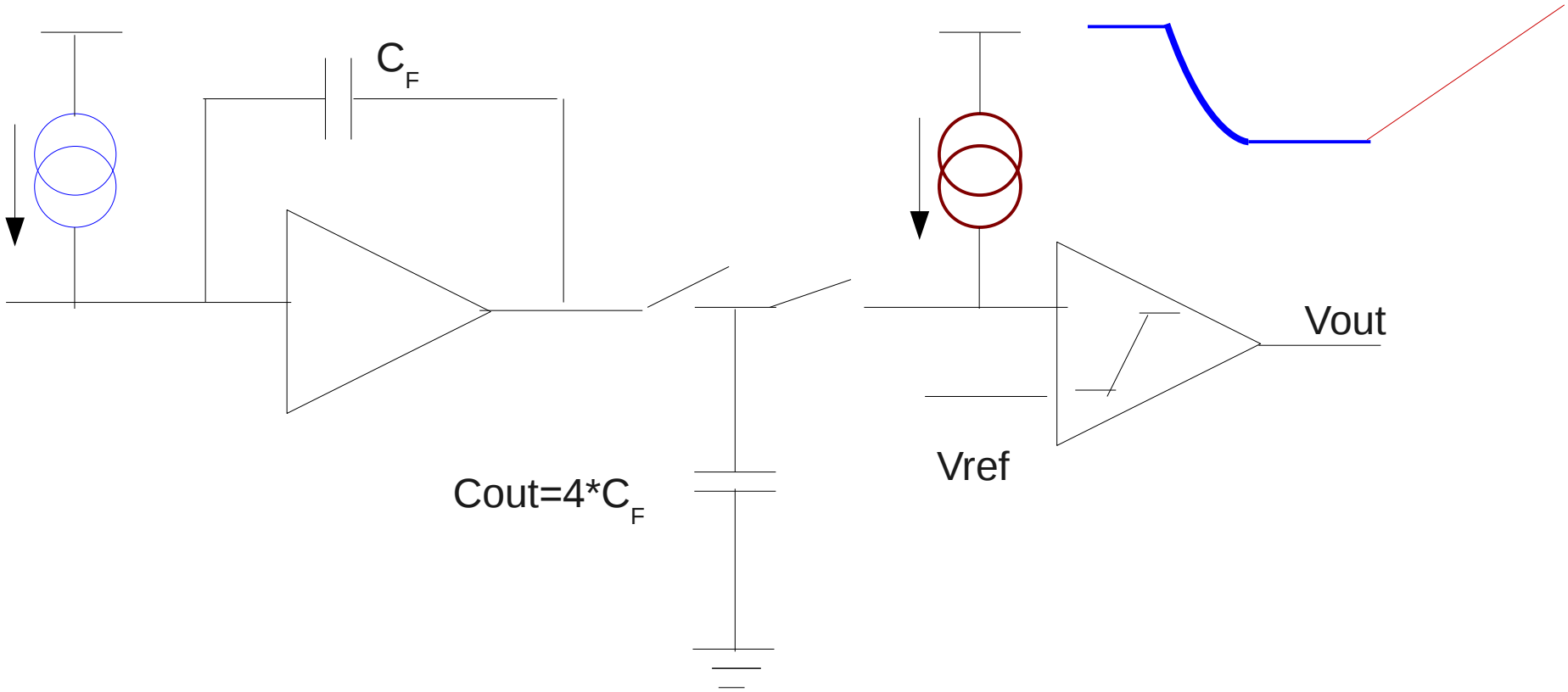




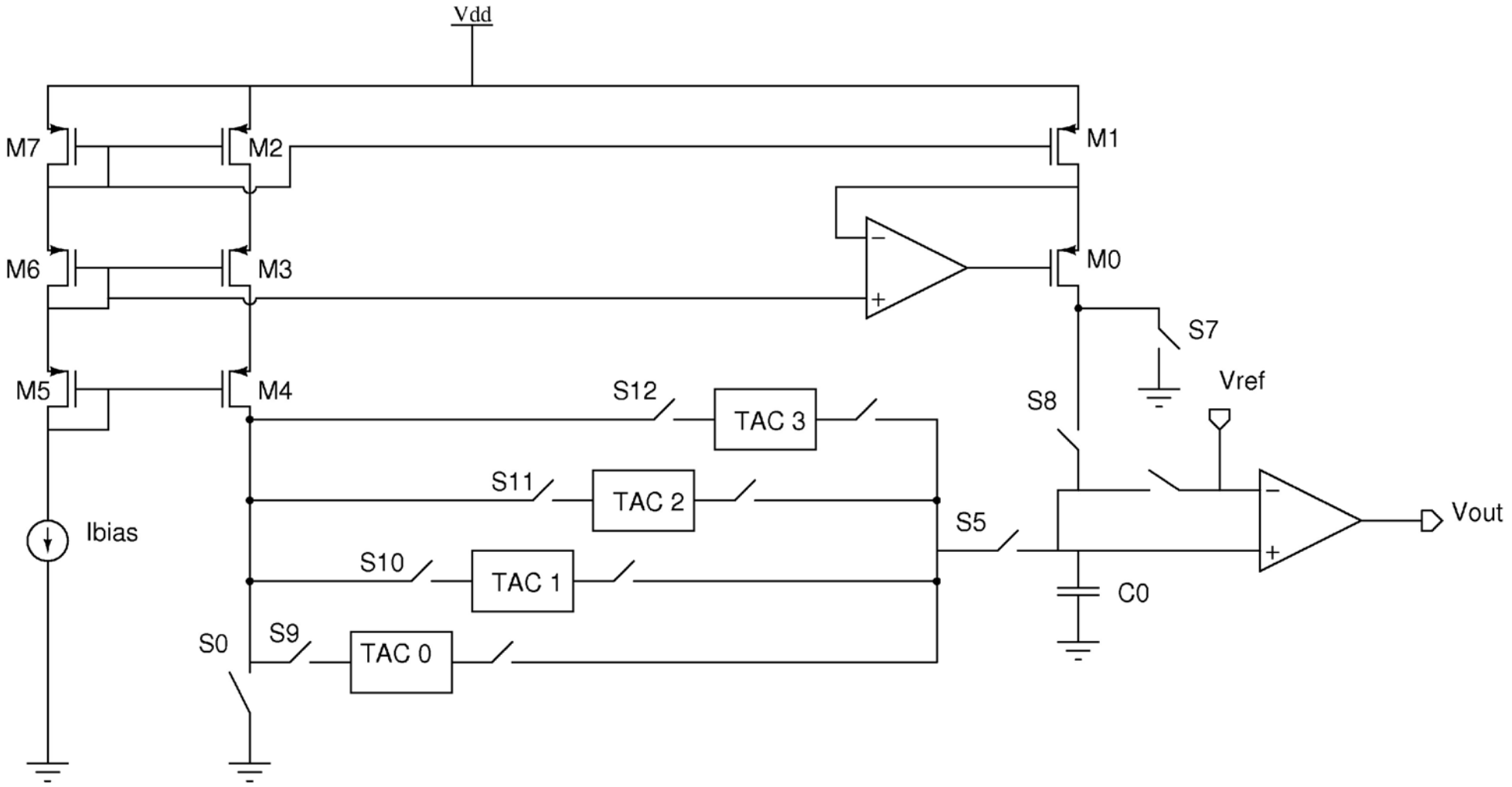
- Introduce offset to avoid sudden “switch-on, switch-off”.
- Use over-ranging to correct for potential ambiguities

Re-sizing and folding the current source

- Precharge C_F to Vref and discharge it when the pulse arrive.
- Transfer the voltage on Cout.
- Recharge Cout back to Vref: currents have the same polarity
- Cout=4*C_F, current source ration scales further by 4x, from 64 to 16.
- Design becomes compact
- Range to interpolate: 18.75 ns, 192 counts, dead time 1.2 µs, 830 kHz.
- Better than 99% 8.3kHz, assuming Poisson incoming rate => Buffering.

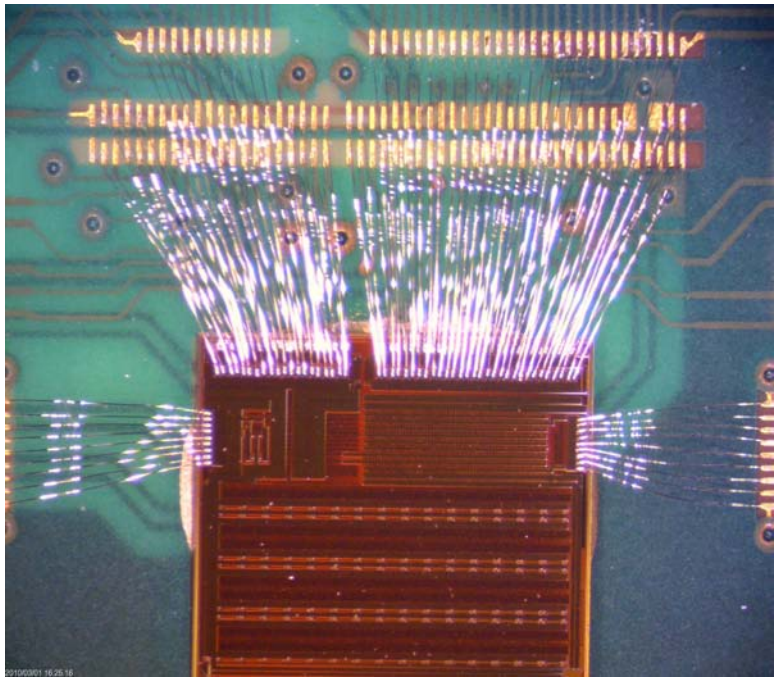


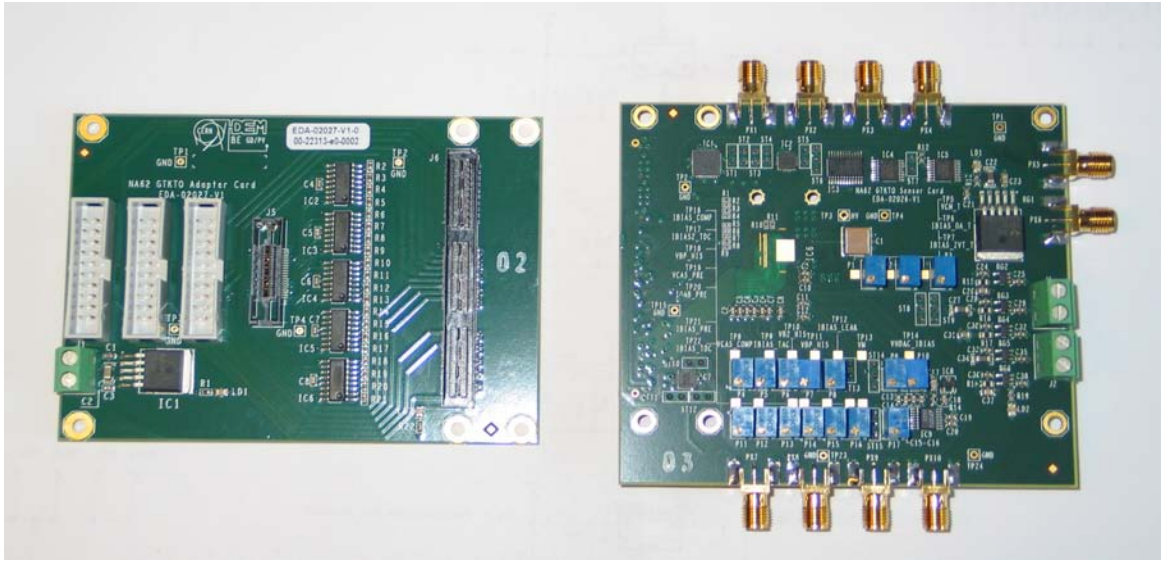
Full TDC implementations



Four integrators available.
Input arrival time averaging
Better than 99.5% at 200 kHz rate (average of a Poisson distribution)

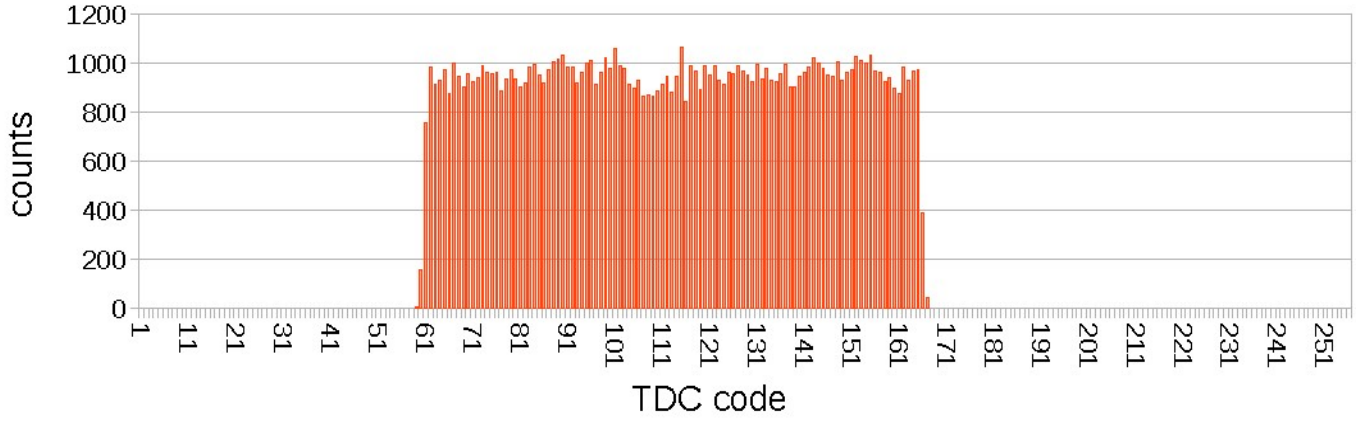
Chip prototype with 105 TDCs

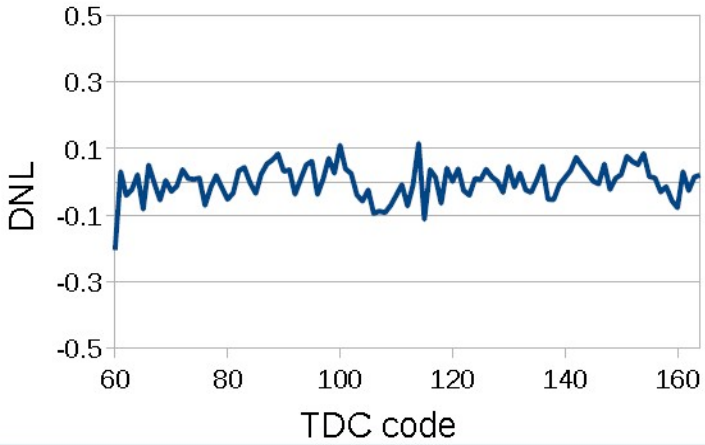


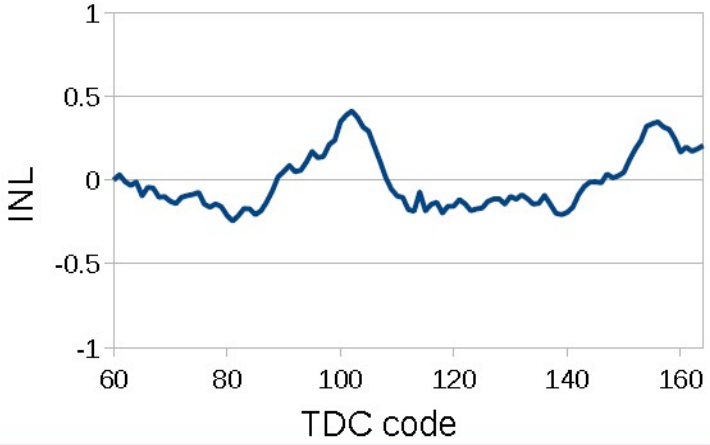


- Developed in the R&D for the NA62 Gigatracker.
- Each channel is 300 μm x 300 μm.
- In each channel: preamplifier+constant fraction discriminator+4-buffer TDC
- Power: 2.5 mW/ch

TDC performance





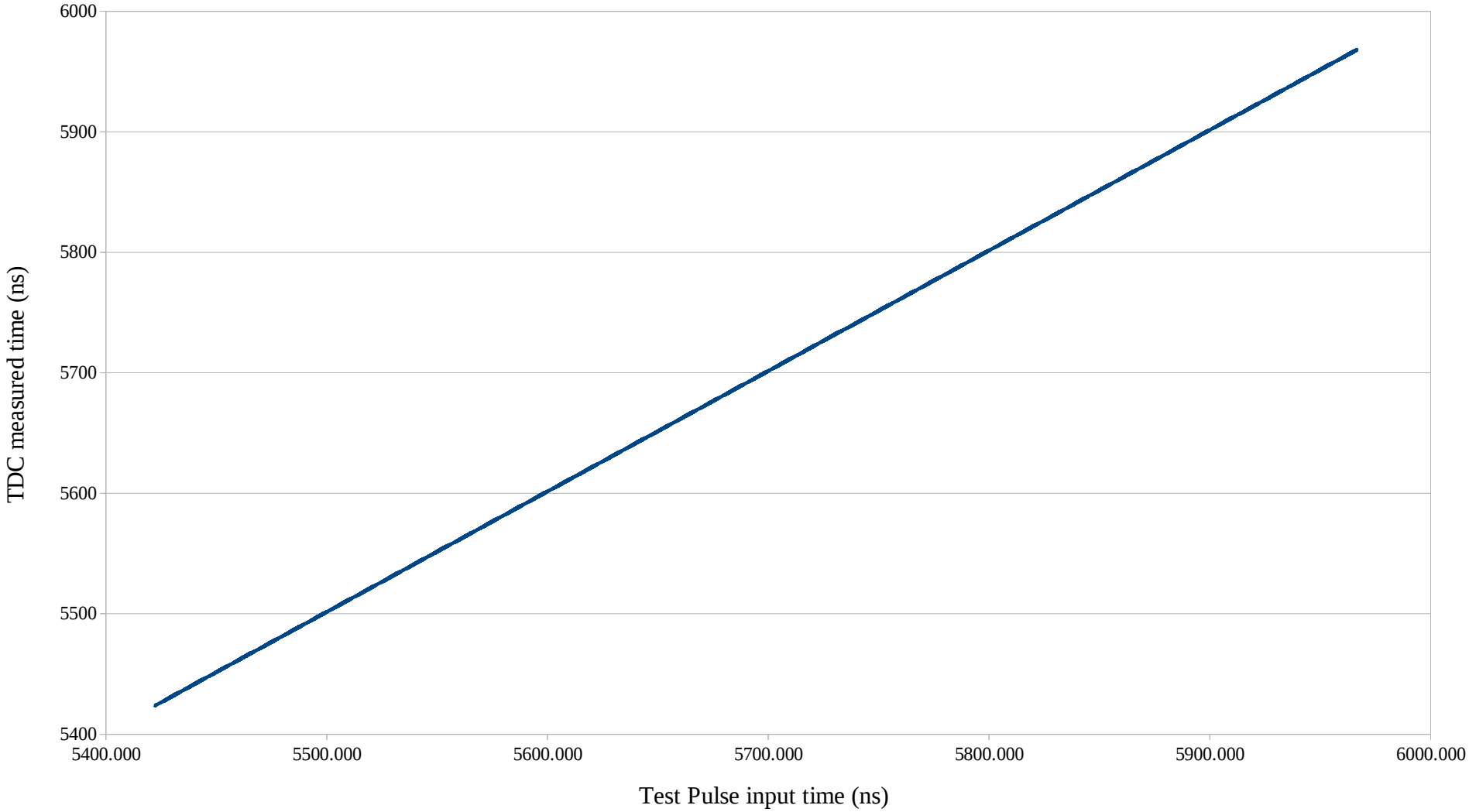


10^5 random test pulses to the 7-bit TDC: $N_{th}=10^5/2^7$

$$-0.5 < DNL(i) = \frac{N_{EXP}(i) - N_{th}(i)}{N_{th}(i)} < 0.5$$

$$-1 < INL(i) = \sum_{i=0}^{k} DNL(i) < 1$$

TDC performance



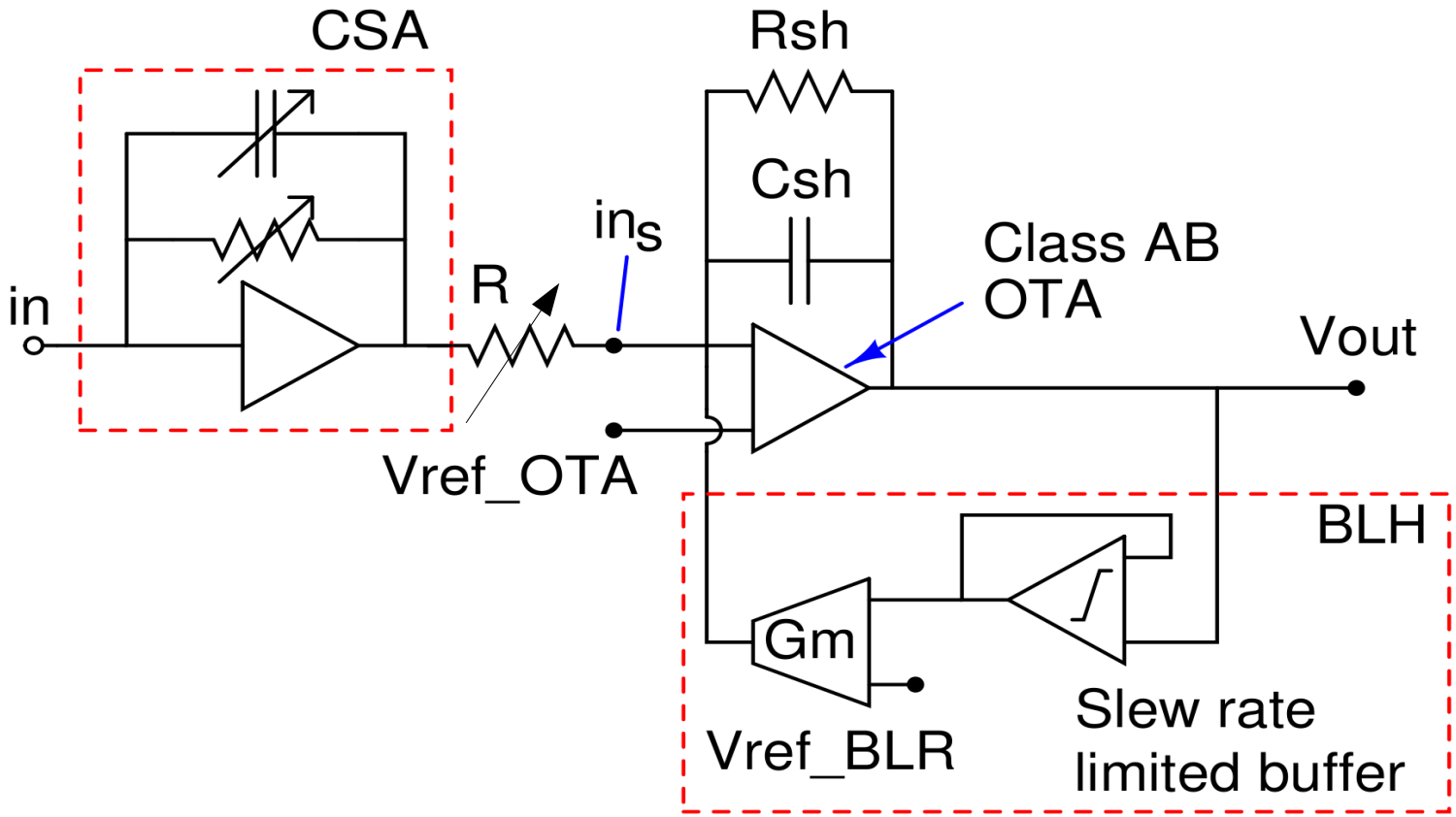
Fast binary front-end for multi-anode PMT

- Development of a fast binary read-out chip for Compass at CERN;
- Chip designed to replace an older ASIC (MAD4) in the RICH upgrade;
- MAD4: 0.8 μm BiCMOS chip developed by INFN-Padova for CMS muon drift tubes.
- User requirements:
  - Full compatibility with the existing read-out electronics;
  - Reduced gain for MPT and same gain of the MAD4 for other applications;
  - Threshold adjustable channel by channel;
  - Maximum hit rate > 5 MHz/channel;
  - Power consumption < 30 mW/channel;
  - Technology: standard 0.35 μm CMOS.

CMAD design choices

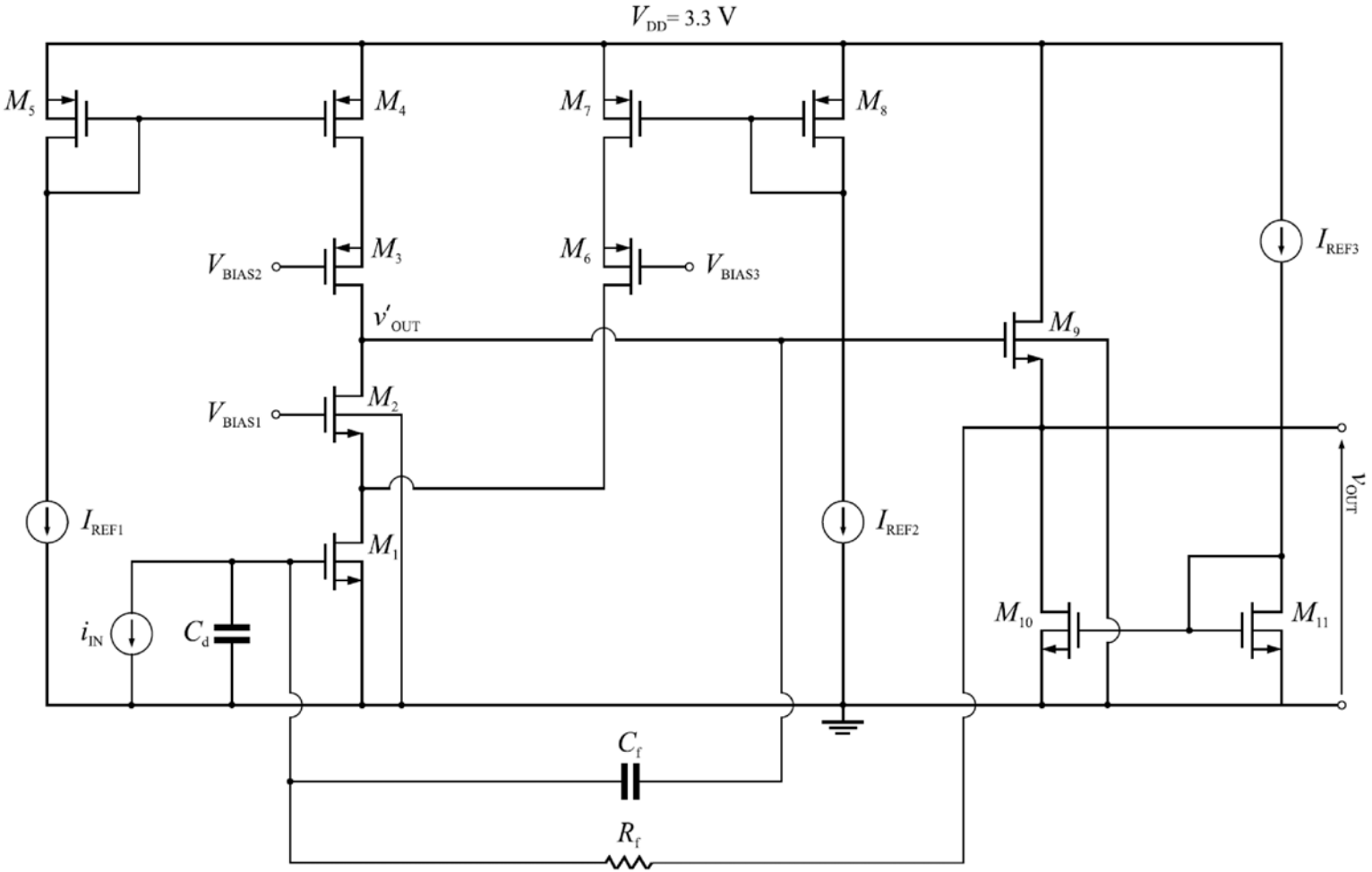
- Work with very low threshold to minimze time walk while using a simple leading edge discriminator:
  - Low noise front-end amplifier:
  - Minimal threshold dispersion.
- Maximize linear operation to allow quick recovery from overdrive;
  - Rail-to-rail output stage before discriminator.
- Keep maximum flexibility:
  - Programmable front-end amplifier
  - “Digital shaper” to guarantee either an output pulse of fix duration or a pulse width modulated by amplitude to allow Time over Threshold operation.
- Design for 10 Mhz/channel operation to have good safety margin.

First stage: overview



- Moderate input capacitance (< 20 pF):
  - Input stage: transimpedance amplifier with resistive and capacitive feed-back
  - Programmable resistance and capacitance in the first stage feed-back
  - Programmable coupling resistance between the stages

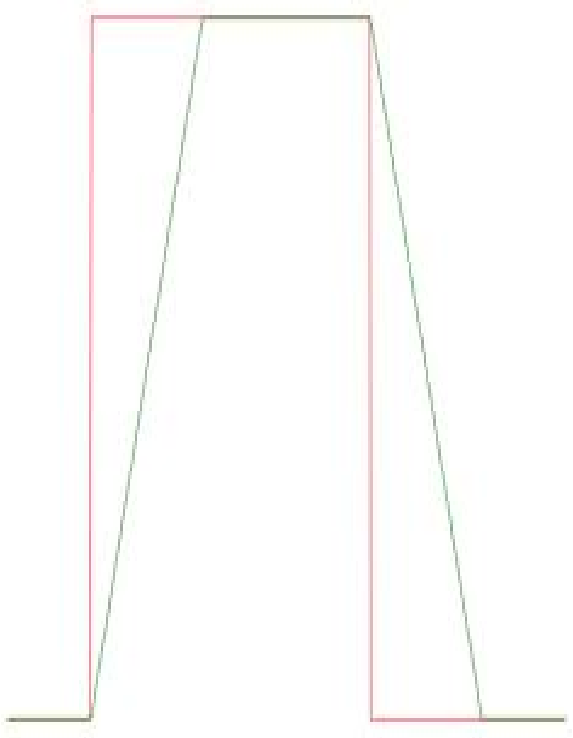
First stage: transitor level implementation



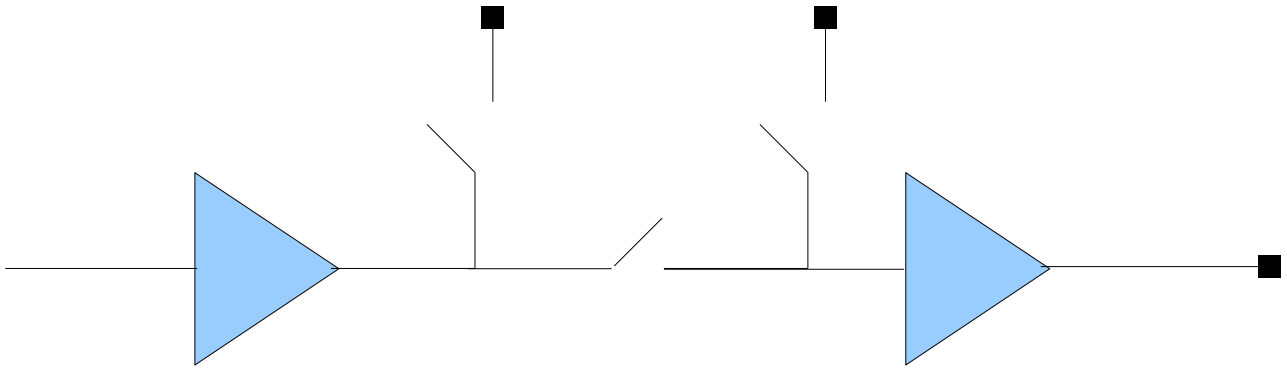
- Single ended telescopic cascode stage:
  - NMOS input to maximize gm and bandwidth: GBW=gm/Cload
  - PMOS loads to minimize current source noise contributions: $Sn=4kTgm_4^2/gm_1^2+4kT/gm_1$
  - Split current sources to maximize gain: Av= gm1*Rload

Second stage: requirements

- Inverting configuration: input is at virtual ground
- High output swing in however needed to maximize the dynamic range
- High slew rate to avoid pulse distortion



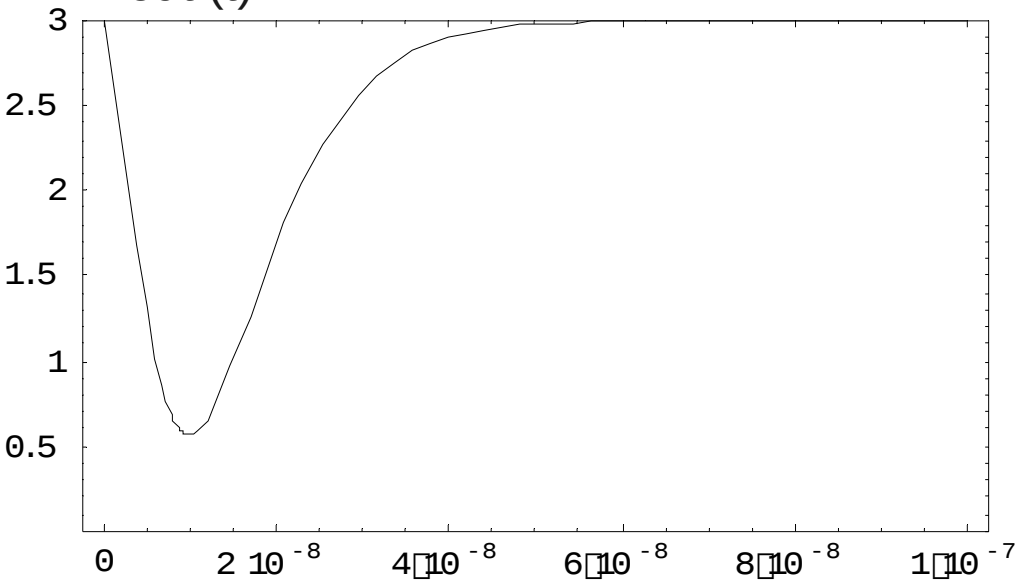
➔ Slew rate=Iout/Cload
➔ Output capacitance modest (<0.5 pF), but need of observing directly the output for testing/debuggin purposes.
➔ Not to distort a sinudoid input SR>2πfVp



Slew rate limitations in pulse amplifier

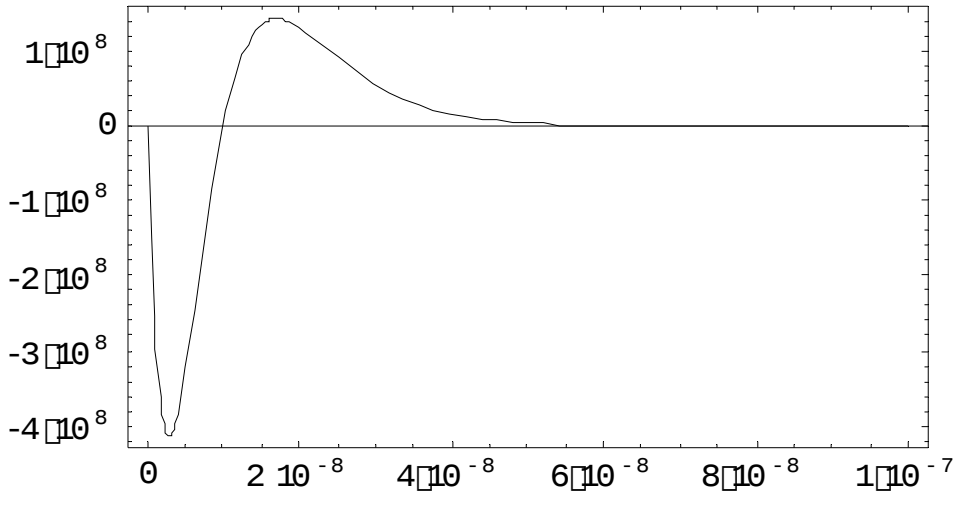
- For fast semi-gaussian shaping slew rare requirements are quite demanding
- Ex: 2.5 V at 10 ns peaking time requires SR of 400 V/μs
- For a class A amplifier and 10 pF bias current of 4 mA.

Vout (t)



time (ns)

dVout (t)/dt

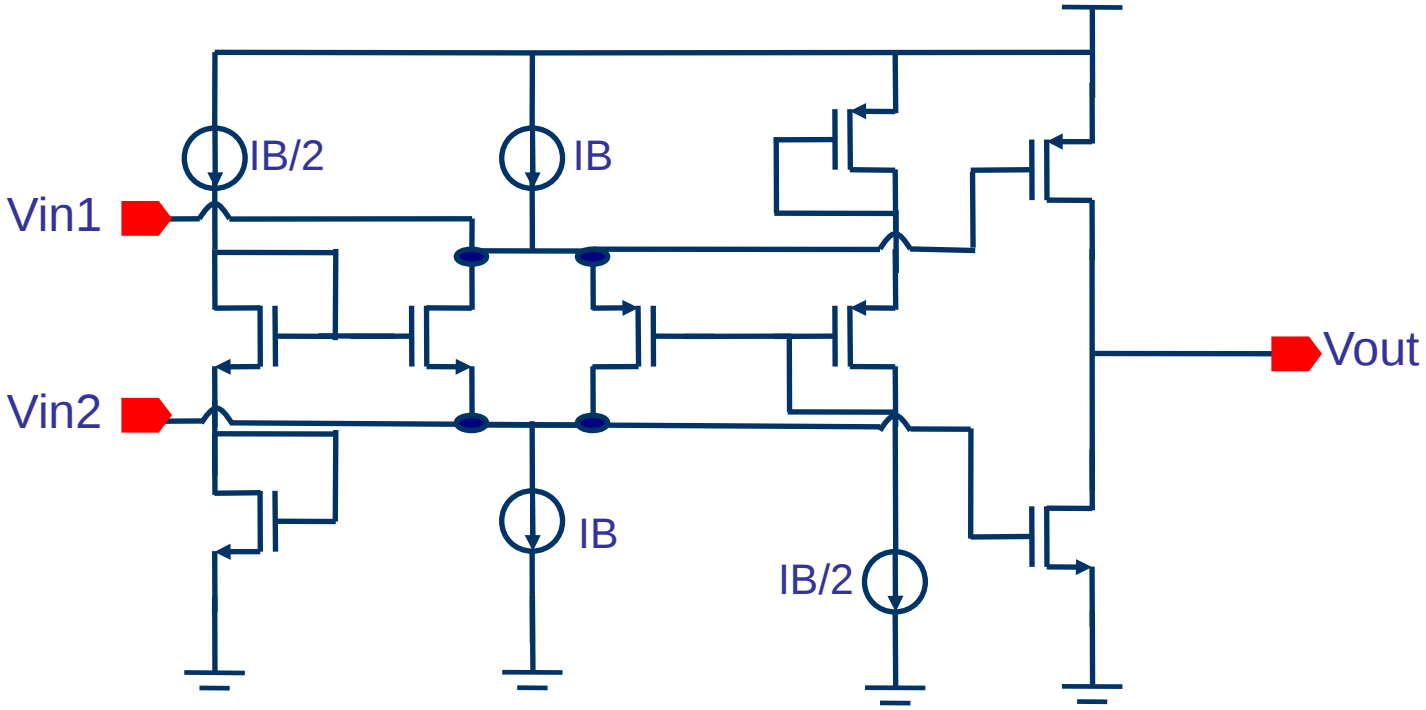


time (ns)

Second stage based on a class AB OTA with rail to rail output

Class AB output stage

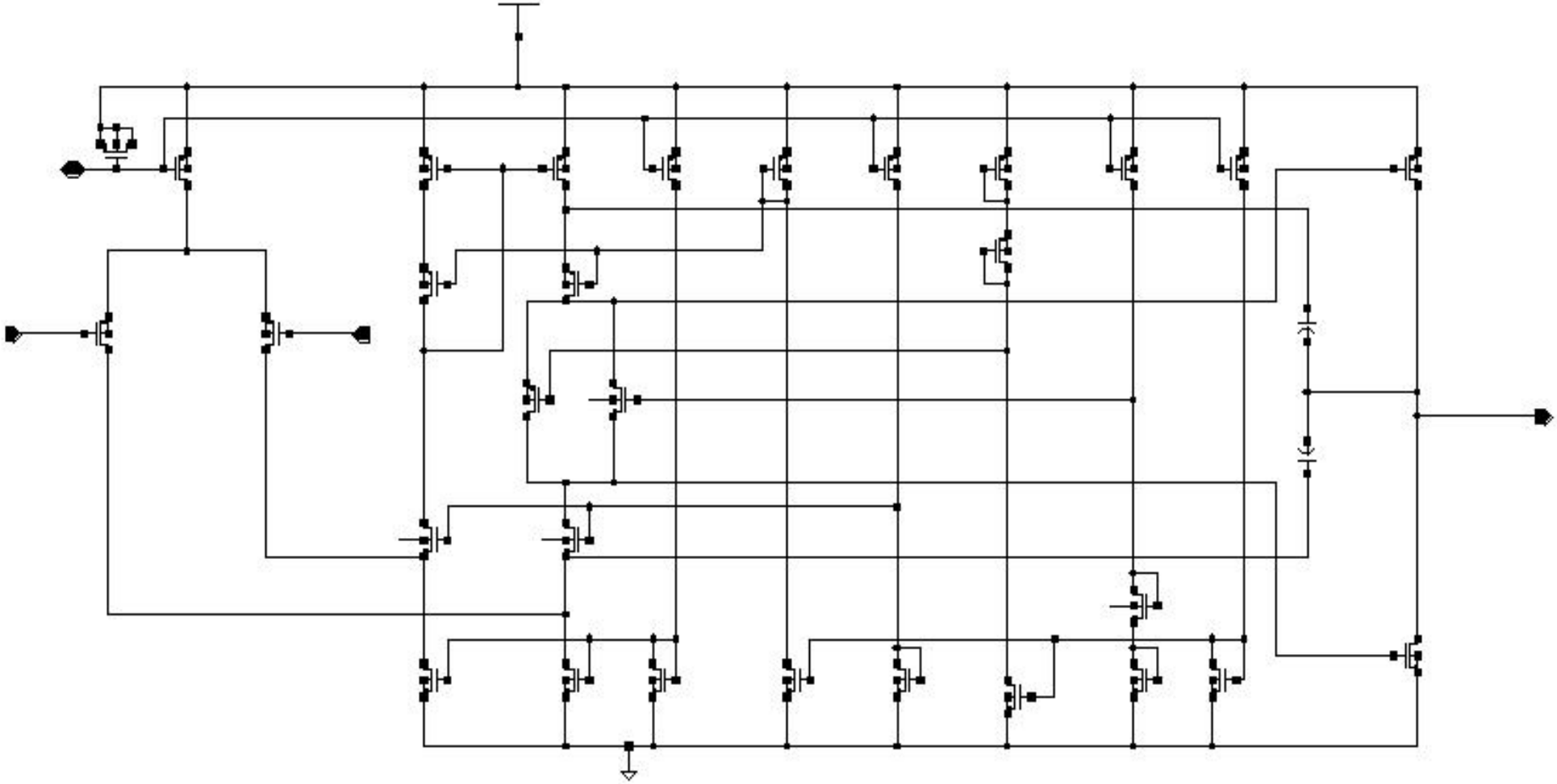
- Output is an inverter;
- The bias circuit set the quiescent current Iq;
- The minimum current for the “non active” transistor is 0.3*Iq;
- The maximum current is >> Iq.



D. M. Montecelli, IEEE JSSC, Vol. SC-21, Dec. 1986
Hogervost et al., IEEE JSSC Vol. 29, No. 12, Dec. 1994.

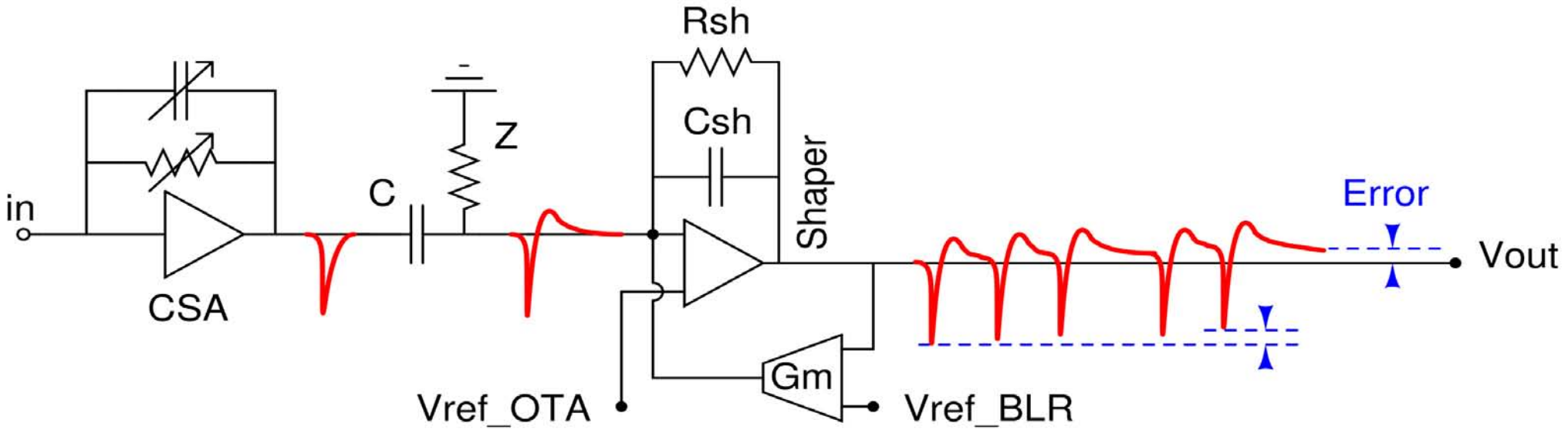
Full operationa amplifier

- Folded cascode with PMOS input devices:
- Input DC level has to match approximately preamp output (0.7 V)
- 3 mW of power, slew greater than 500 V/μs



Baseline control: the principle

- An operational transconductance amplifier (Gm-stage) is inserted in feed-back around the shaper;
- The stage sink current to bring the DC output to the reference voltage to Vref_BLR;
- Bandwidth of the Gm stage must be small otherwise also signal are clipped!
- Large time constant can be implemente with small capacitor by starving Gm.
- The DC output voltage can be locked to the desired reference value



It is an ac coupling, so it can be subjected to rate-dependent baseline drift!

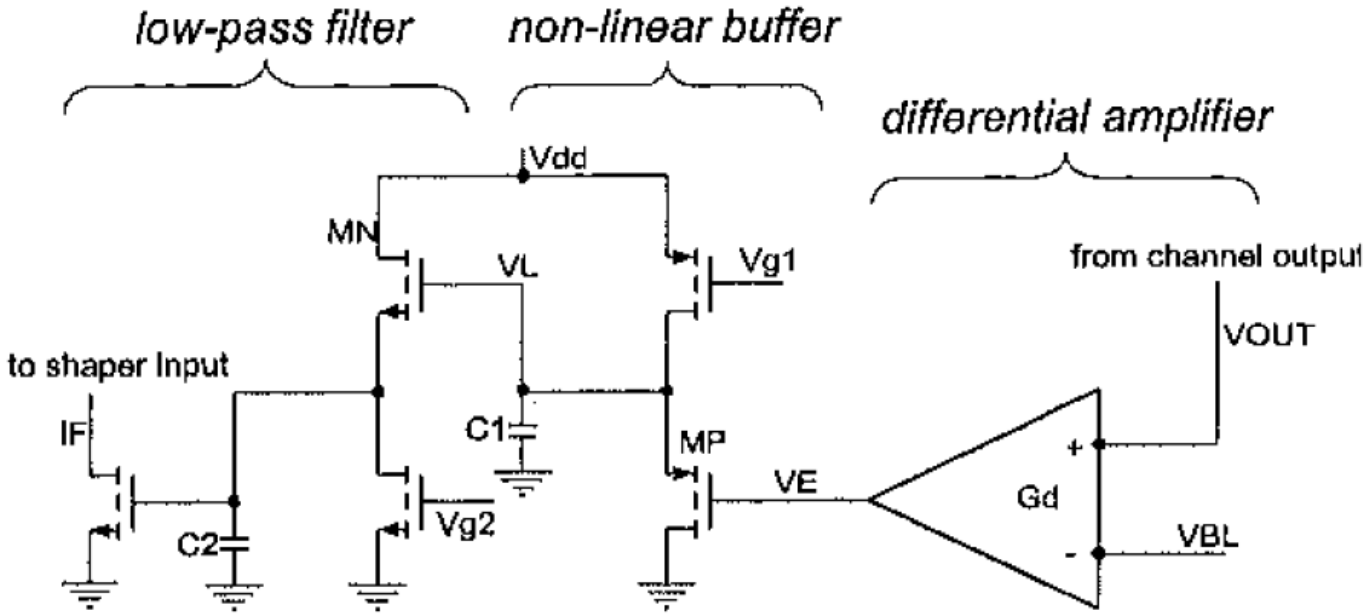
Non linear processing of fast signals

- A non-linearity must be inserted in the chain, so that fast signals are severely clipped;
- Slew rate limitations are very well suited to this purpose.
- So a slew-rate limited buffer must be inserted in the baseline controlling chain.

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 47, NO. 3, JUNE 2000

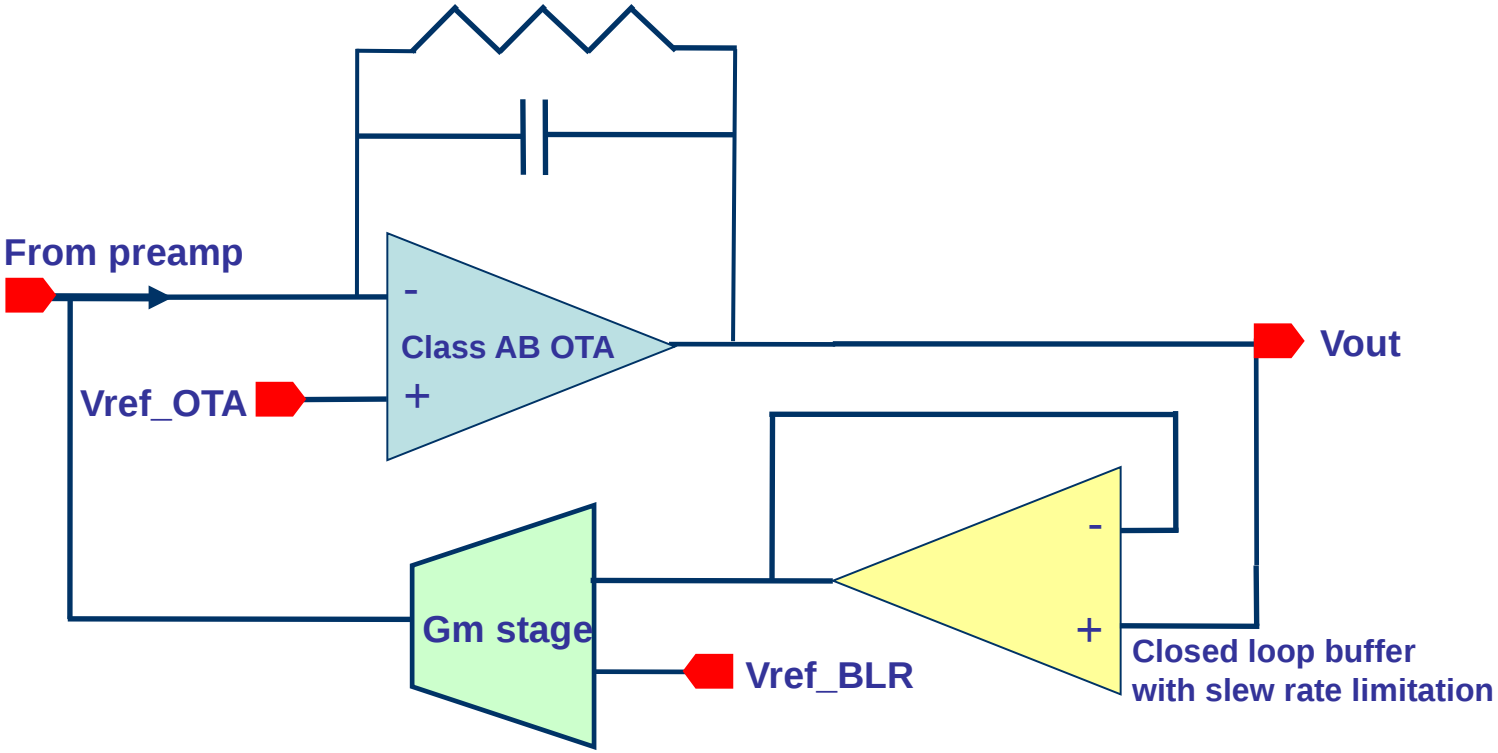
A CMOS Baseline Holder (BLH) for Readout ASICs[1]

G. De Geronimo[2], P. O'Connor[2] and J. Grosholz[3]
[2]Brookhaven National Laboratory, Instrumentation Division, Bldg 535B, Upton, NY 11973, USA
[3]eV Products, Div. of II-VI Inc., 373 Saxonburg Blvd., Saxonburg, PA16056, USA



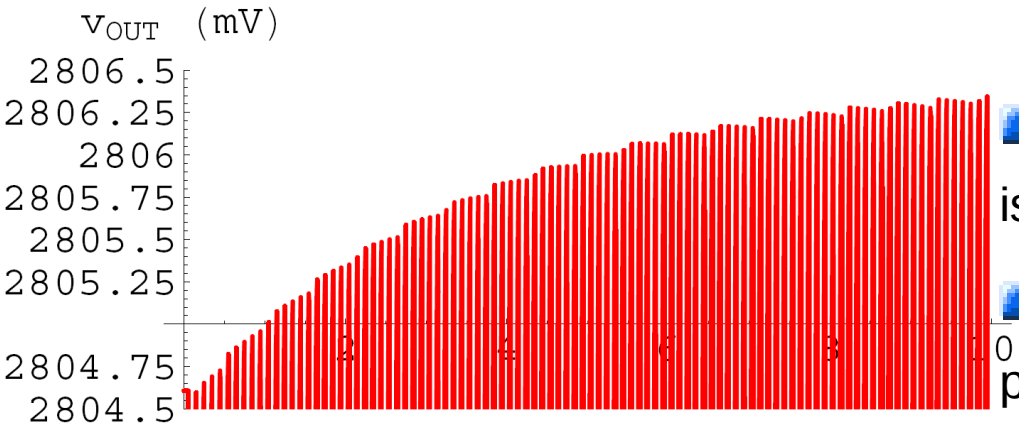
SR limitations with unity gain buffer

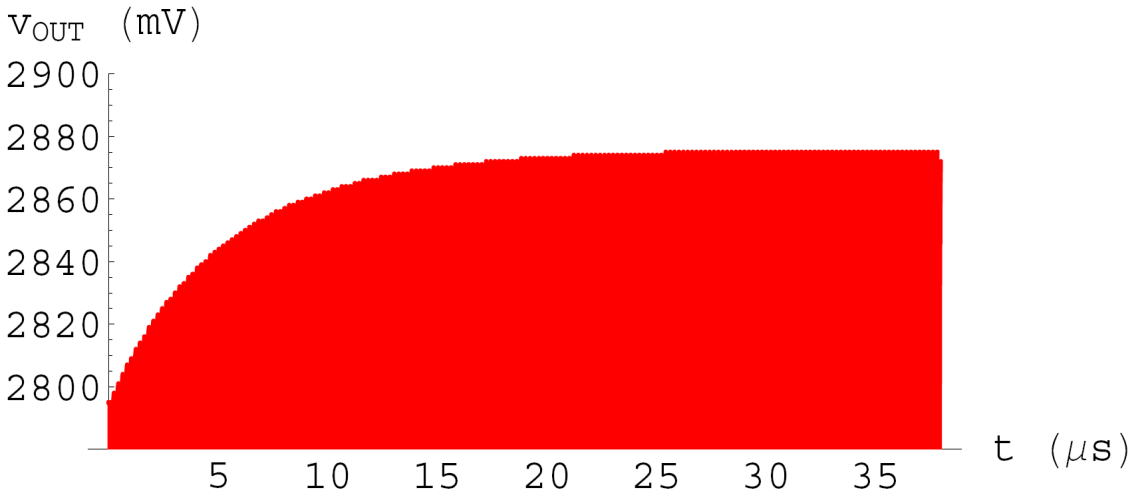
- A voltage follower is used with high-bandwidth e strong slew rate limitation;
- The unity-gain feedback gives an high frequency pole which does not interfere with the compensation.



Effect of slew-rate limitation

- Spice simulations with and without SR-limited buffer

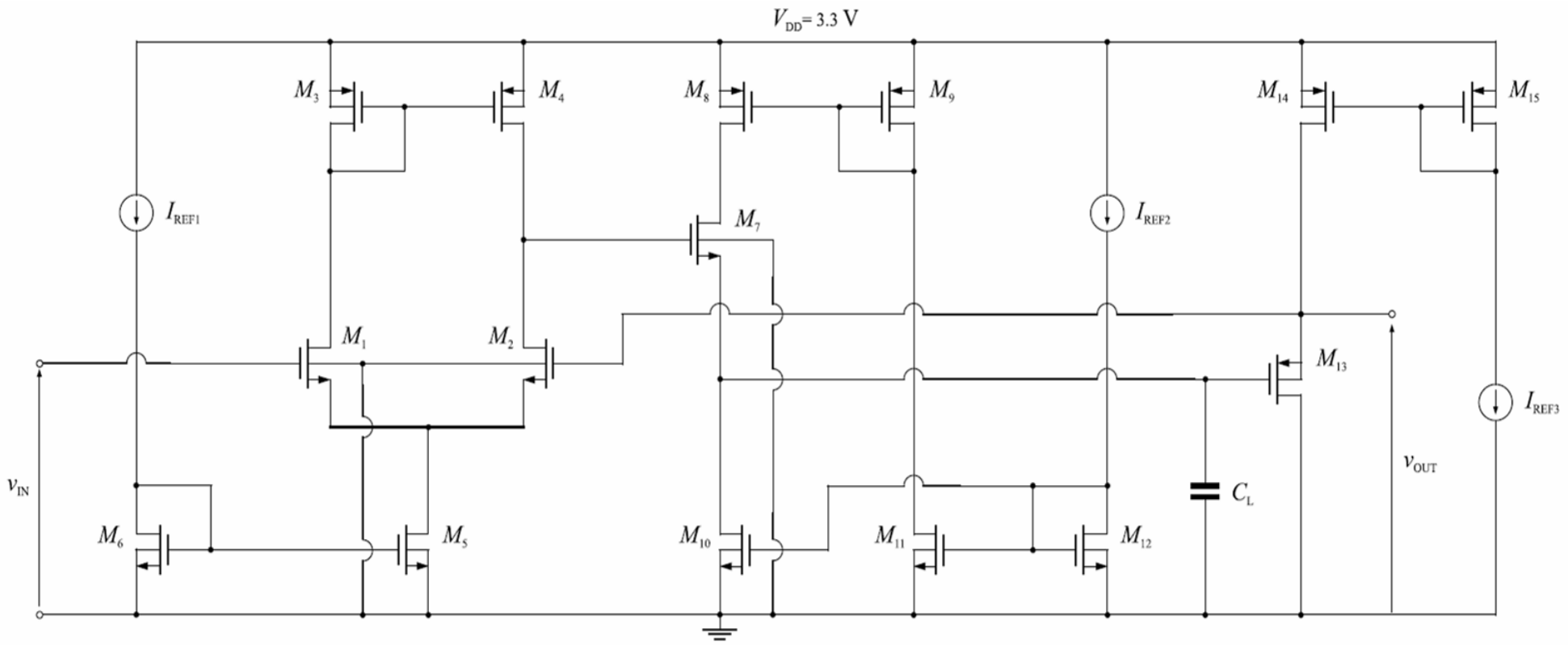




- With 10 MHz, 2.7 V pulse the baseline drift is < 1mV
- This is a very pessimistic assumption. For practical cases baseline fluctuation will be kept in the noise

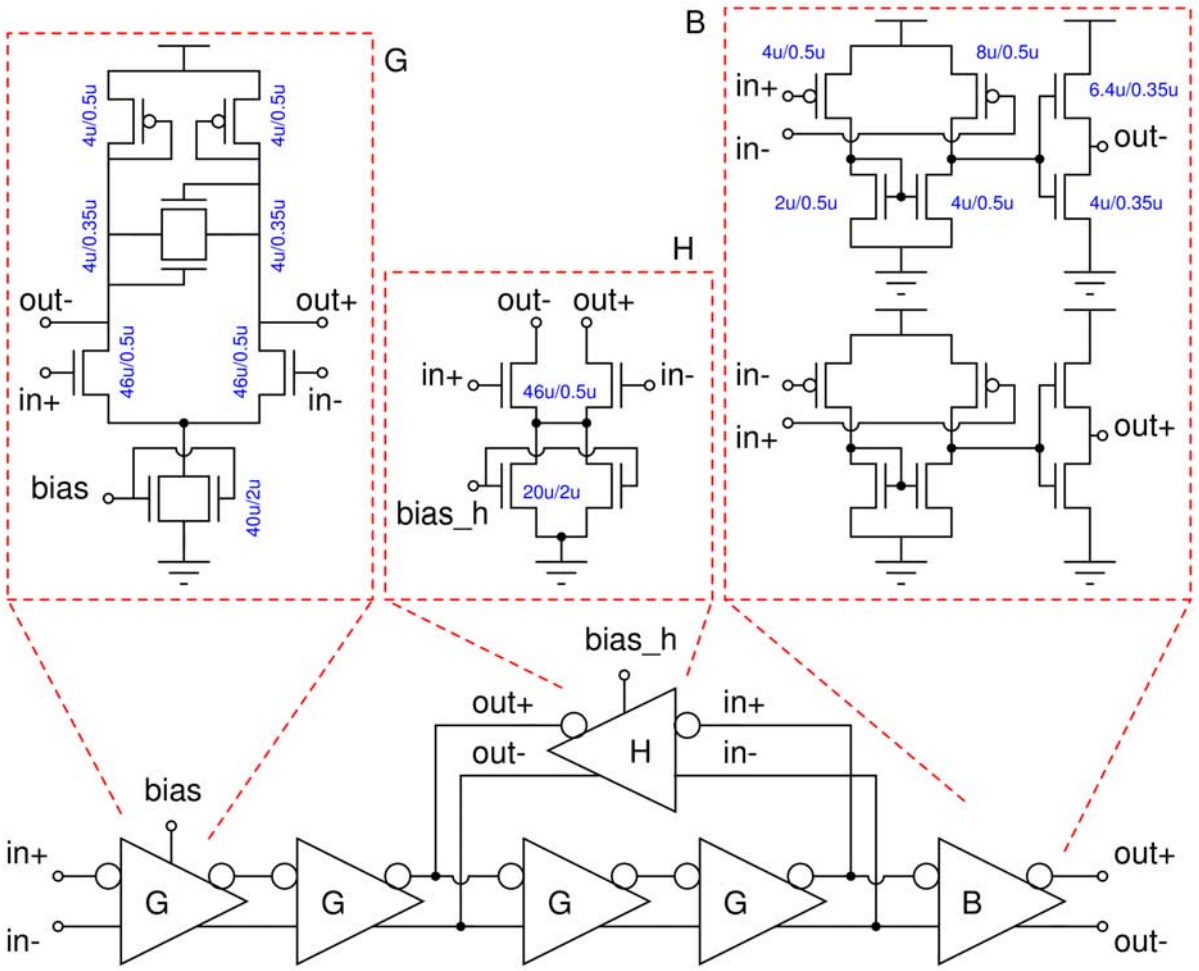
SR-limited buffer schematic

- CL must be protected by charge injection from the past preamplifier output via the parasitics of M1 and M2.



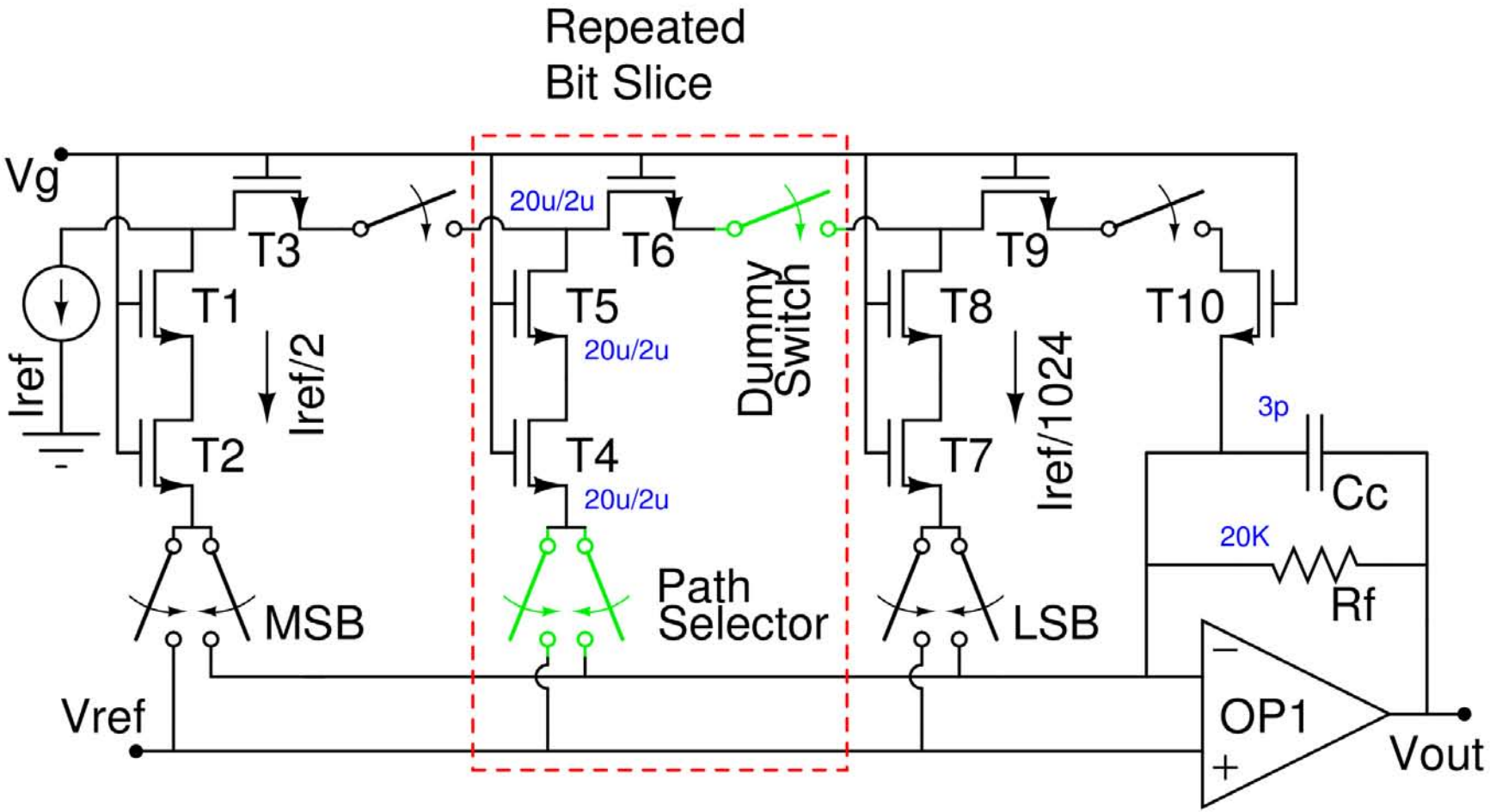
Comparator schematic

- Cascade of fully differential chain with hysteresis;
- Generation of CMOS levels only in the last stage;
- Small devices for high speed=offset.



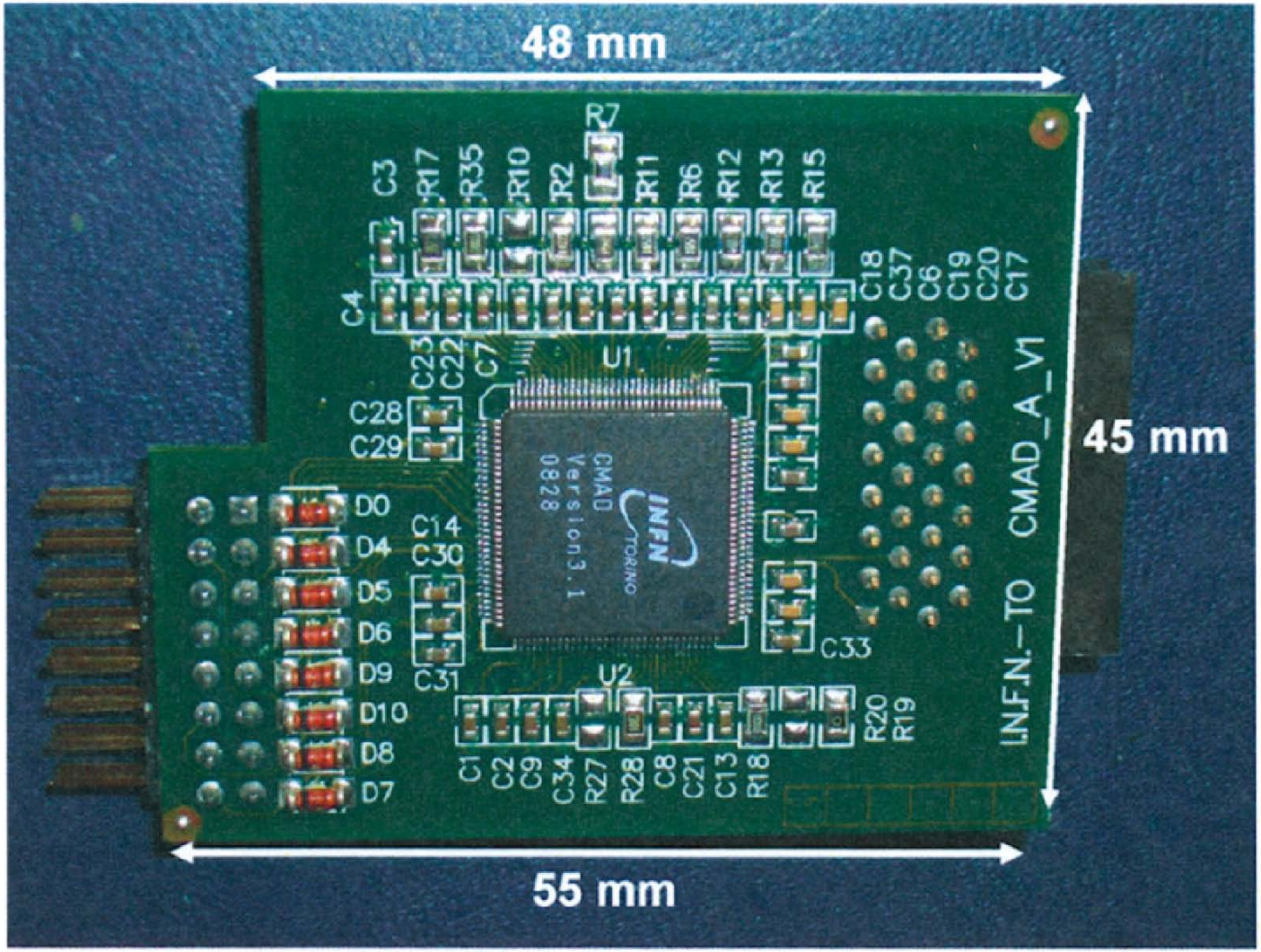
DAC schematic

- Current division by mean of equal slices;
- Size grows linearly with the number of bits;
- Two DACs per channel: one for baselines and one for thresholds.



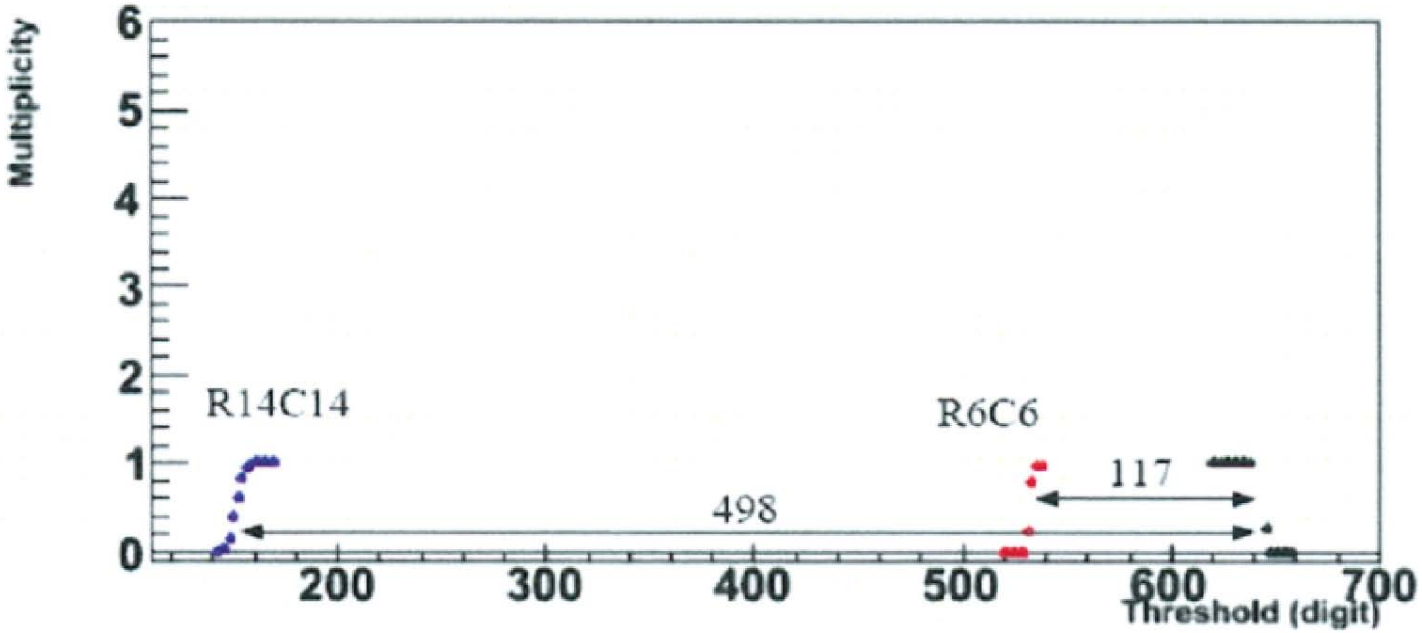
PCB

- Test board used in data taking in the experiment



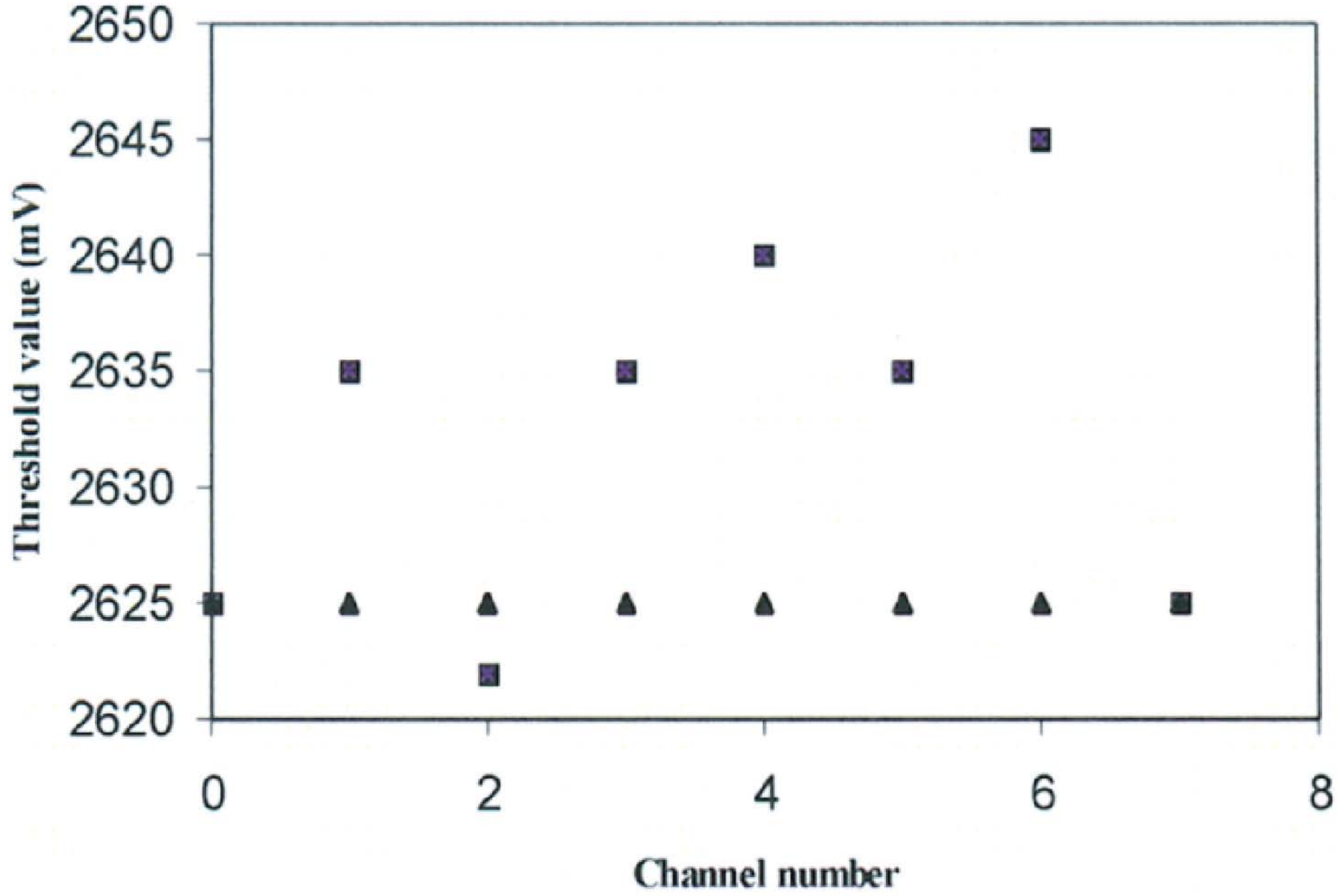
Gain settings

- Threshold scan with the same input signal and two different gain settings



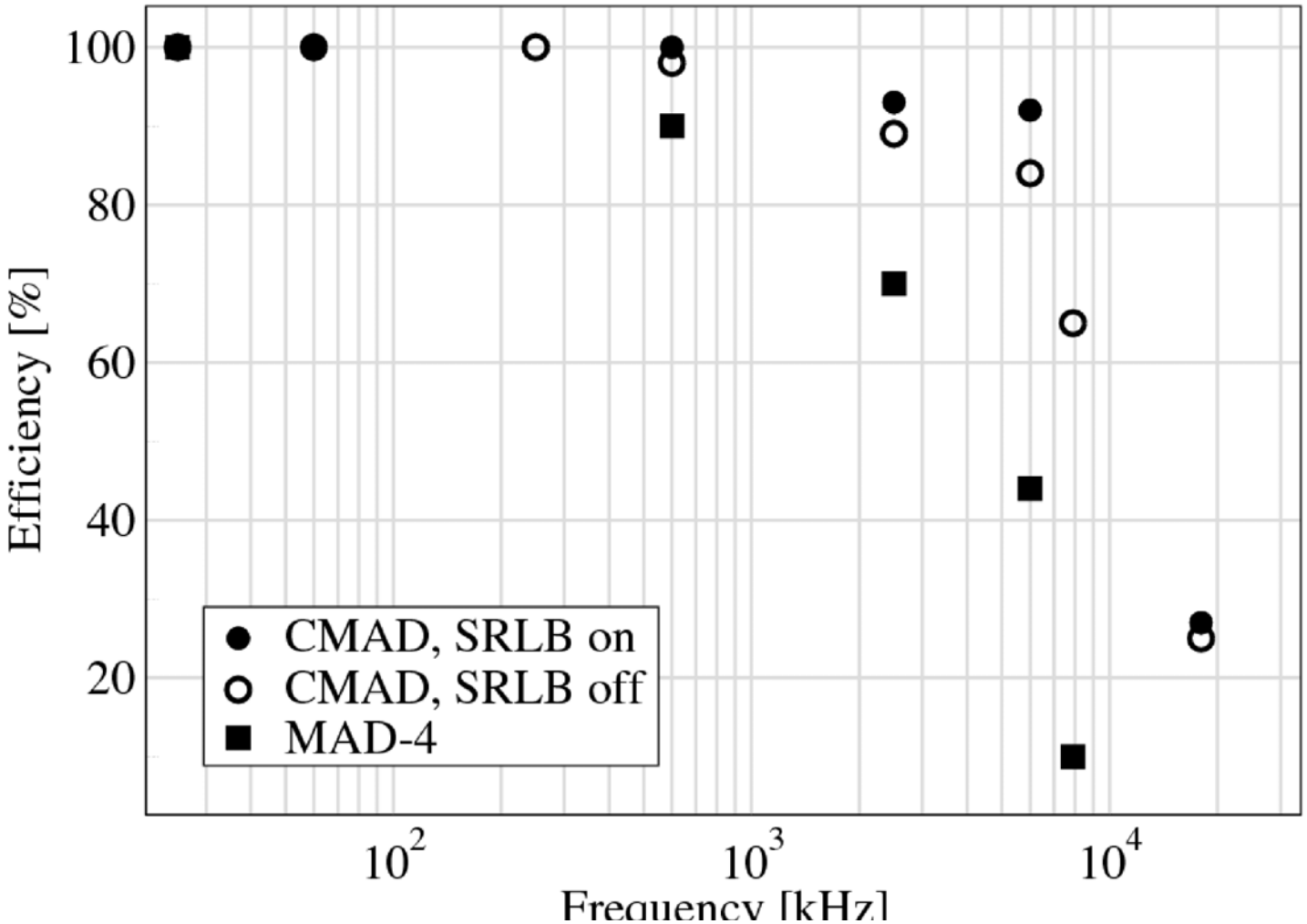
Threshold equalization

- Threshold residual dispersion less than 0.5 mV (200 electrons for the max gain)



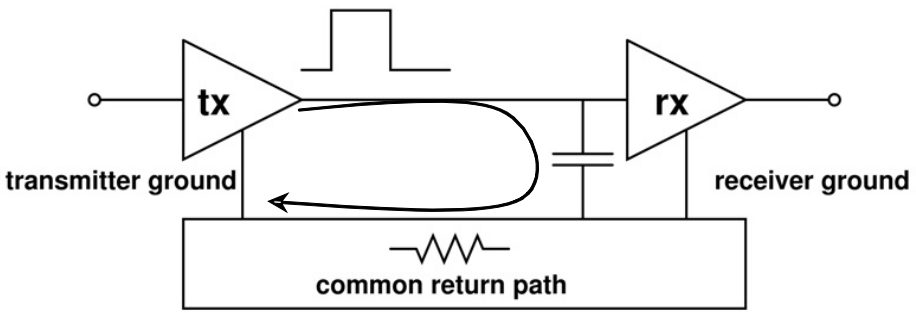
High rate performance

- Efficiency vs rate
- Measurements done with PMTs

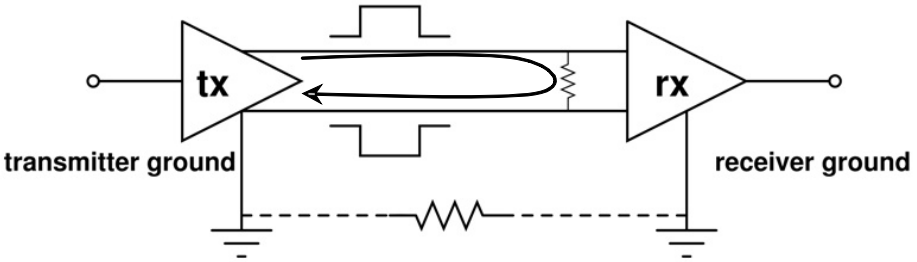


Integrating digital and analog .....

- ...can be very dangerous!!
- 1.2 V x 1 fF= 1 fC = 6250 electons...
- Amplifiers input must be very well isolated from the digital part
- Coupling can easily occur through the I/O
- Use of differential signalling on chip mandatory....

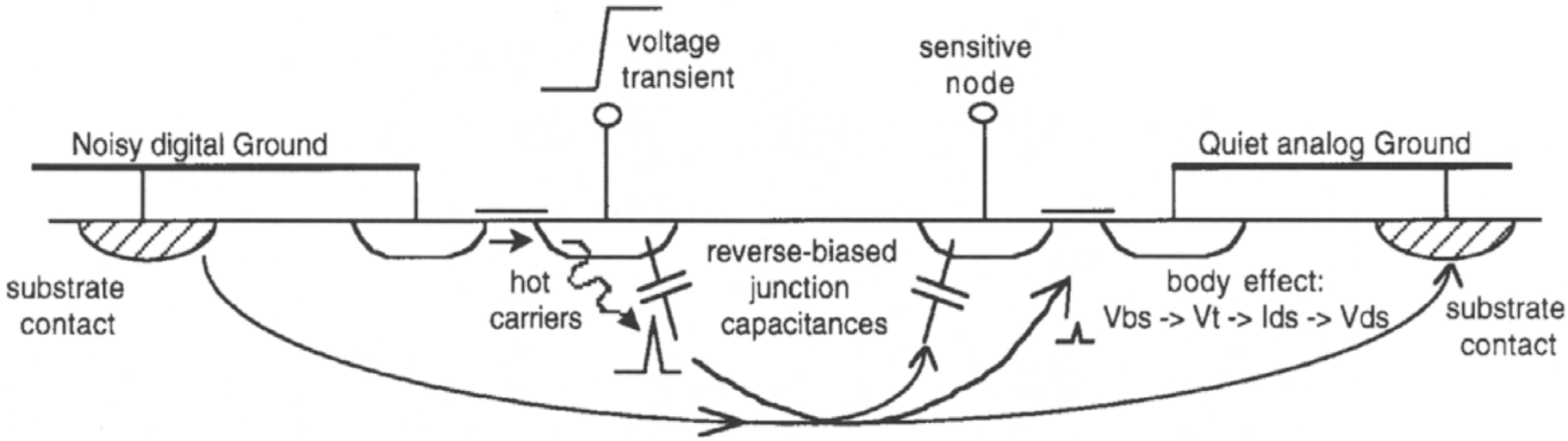


a)



b)

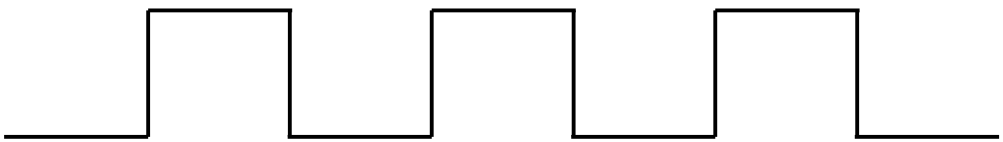
Internal digital coupling



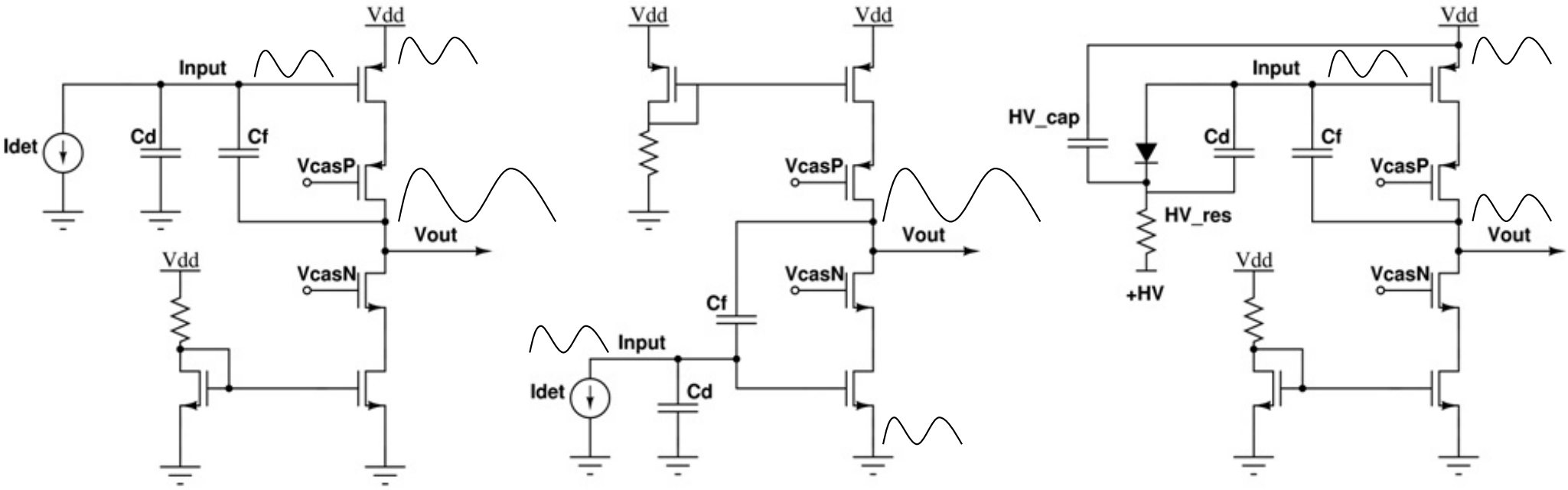
Homogeneous wafer

epi-wafer

Which signals are more dangerous?

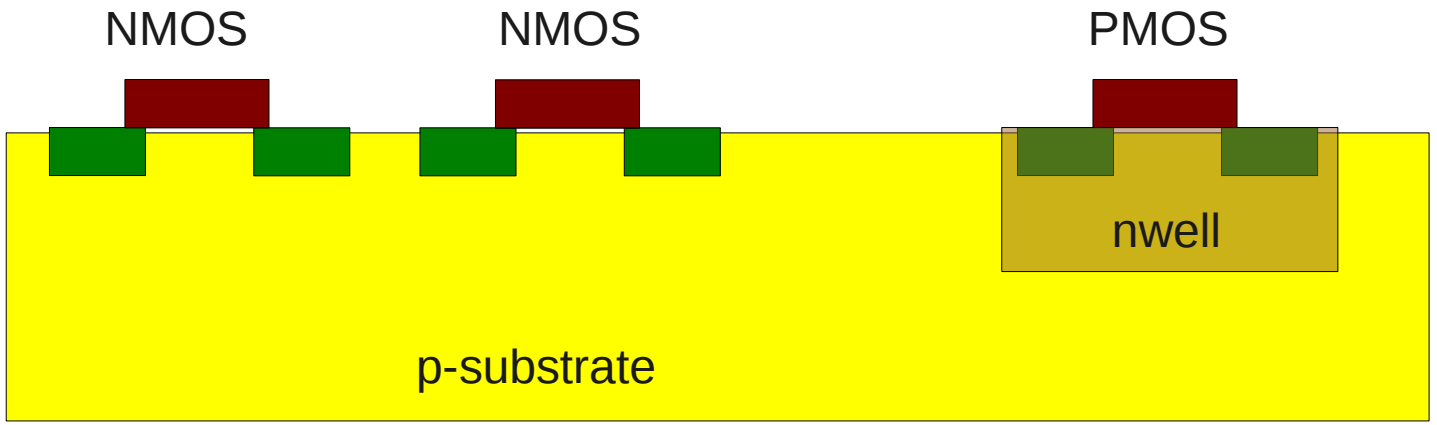


(De)-coupling

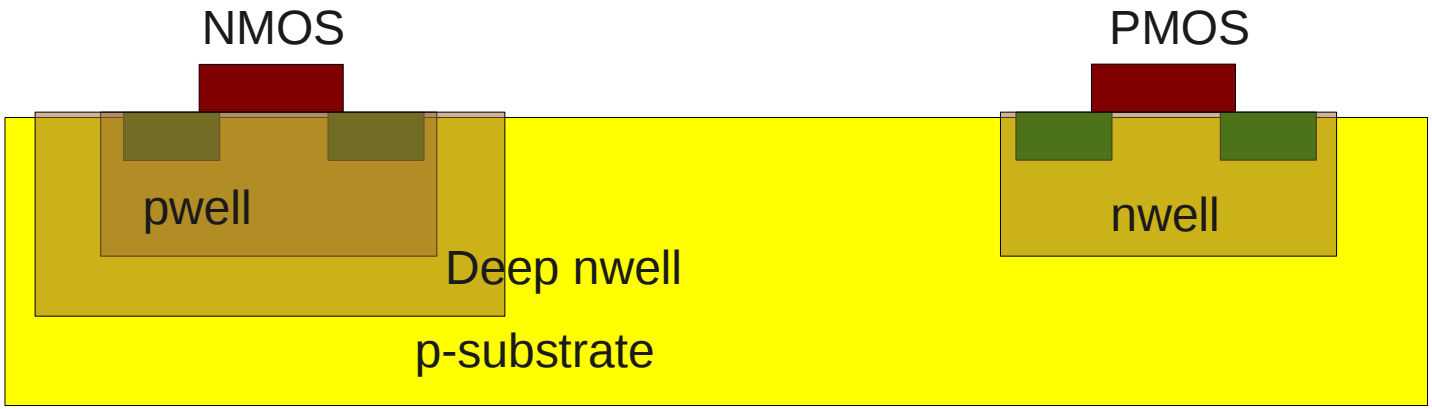


a) b) c)

Insulating (another feature of DST)



Standard nwell process



Triple well possible in very deep submicron processes (0.13 μm and beyond)

What next in high speed?

PRESSMEDDELANDE
Press release

5 October 2010

The Nobel Prize in Physics 2010

The Royal Swedish Academy of Sciences has decided to award the Nobel Prize in Physics for 2010 to

Andre Geim
University of Manchester, UK

and

Konstantin Novoselov
University of Manchester, UK

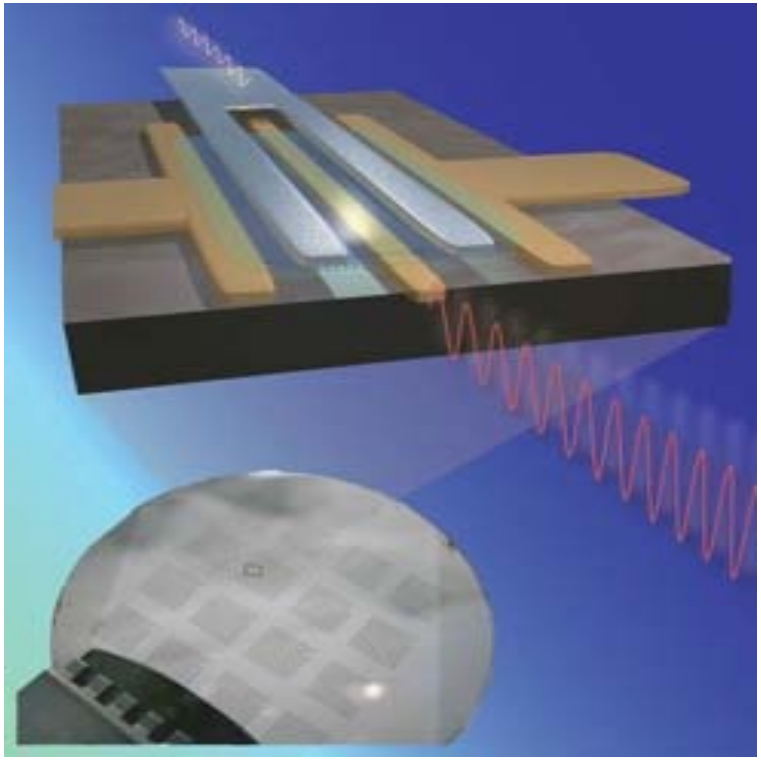
"for groundbreaking experiments regarding the two-dimensional material graphene"

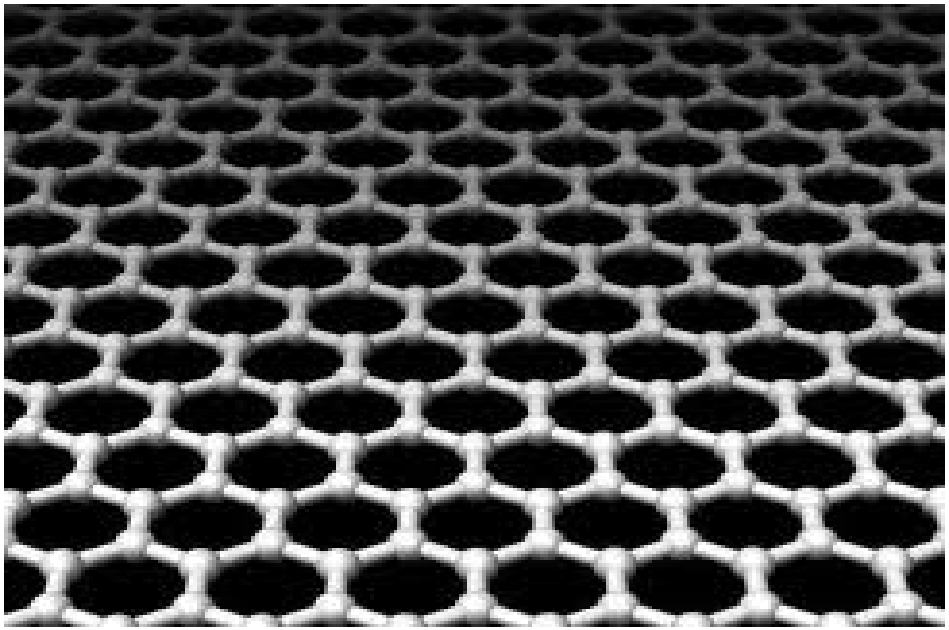
Graphene – the perfect atomic lattice

A thin flake of ordinary carbon, just one atom thick, lies behind this year's Nobel Prize in Physics. Andre Geim and Konstantin Novoselov have shown that carbon in such a flat form has exceptional properties that originate from the remarkable world of quantum physics.

When mixed into plastics, graphene can turn them into conductors of electricity while making them more heat resistant and mechanically robust. This resilience can be utilised in new super strong materials, which are also thin, elastic and lightweight. In the future, satellites, airplanes, and cars could be manufactured out of the new

What next in high speed?





- Maximum theoretical mobility: 200000 $cm^2/V\ s$ (1350 of Si)
- In practice 40.000 achieved. FT of 100 GHz demonstrated with 240 nm gate
- Symmetry between electrons and holes
- Still in its infancy....
- End of CMOS scaling around 2020, so CMOS still a good baseline choice for future detectors!