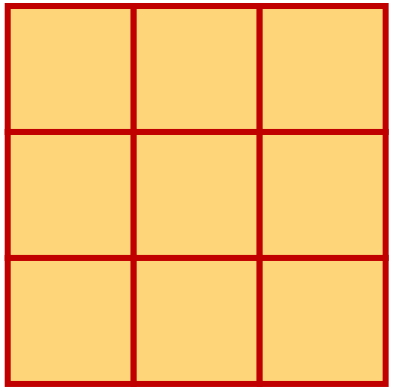
URANIA LNF MEETING – 5 Feb 2021

- Pads number
- Readout
- Example of front-end stages
- Conclusions & to do list

8 CHANNELS ARE BETTER THAN 9 …

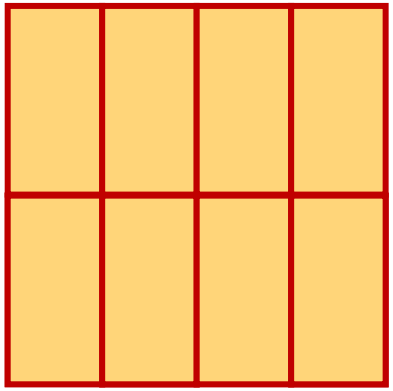
CONSTRAINTS

- Gain ≃ 500
- Primary electrons ≃ 20.000 electrons
- Charge ≃ 1.6 pC → 0,5 pC (gas gain fluctuation/geometry)
- Pad Capacitance(3x3 cm^2) ≃ 240 pF (er kapton =3)
- N. Channels: 9
- Analog outputs for external waveform digitizing



CONSTRAINTS

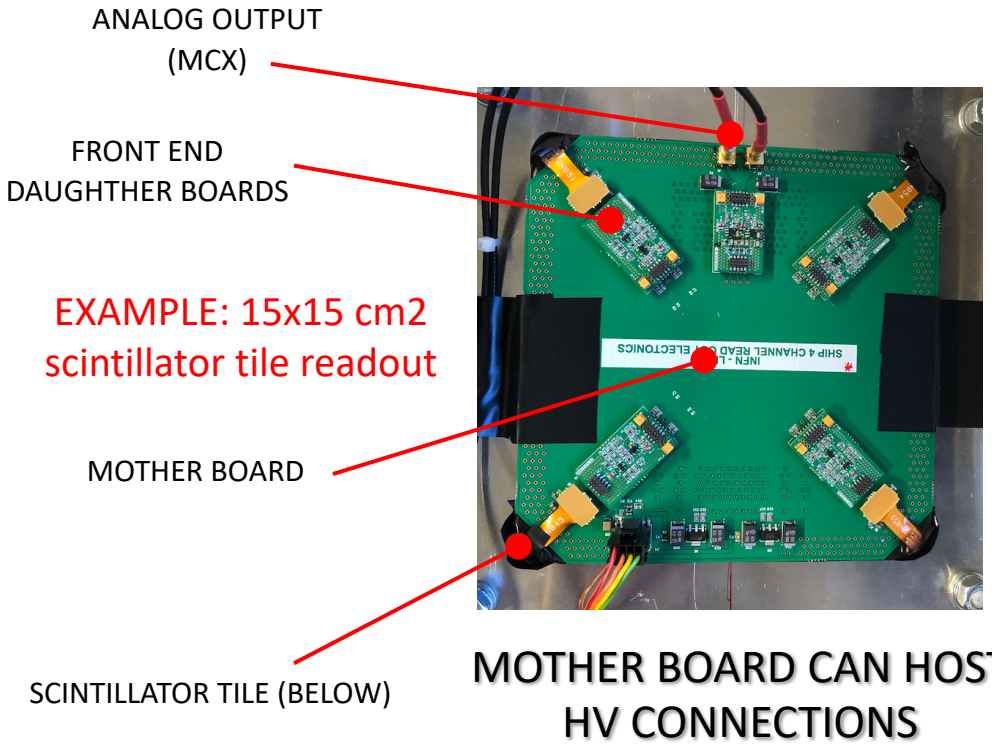
- Gain ≃ 500
- Primary electrons ≃ 20.000 electrons
- Charge ≃ 1.6 pC → 0,5 pC
- Pad Capacitance(2.5x5 cm^2) ≃ 330 pF (er kapton =3)
- N. Channels: 8
- Analog outputs for external waveform digitizing

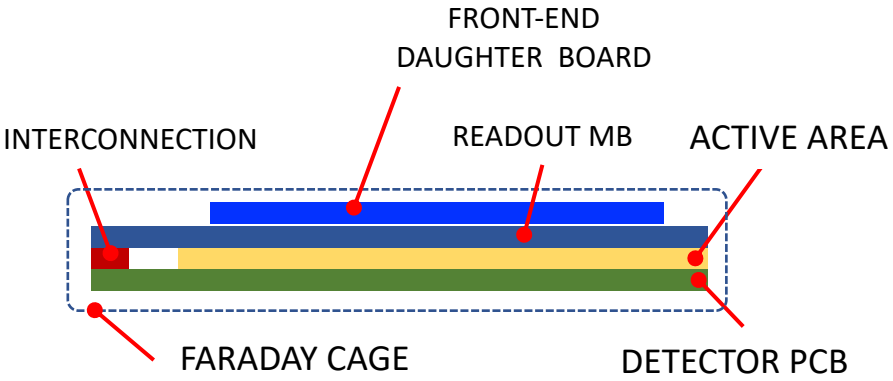


READOUT ASSEMBLING EXAMPLE

Only 8 channels --> discrete readout can be used

- Mother Board
- Front-End Daughter Boards (4 or 8 channels)
  - More expensive but more flexible

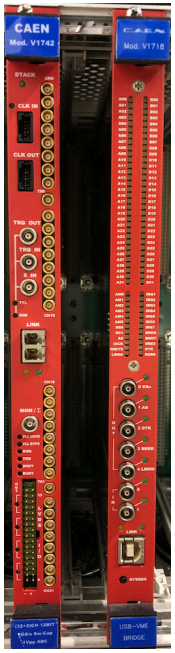




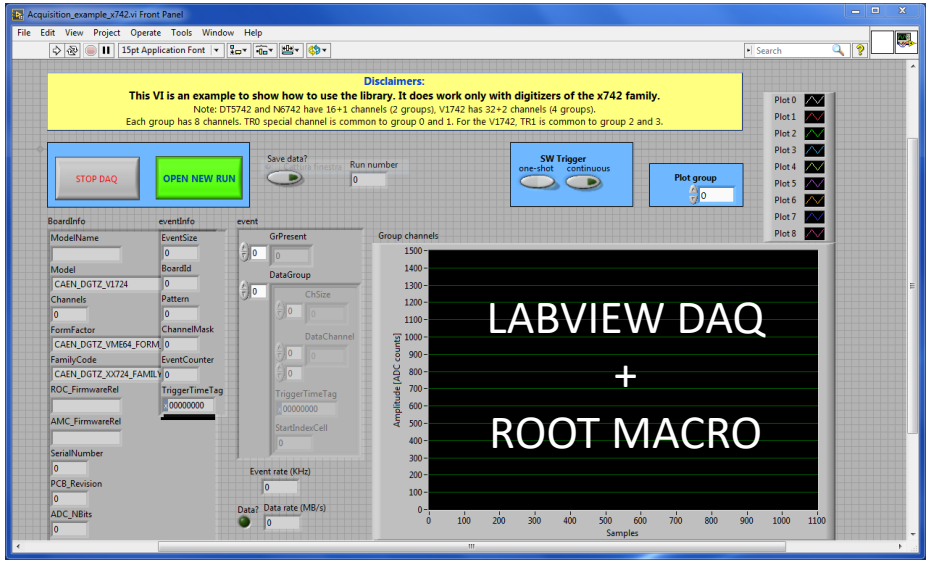
EXAMPLE: FC INTERCONNECTION PANEL

EXAMPLE: DIGITIZING CHAIN USED FOR BTF SHADOW TEST BEAM (ALESSANDRO CALCATERRA)

CAEN FADC
- V1742
- 32 + 2 chs
- 12 bits
- DRS4 BASED (1024 cells)
- 750MS/s - 5GS/s



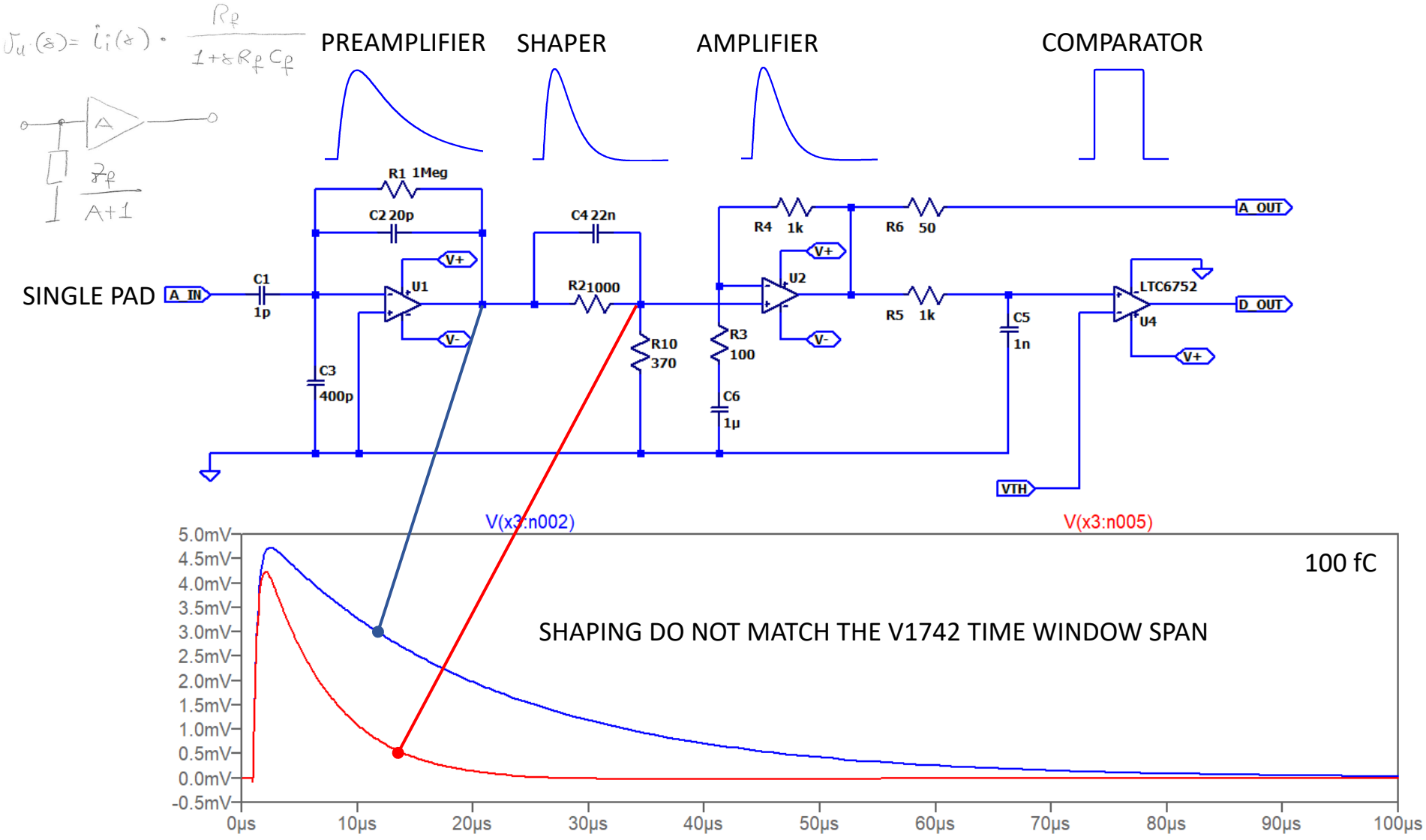
CAEN
Crate
Controller



Self-trigger, combinations of channels over-threshold in logic OR; common to couples of groups

TO BE INVESTIGATED

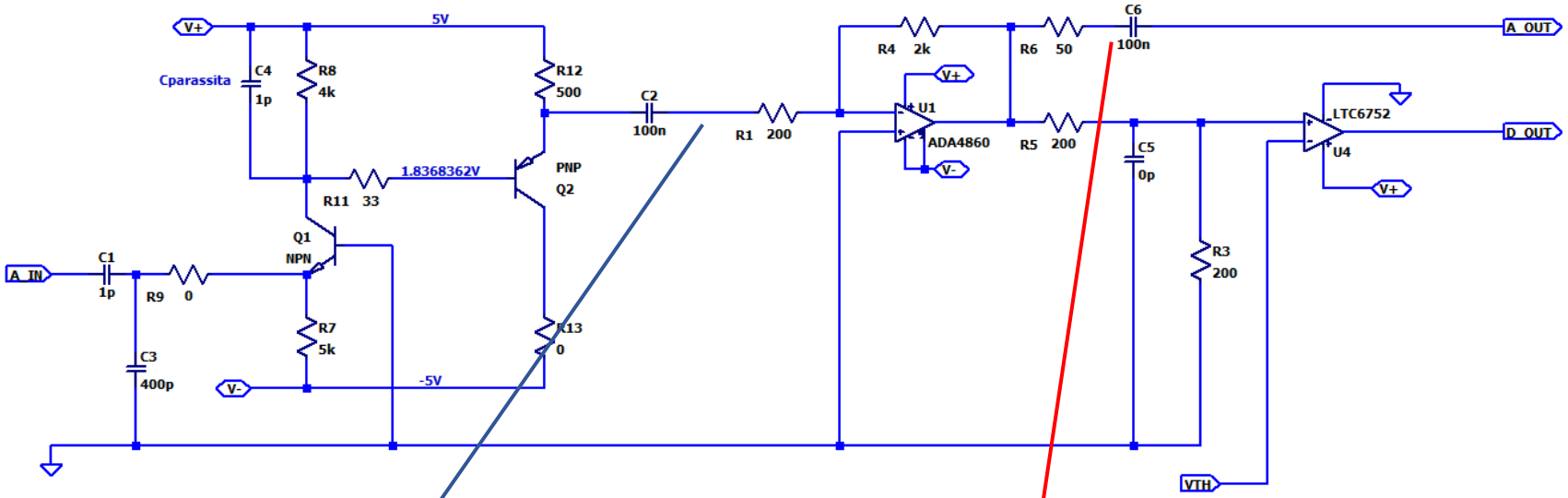
READOUT: example 1 (no noise simulation - ideal component)

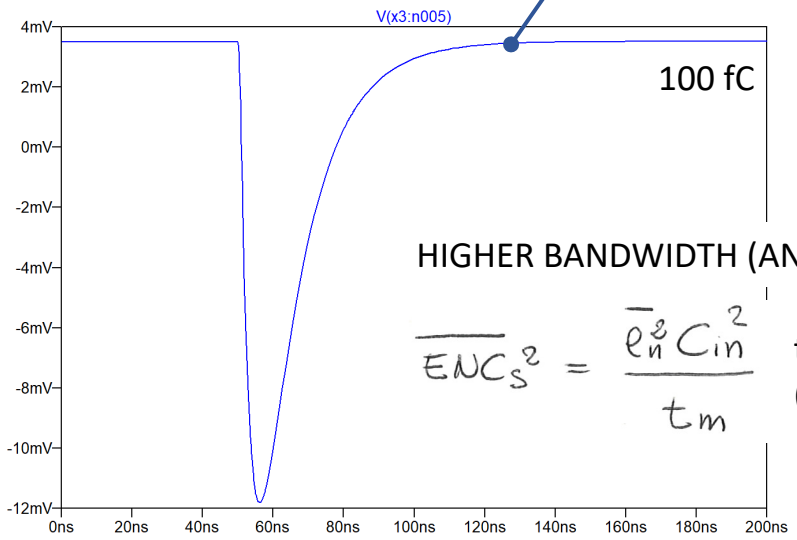


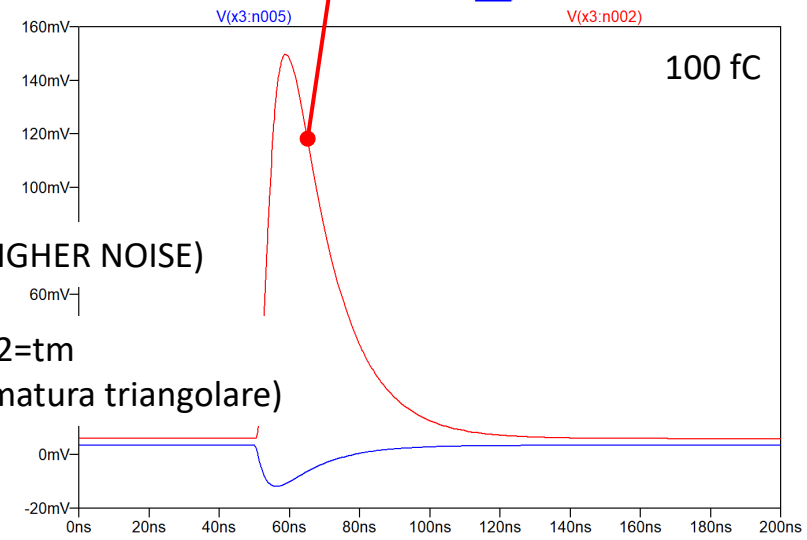
READOUT: example 2 (no noise calculation - ideal component)

$$r_{in} = 1/g_{m1} \qquad v_o(s) = i_i R_L \frac{1}{(1+s\tau)}$$

SINGLE PAD







HIGHER BANDWIDTH (AND HIGHER NOISE)

$$\overline{ENC_s^2} = \frac{\overline{e_n^2} C_{in}^2}{t_m}$$

t1=t2=tm
(formatura triangolare)

CONCLUSIONS

- 8 pads (2.5 x 5 cm^2)
- Compact readout (no interconnection wires used in sensitive area)
- Mother Board and Daughter Board readout assembling (different FE stages can be easily tested)
- If using V1742 digitized the maximum acquisition time window is about 1.6 us
- A faraday cage should be used to minimize external pickup

NEXT STEPS

- Design/Simulation/Test/Optimization preamp configuration
- Mother board - detector assembling system
- HV connections

} ASSUMING FC

DEADLINES ???????