# TimeSPOT WP4:
# Stato delle attività a Milano

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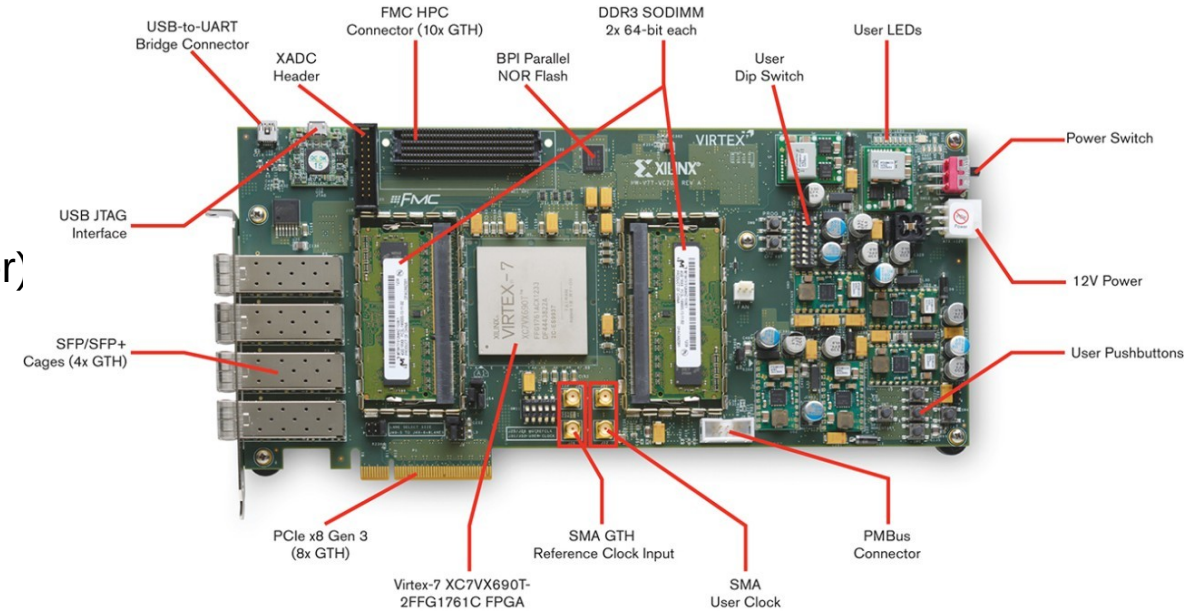
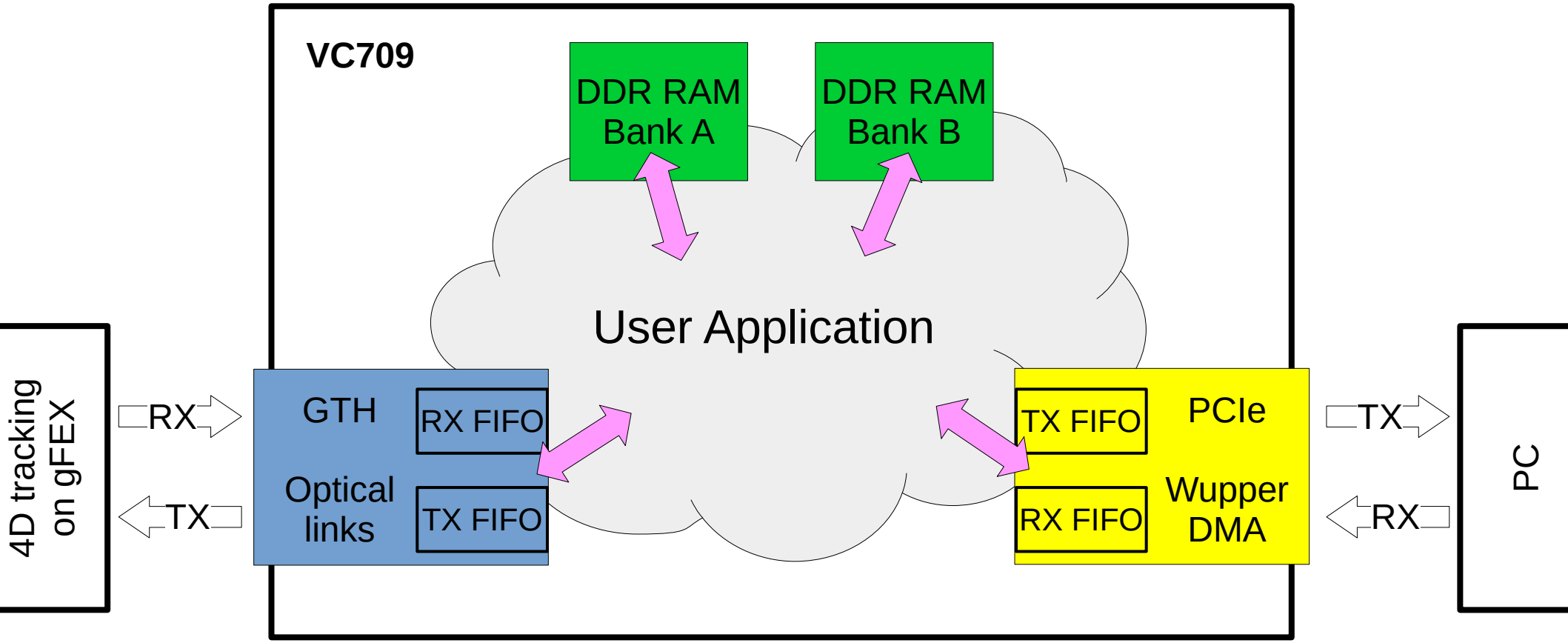
# VC709 implementation

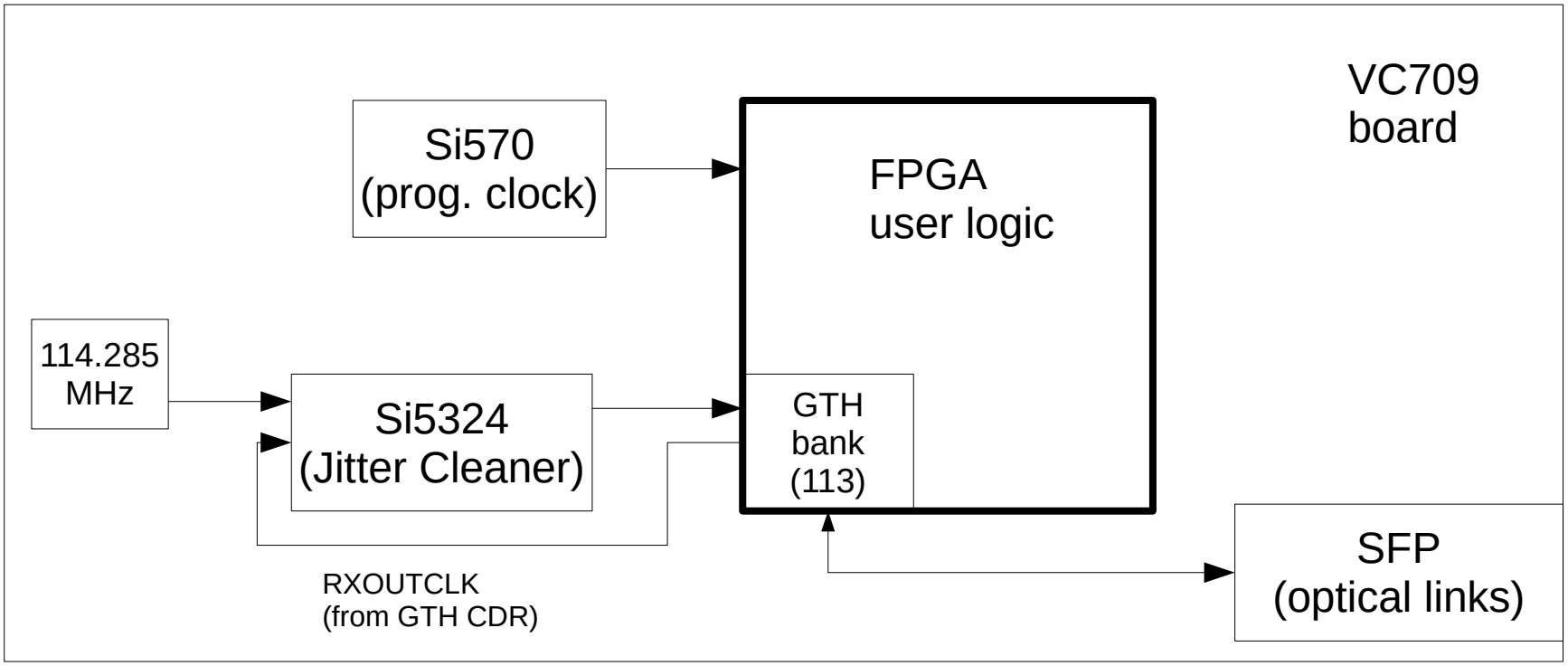
- **Three main blocks implemented:**
  - **DDR** banks (2x4GB, Xilinx MIG)
  - **PCIe** communication (using Wupper)
  - **GTH** (over optic fibers)
- An **Application** connects the three blocks and manages the data flow



# VC709 block scheme



# VC709 clocking scheme




- T**wo on-board components for clocking**:
  - **Si570**: programmable clock used as a reference for the DUT (i.e. the stub constructor)
  - **Si5324**: Jitter Cleaner, used to provide the reference clock to the GTH block

# User Guide reference

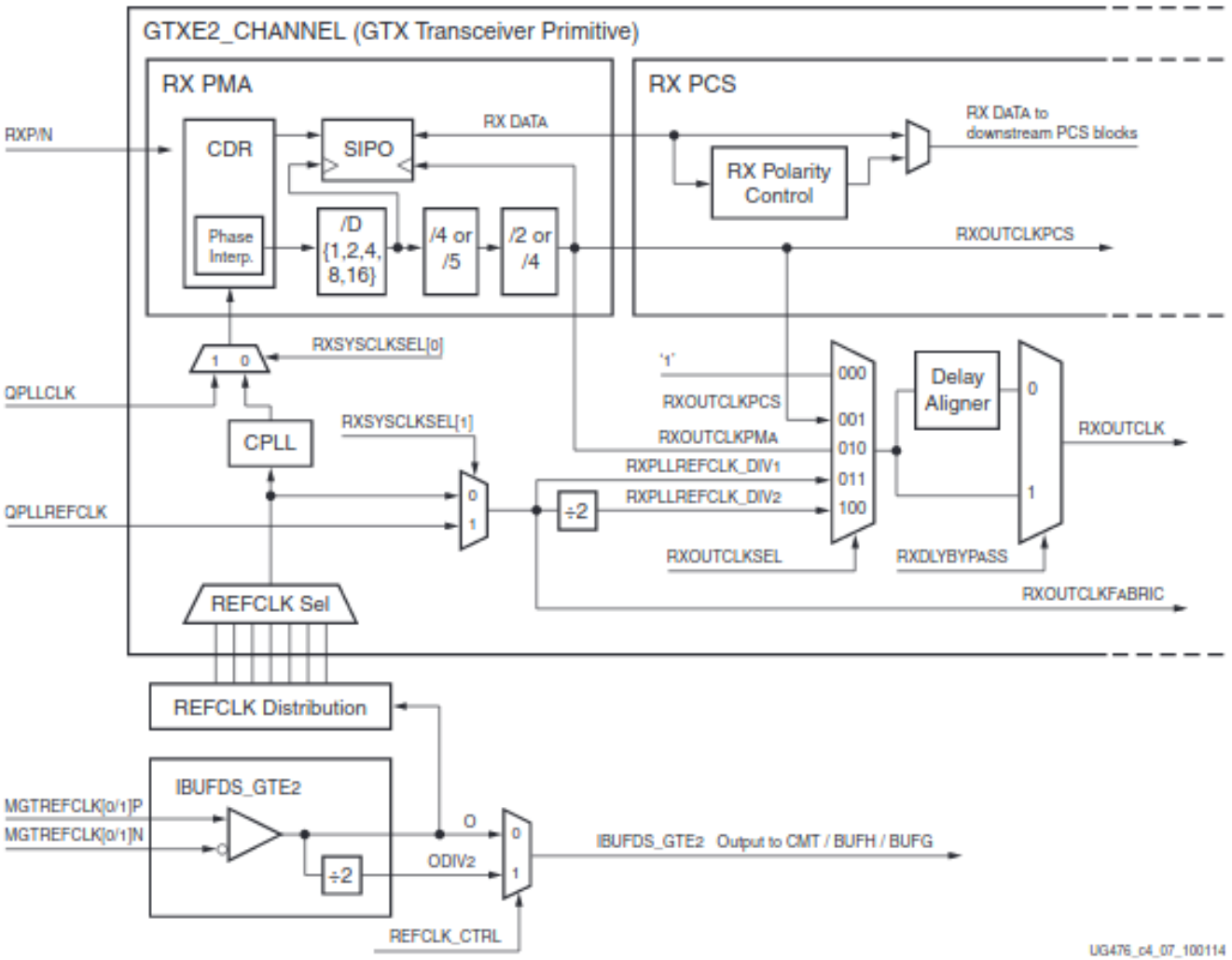



*Figure 4-23:* **RX Serial and Parallel Clock Divider**

From Xilinx User Guide 476 , pag 210

# VC709 – gFEX communication

- **Setup** of the GTH lane (on the two boards)
  - 11.2 Gbps, with 140 MHz ref.clock
  - One fiber connected from the VC709 to the gFEX and viceversa
  - Note : GTH are organized into “quads” and only one lane is used to perform the clock data recovery (CDR) and data synchronization

- **Test** performed with PRBS data:
  - **The gFEX receives the data**, and the PRBS test passes (received data are within the expected pattern)
  - **The VC709 can not “align”** to the incoming data, and the PRBS test fails

# Comments

- The GTH block in the VC709 is implemented using two different Xilinx IP-Core
  - In fact VC709 has a Virtex 7 FPGA
  - gFEX has a Virtex UltraScale FPGA

- In the gFEX implementation the GTH reference clock does not perform a loop (as the Si5324 in the VC709)
- The Si5324 “loop” is not necessary for the VC709 test in loopback mode, since the TX and the RX clocks are the same. When it receives data from the gFEX, the clock is recovered from the data (CDR)