







Kick off meeting

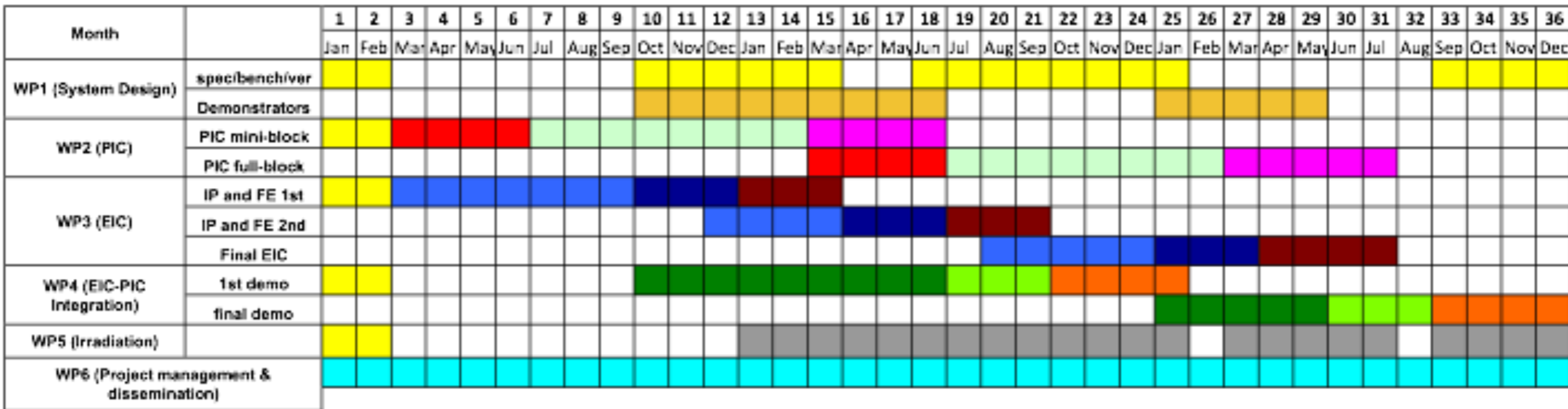
 **Benvenuti!**

 **Goals per oggi:**

-  Iniziare a definire le specifiche dei vari sottosistemi e della loro integrazione, nonché dei test
 -  Abbiamo un paio di mesi per finalizzarli, come da Gantt chart
 -  Teniamo in mente le tempistiche delle sottomissioni dei chip elettronici e fotonici (ed eventuali tempi di prenotazione)
-  Definire i lavori nei WP per i prossimi mesi
-  Logo del progetto
-  Individuare i profili e possibilmente i candidati da reclutare per gli assegni di ricerca, tenendo in conto delle tempistiche (~3-4 mesi) di reclutamento INFN

 **Contatti con il CERN e con il FNAL**

Gantt chart



- Milestones**
- M1 (Definitions of the specs and KPI) (T0+2)
 - M2 (Silicon Photonics PIC design for the submission of the mini-block chip fabrication) (T0+6)
 - M3 (1st submission of the High Speed rad-hard block design) (T0+10)
 - M4 (2nd submission of the High Speed rad-hard block design) (T0+16)
 - M5 (Final Silicon Photonics PIC design for the submission of the full block chip fabrication) (T0+18)
 - M6 (First integration EIC+PIC) (T0+21)
 - M7 (Final, large area EIC submission) (T0+25)
 - M8 (Qualification of rad-hardness of PIC and EIC) (T0+29)
 - M9 (Final demonstrator integration) (T0+32)
 - M10 (Final demonstrator qualification) (T0+36)

Work package details - I

- WP1 (System Design) defines the system specifications and key performance indicators (KPI) as inputs to WP 2 to 5 to outperform state of the art and benchmarking. Designs the final demonstrator together with WP4.
 - D1.1 System specifications and KPI (INFN PV, UNIMI) (T0+2)
 - D1.2 Demonstrator design (INFN PV) (T0+18)

- WP2 (Silicon Photonics) It will develop the SiPh building blocks including RM, MZM, bus waveguides, optical couplers and splitter, integrated thermal heaters. It will submit the MPW of a mini-block chip ($2.5 \times 5 \text{ mm}^2$). The fabricated mini-block will be characterised, providing information for the design and fabrication of the second full block chip ($5 \times 5 \text{ mm}^2$) that will be tested allowing the final integration with EIC.
 - D2.1 SiPh submissions for the MPW run of the first miniblock including the building blocks (SSSA, INFN PI, UNIFI, UNIMI) (T0+7)
 - D2.2 SiPh submission for the MPW run full final block (SSSA, INFN PI, UNIFI, UNIMI) (T0+19)
 - D2.3 SiPh final PIC characterization (SSSA) (T0+31)



Work package details - II

- **WP3 (Electronics) design of the fundamental rad-hard and high-speed electronics and test boards**
 - D3.1/3.1b Serdes (INFN PI, UNIPI, UNIMI): 1st/2nd submissions (T0+10, T0+16)
 - D3.2/3.2b Drivers and Tune circuit (INFN PI and PV, UNIPI): 1st and 2nd submissions (T0+10, T0+16)
 - D3.3/3.3b PLL/CDR (UNIPI, INFN PD and PI): 1st/2nd submission (T0+10, T0+16)
 - D3.4/3.4b Front-End circuits (INFN PV): 1st/2nd submissions (T0+10, T0+16)
 - D3.5/3.5b DAC/Bandgap (INFN PV, UNIMI): 1st/2nd submissions (T0+10, T0+16)
 - D3.6 Final large area EIC submission (INFN PV) (T0+25)

- **WP4 (EIC-PIC Integration) will develop the integration of the PIC and EIC (akaDemonstrator), together with an external company.**
 - D4.1/4.1b Prototypes and final demonstrator system (All) (T0+22, T0+32)
 - D4.2 Demonstrator tests (All) (T0+36)

Work package details - III

WP5 (Radiation hardness)

-  D5.1 Perform irradiation of the electronics and photonics dies (INFN Padova) (T0+17, T0+24, T0+30)
-  D5.2 Perform irradiation of final demonstrator (INFN Padova) (T0+36)

WP6 (Project management & dissemination)

-  D6.1 Recruit AdR (T0+5)
-  D6.2 Publish results (T0+36)

Assegni

A d R #	T y p e	Un it	Mon ths	Research Topic	Bandito/ Partenza	Vincitore
1	J	PI	30	PIC design and test. PIC-EIC integration and test	2021	
2	S	PI	24	Driver design. PIC-EIC integration and test	2020/2021	G. Ciarpi
3	J	PI	12	PLL/CDR design and test	2022	
4	J	PV	30	DAC design and test	2020/2021	
5	S	PV	12	FE design, test and integration in the demonstrator	2022	
6	J	P D	12	Irradiation tests and analysis	2022	

WP Structure

Table 3. Work Packages.

WP	Topic	Leader	Unit	Areas of work
1	System Design	Luigi Gaioni	INFN Pavia	Demonstrator design, system specifications and key performance indicators
2	Silicon Photonics	Stefano Faralli	Scuola Superiore S. Anna of Pisa	PIC blocks, Ring-Resonator Modulator, MachZehnder Modulator, WDM and SDM
3	Electronics	Gianluca Traversi (focus FE) and Guido Magazzu (focus IP cores)	INFN Pavia INFN Pisa	Serdes, Driver, PLL/CDR, DAC, Bandgap, Front-End
4	EIC-PIC Integration	Sergio Saponara	University of Pisa	Packaging and integration, thermal studies, prototyping and fabrication
5	Radiation hardness	Serena Mattiazzo	INFN Padova	Tests with X-rays, Heavy Ions, protons, neutrons
6	Project management and dissemination	Fabrizio Palla	INFN Pisa	Resource management, planning and coordination. Dissemination and exploitation of the results