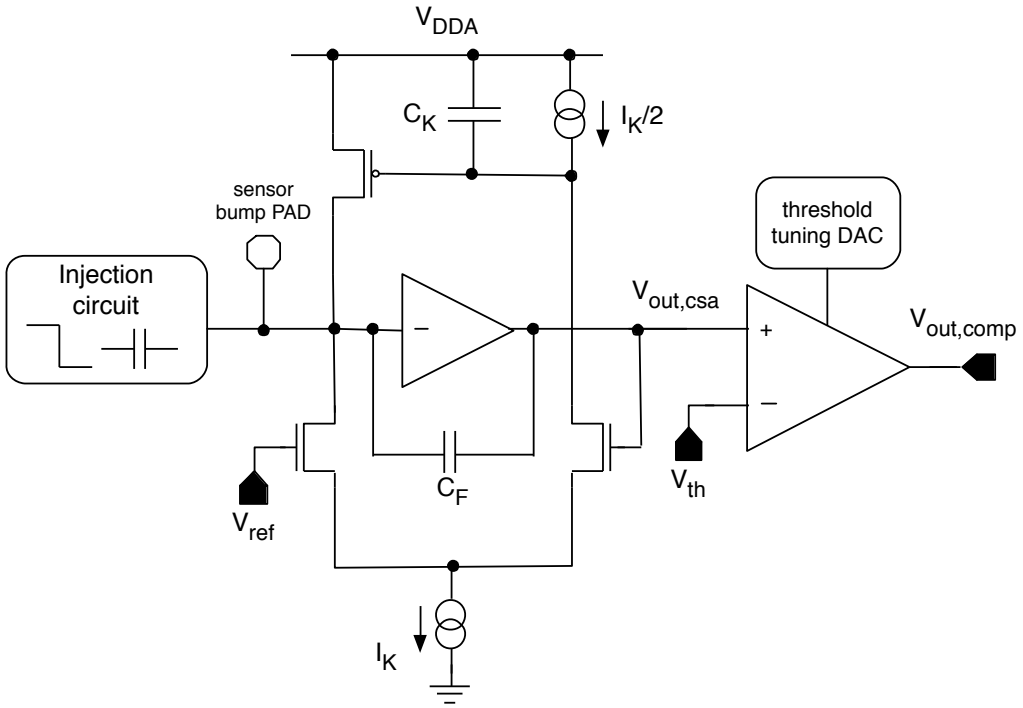
WP3 –Electronics

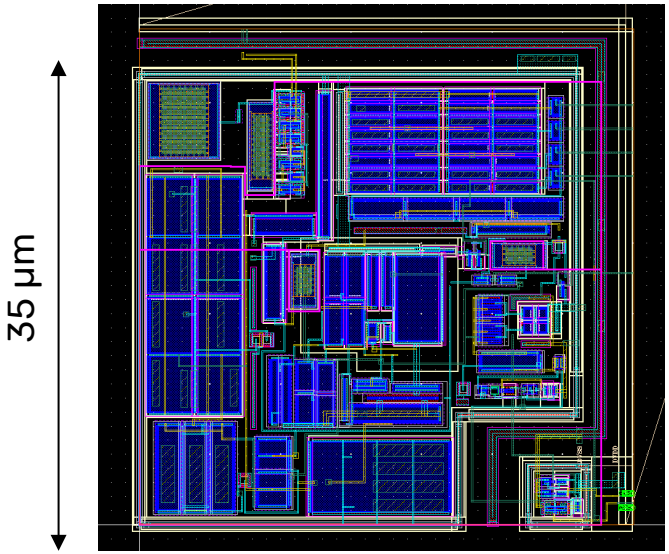
Gianluca Traversi

Kick off meeting - 15 gennaio 2020

Porting the RD53 Linear front-end in 28nm



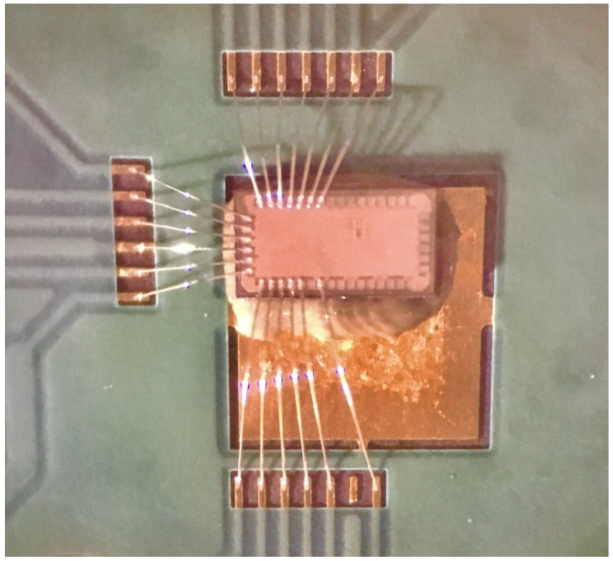
Layout for RD53A

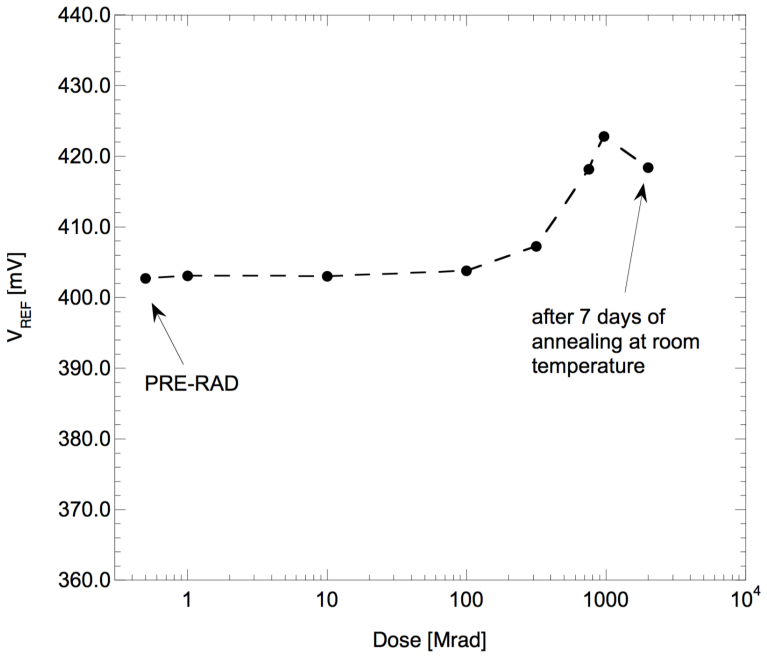


- One stage Krummenacher feedback to comply with the expected large increase in the detector leakage current
- Low power asynchronous current comparator combined with a 40 MHz Time-over-Threshold (ToT) counter for digitization of the signal
- 5 bit local DAC for threshold tuning
- Redesign of the analog front-end with the 28nm CMOS technology (target 25x25um^2 - 20x20um^2)

Building Blocks in 28nm

- A current-mode, rad-hard bandgap has been designed and characterized within the RD53 collaboration
- A modified version, able to withstand a voltage supply of 2V (with core MOSFETs only) has been developed for the SLDO circuit
- Prototypes have been irradiated up to 1Grad with moderate variation (≈ 5%) of the reference voltage
- Redesign of the BGR with the 28nm CMOS process
- The design of a trimming DAC for bias purpose is also foreseen





Schedules and Prices 2021

TSMC mini@sic	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
TSMC 0.18µm CMOS General Mixed-Signal/RF		10			12			25			17	
TSMC 0.18µm CMOS High Voltage BCD Gen 2				14						20		
TSMC 65nm CMOS Low Power MS/RF	27			14			21		22		24	
TSMC 40nm CMOS Low Power MS/RF			24							27		
TSMC 28nm CMOS RF HPC+			17			23					17	
TSMC 28nm CMOS RF HPC					26							

TSMC

Technology	Standard prices		Discounted prices	
	EUR/ min area	EUR / extra area	EUR/ min area	EUR / extra area
TSMC 0.18 MS RF (min area = 3 mm^2)	2,900	839 / 1 mm^2	2,510	798 / 1 mm^2
TSMC 0.18 BCD Gen II (min area = 4 mm^2)	4,370	947 / 1 mm^2	3,770	900 / 1 mm^2
TSMC 65 LP MS RF (min area = 1 mm^2)	3,720	310 / 0.1 mm^2	3,120	295 / 0.1 mm^2
TSMC 40 LP MS RF (min area = 3 mm^2) *	15,395	490 / 0.1 mm^2	14,626	466 / 0.1 mm^2
TSMC 28 HPC RF (min area = 1 mm^2) *	9,010	662 / 0.1 mm^2	7,240	629 / 0.1 mm^2
TSMC 28 HPC+ RF (min area = 1 mm^2) *	9,010	662 / 0.1 mm^2	7,240	629 / 0.1 mm^2

Important notes: This is a new flexible pricing with reduced minimal area.
The prices are area based, and the aspect ratio is free to choose but it is strongly recommended not to have sides less than 1mm.
Design registration must be done at least **3 months** in advance, preferably at the moment of reservation.
* The areas in the table for 28nm and 40nm are on-silicon dimensions. This means the designed area can be (area/0.81).