Status of MSD subsystem

FOOT EXPERIMENT

Keida Kanxheri (on behalf of the PG group) – FOOT Physics meeting

INDEX

- MSD architecture
- MicroStrip detectors development state
- Module construction and Mechanical assembly status
- ADC Board
- MSD DAQ firmware status
- Merging MSD firmware with central DAQ firmware
- First data acquisition (no detector on DAQ chain)
- Trigger board
- Conclusions and future steps

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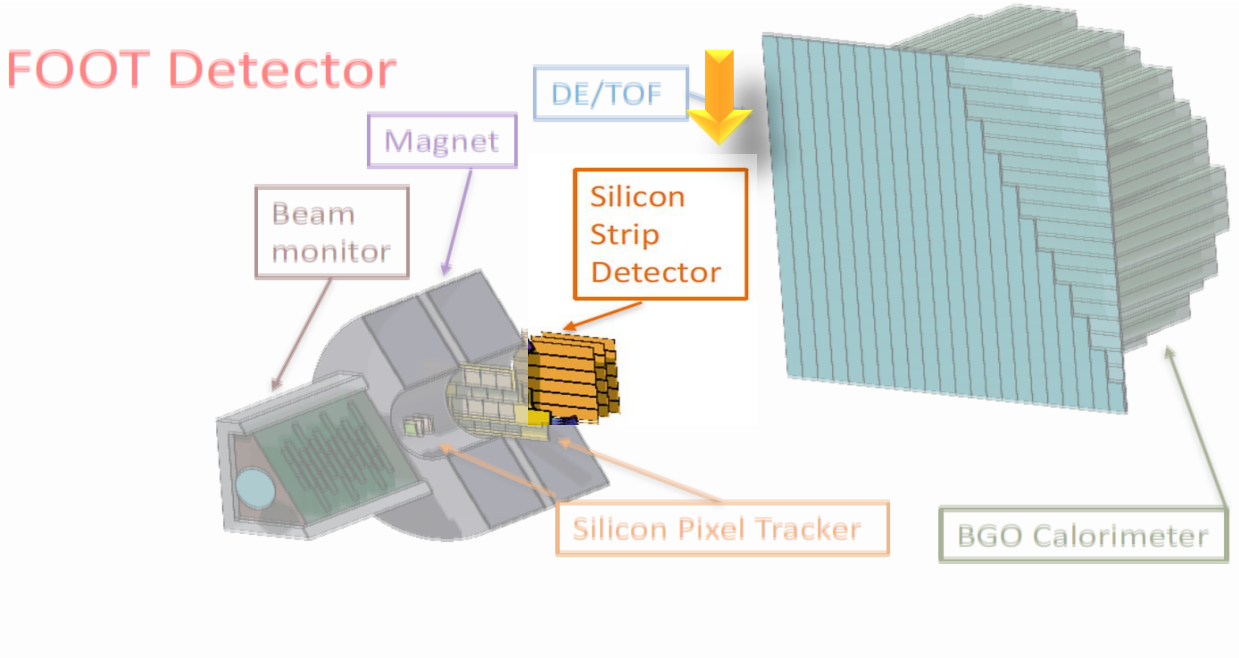
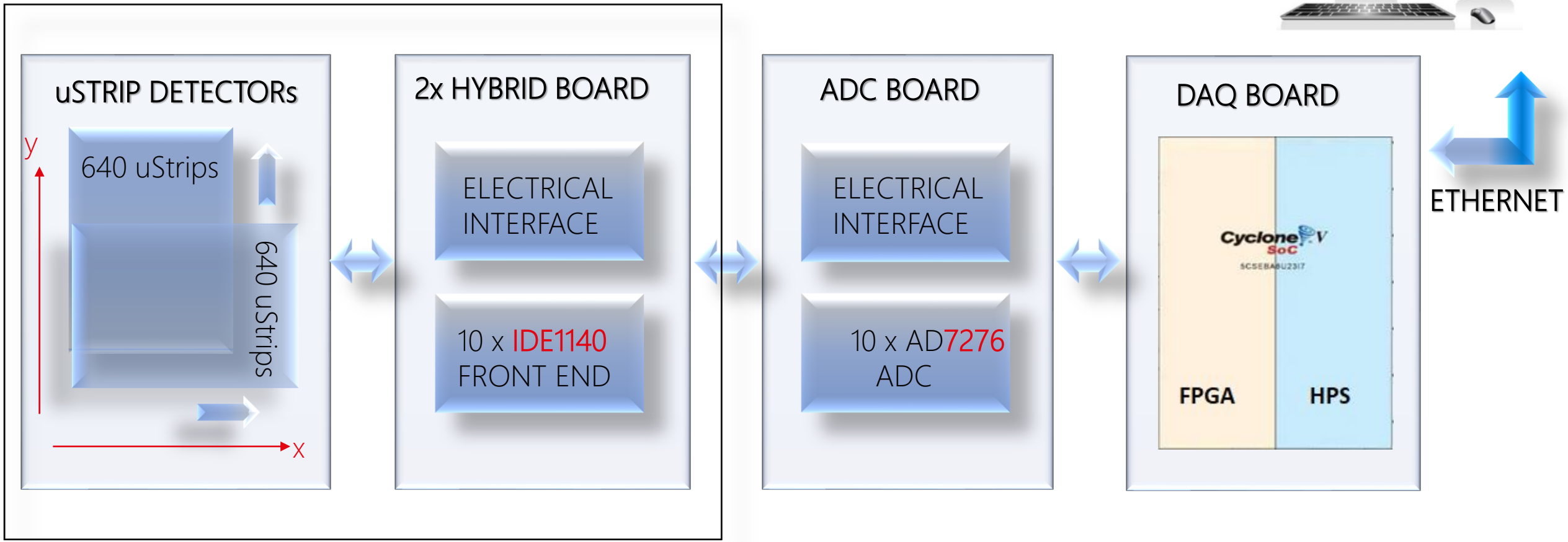
F. Peverini



MSD DAQ ARCHITECTURE

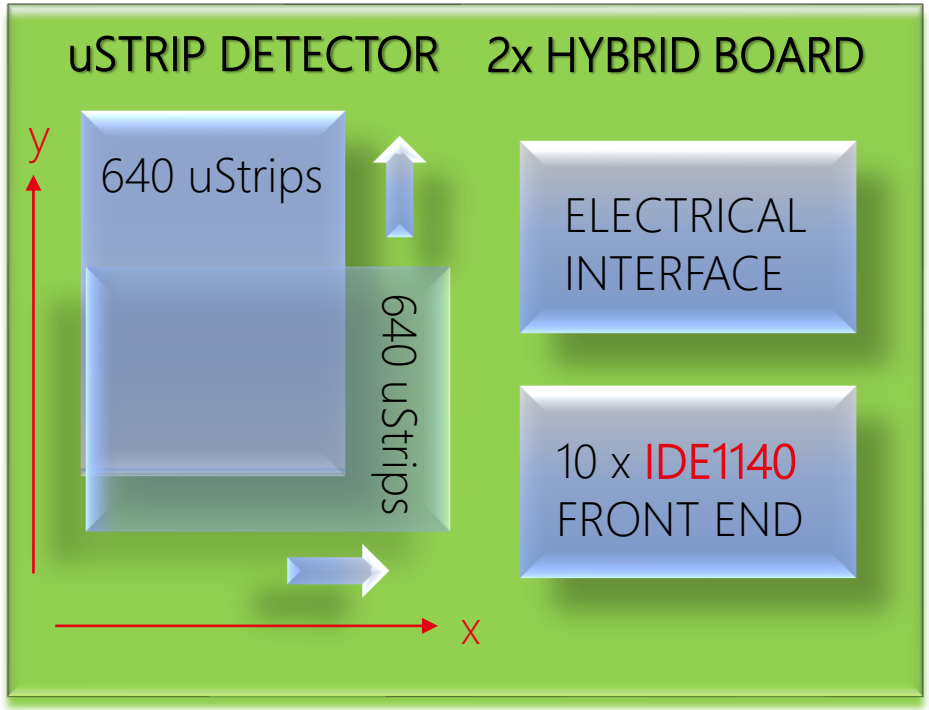
DAQ schematic view

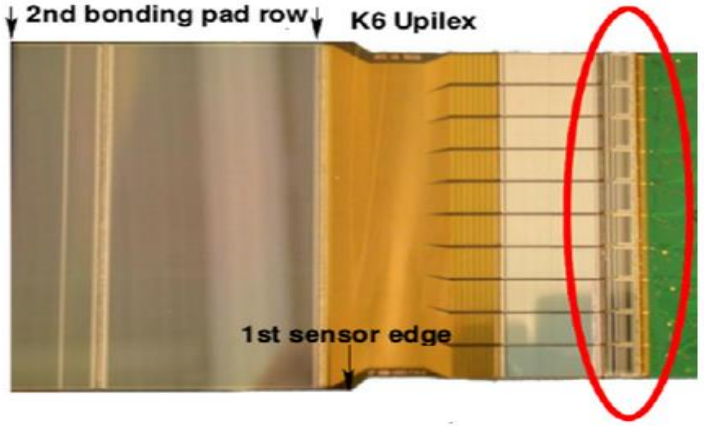


uSTRIP DETECTORs

HYBRID BOARDs

150 um thick Hamamatsu sensor with 640 strip





The IDE1140 is an application specific integrated circuit (ASIC) for the readout of silicon strip radiation detectors.
The IDE1140 is equivalent to the VA140

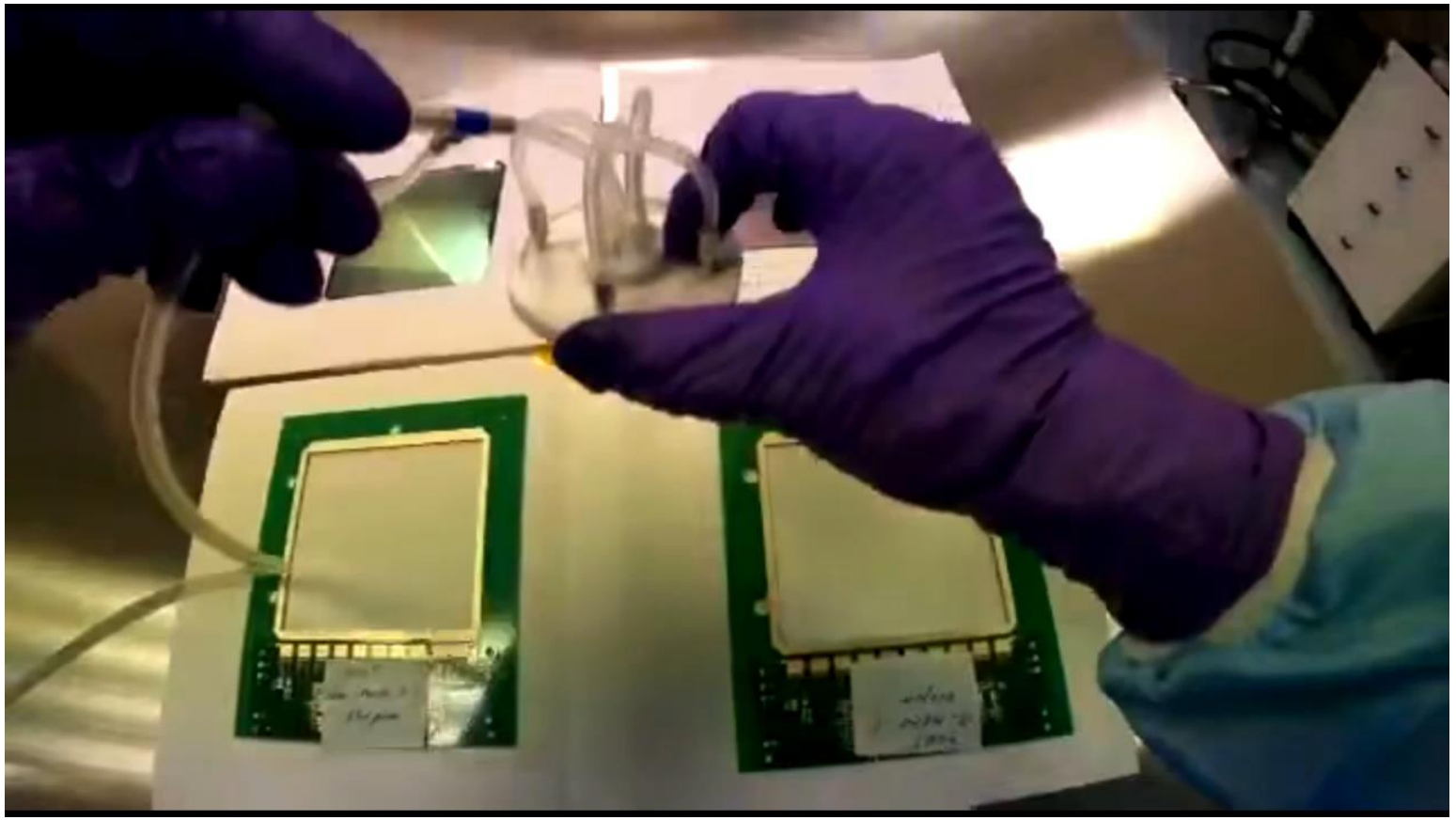
Si-strip readout with 64 Channel FE with Analogue Mux Output (10 FEs are needed for a microstrip plane)

- Serialize the data and shift the analog output into the ADCs

HYBRID BOARD

HYBRID BOARD WITH uSTRIP DETECTOR

Mounting the detector on the hybrid board and microbonding the IDE1140



uSTRIP DETECTORS

SOME STEPS OF THE MECHANICAL SUPPORT ASSEMBLY

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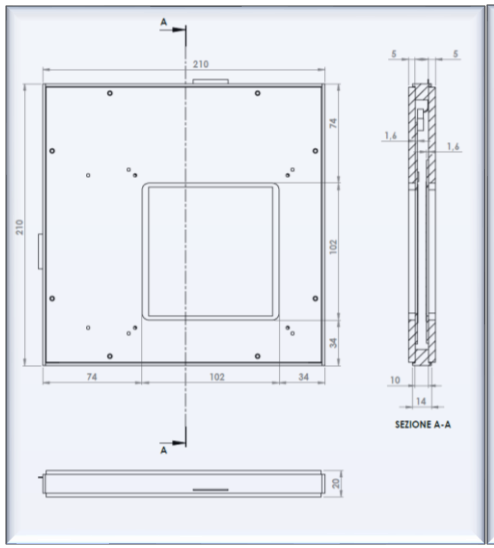
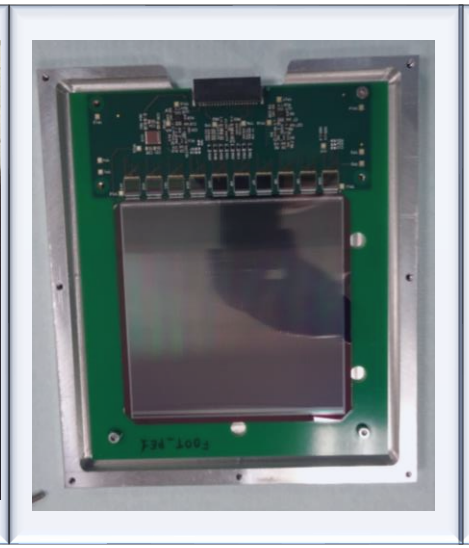
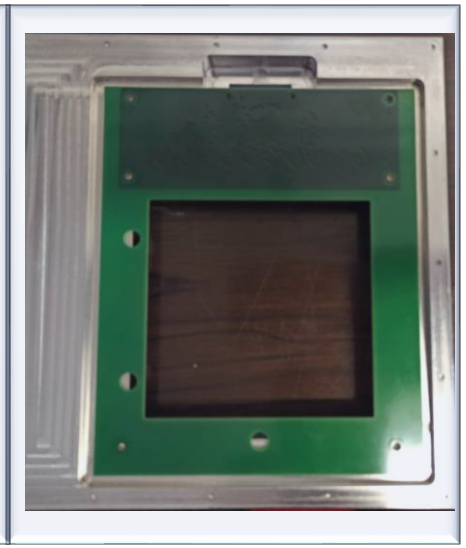
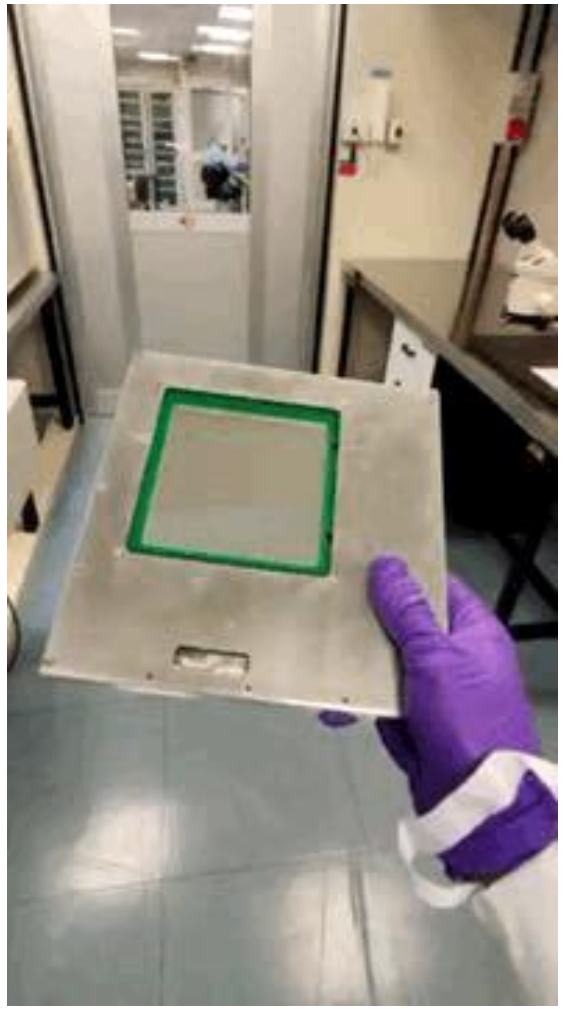








BOARD Dimensions: 13.5 cm x 16.5 cm

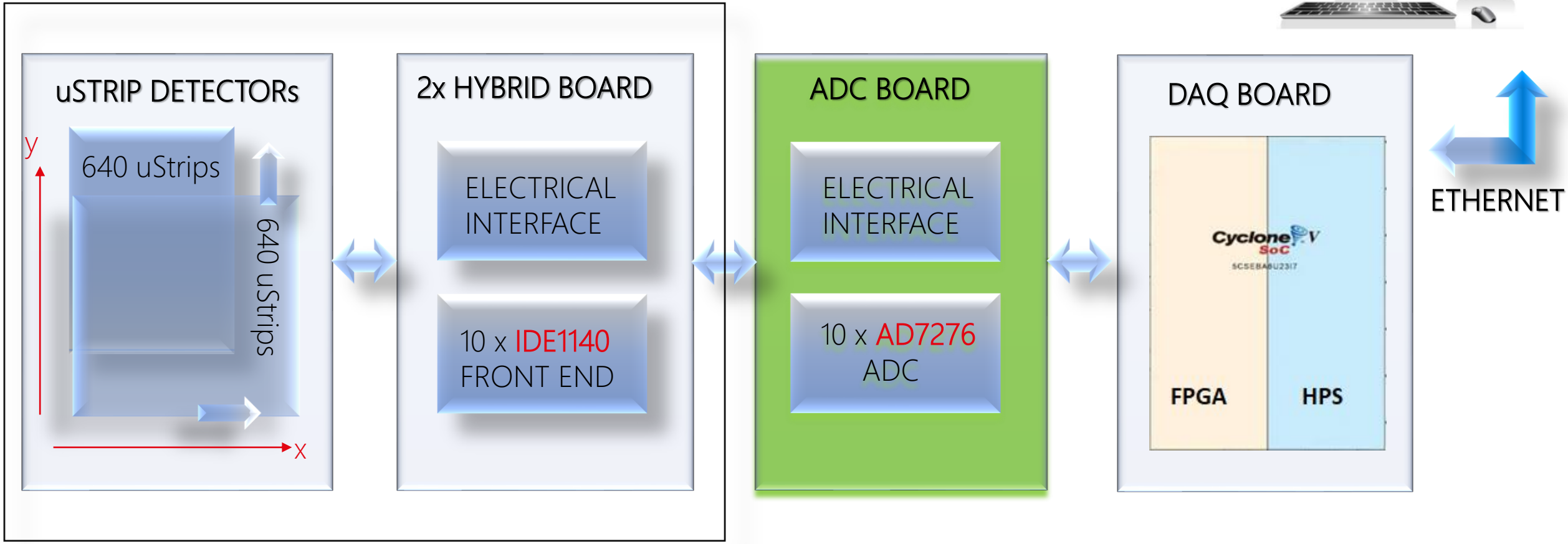
BOX Dimensions: 21 cm x 21 cm x 2 cm

Metalized sides of the detectors on the outside of the box

→ No additional material in the ion's path

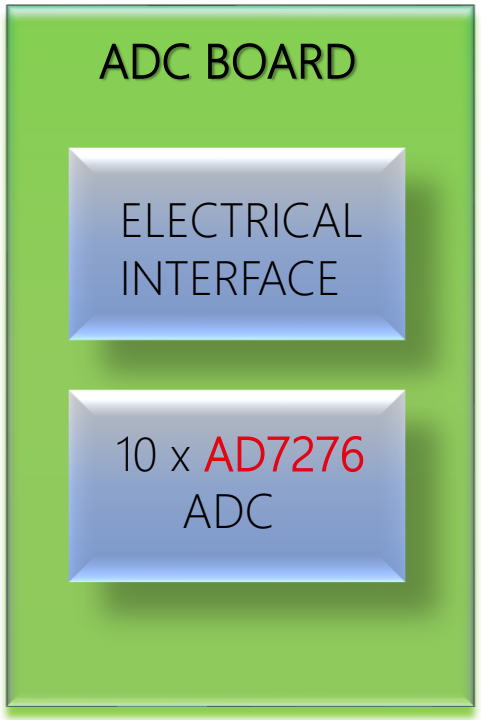
MSD DAQ ARCHITECTURE

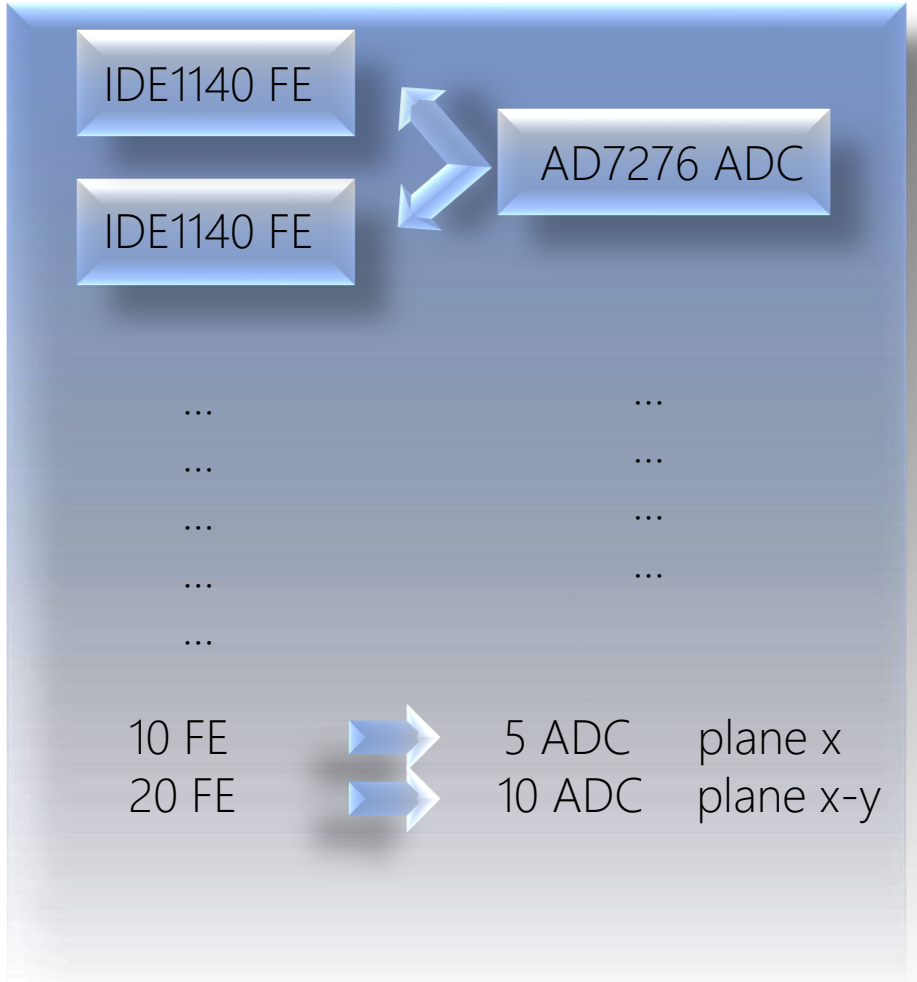
DAQ schematic view



DAQ ARCHITECTURE

ADC BOARD MORE DETAILS





AD7276 ADC

- 12-bit low noise high power successive approximation ADC
- Throughput rates up to 3 MSPS
- 5 ADCs in parallel to cover a microstrip plane, one for each subset of 2x FEs, 640 words of 16 bit (12 bit without zeros)
- In order to read an x-y plane -> 10 ADCs

MSD EVENT SIZE

128 x 2 Byte-> 256 Byte/event for a single ADC
1280 Byte/coordinate event (x plane)

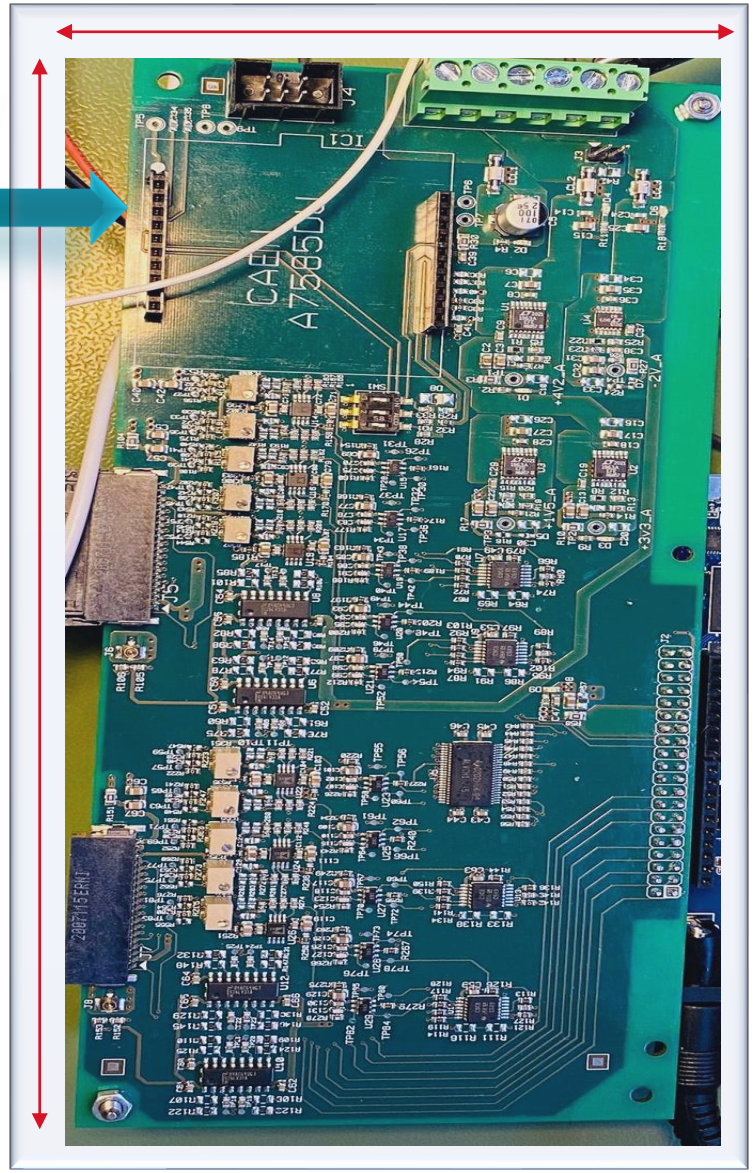
2560 Byte/event for an x-y plane

About 8kByte of data for a single event readout in 3 x-y planes

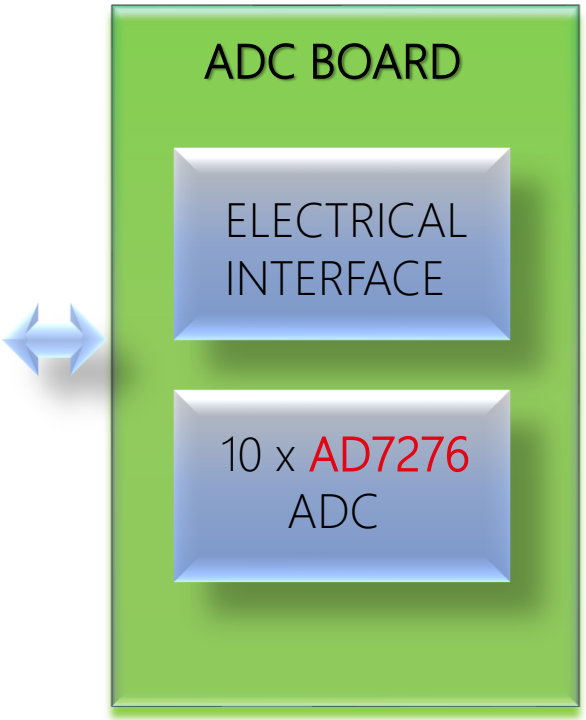
DAQ ARCHITECTURE

ADC BOARD

Daisy chain to bias control (Arduino)



Board dimensions: 9 cm x 21 cm



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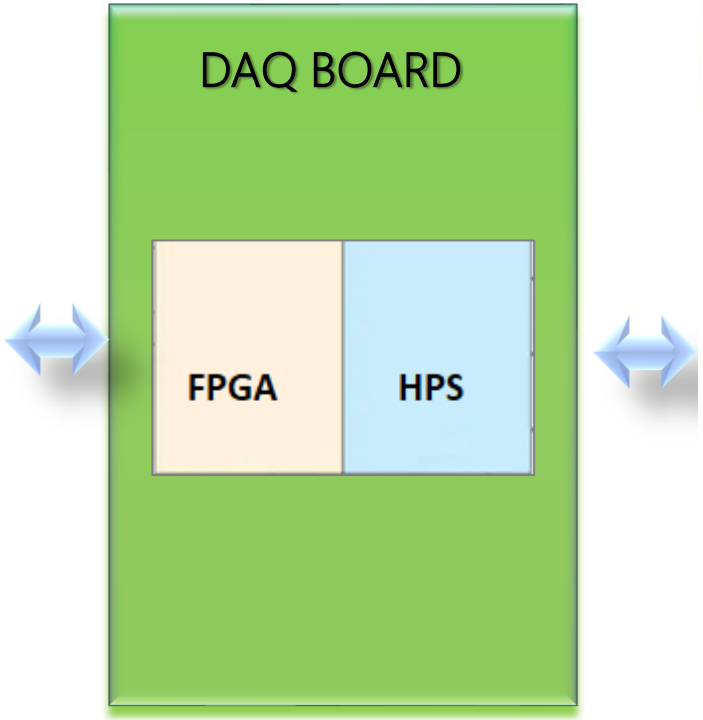
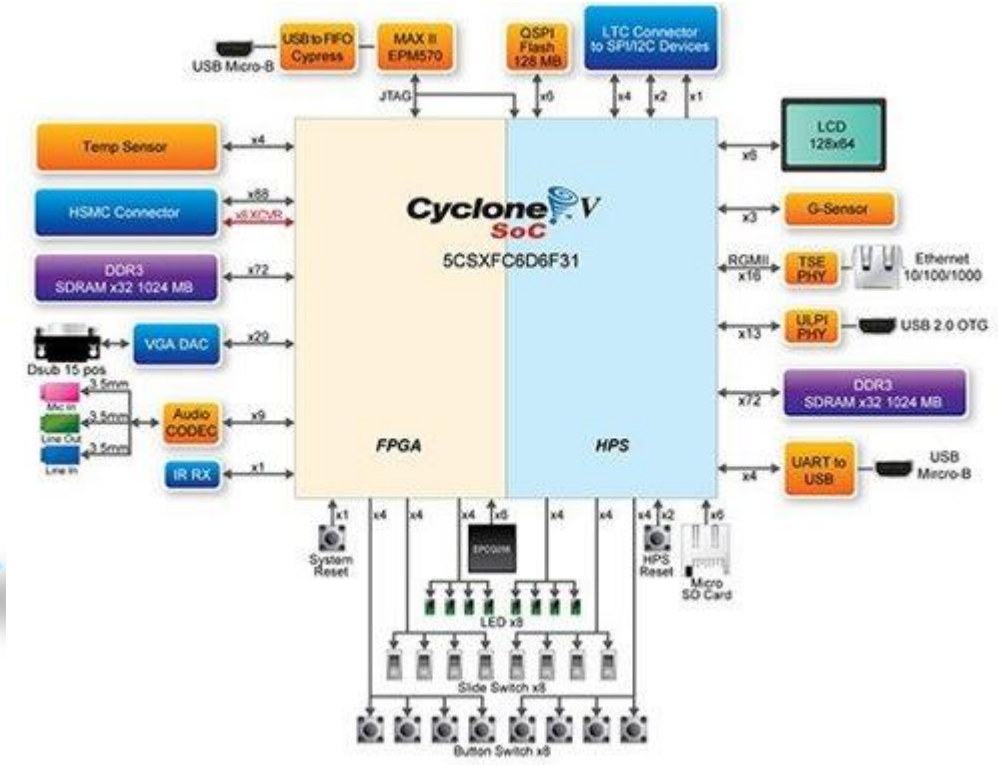
DAQ BOARD

DE10 NANO

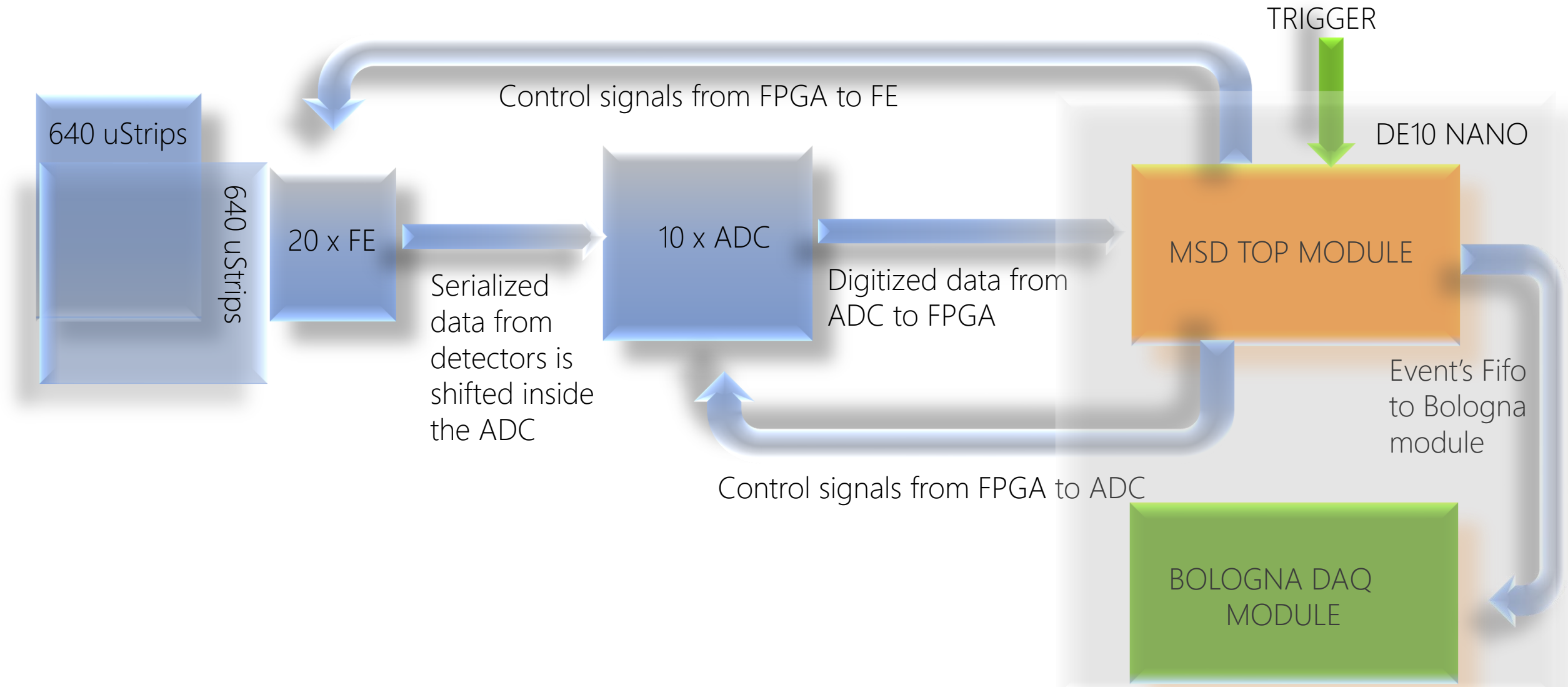




Commercial System-on-Chip board
- A Hard Processor System (HPS) and an FPGA
- Dual-core ARM Cortex-A9 & Intel Cyclone V FPGA

MSD FIRMWARE

DATA FLOW SCHEMATIC DESCRIPTION FOR AN x-y PLANE



MSD FIRMWARE

DE10 NANO SOME MORE DETAILS

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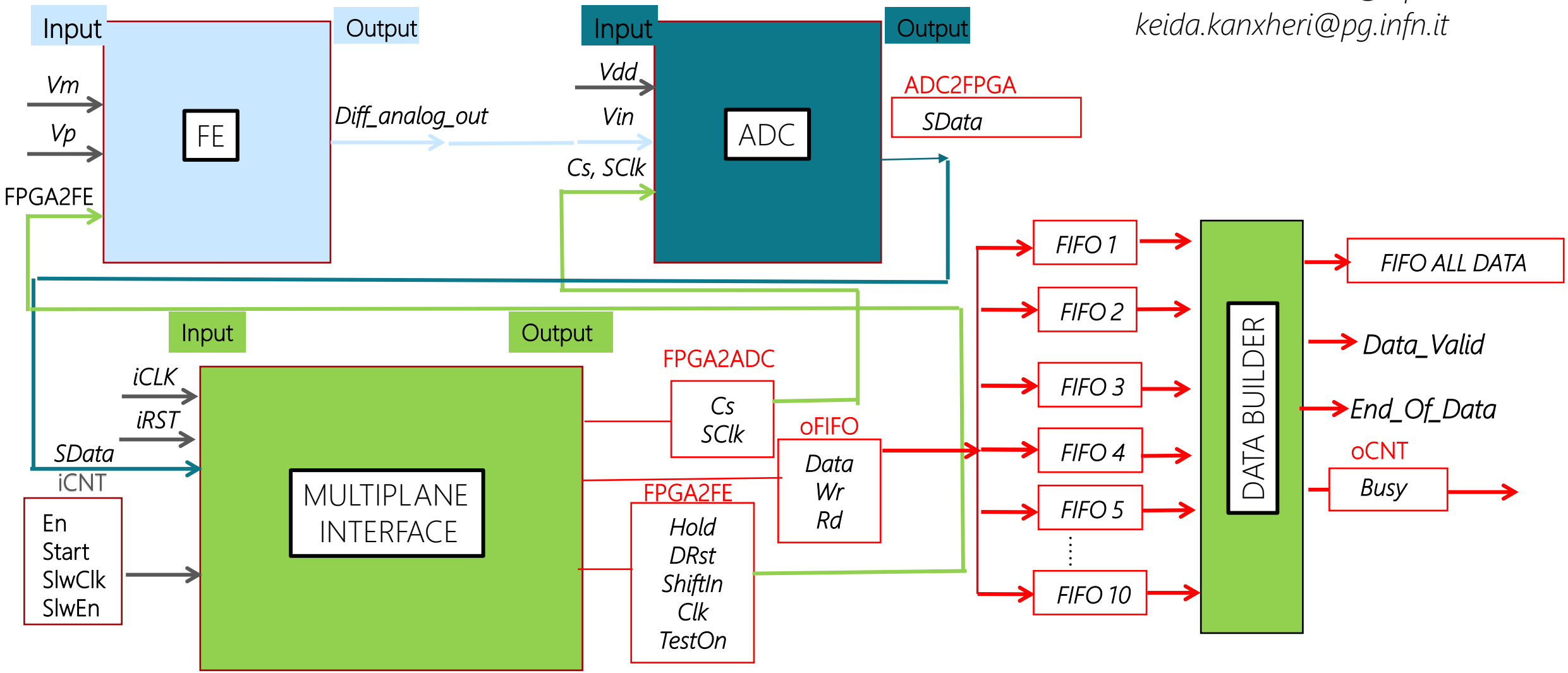
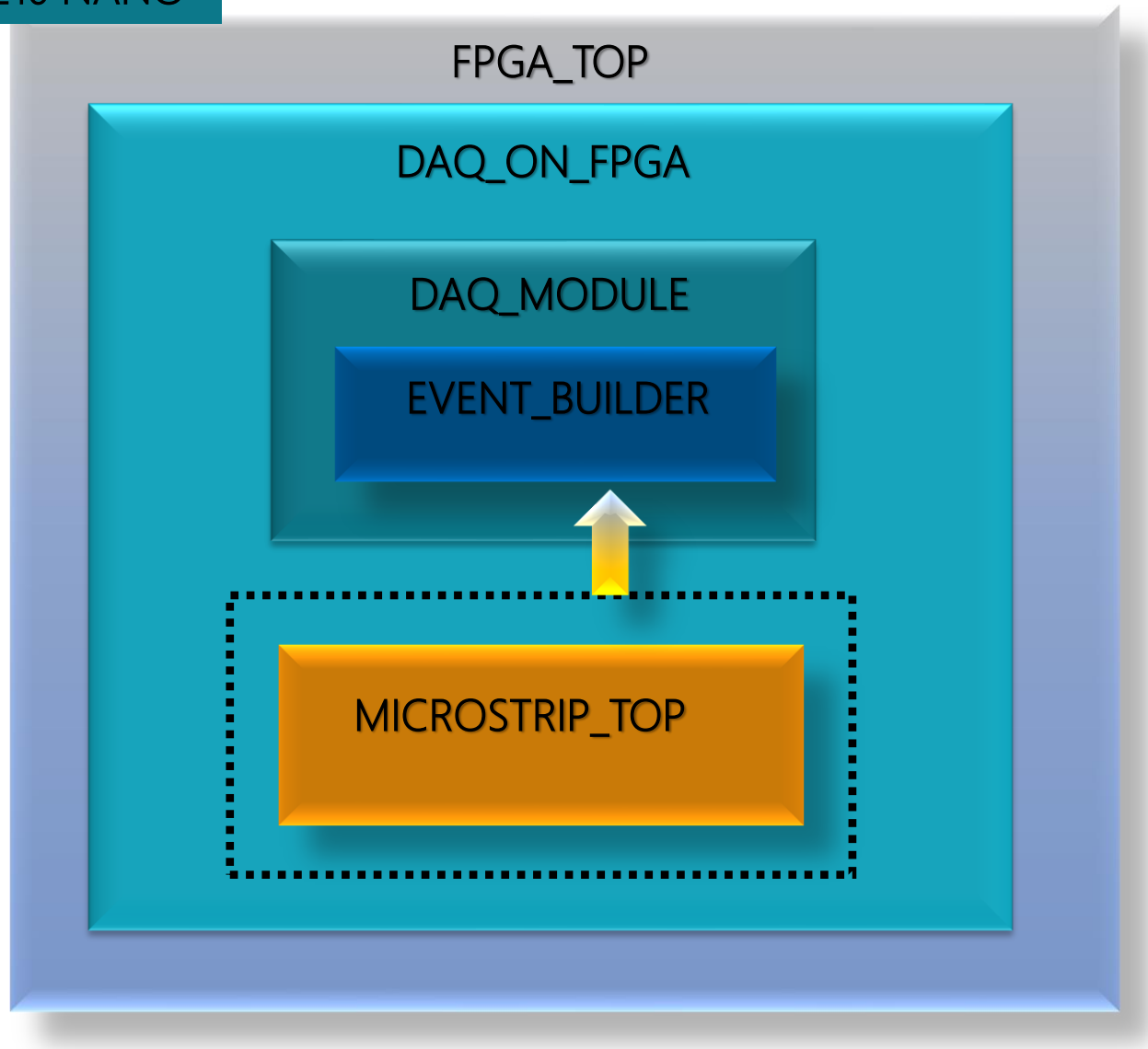


DAQ BOARD MERGING SYSTEMS

DE10 NANO

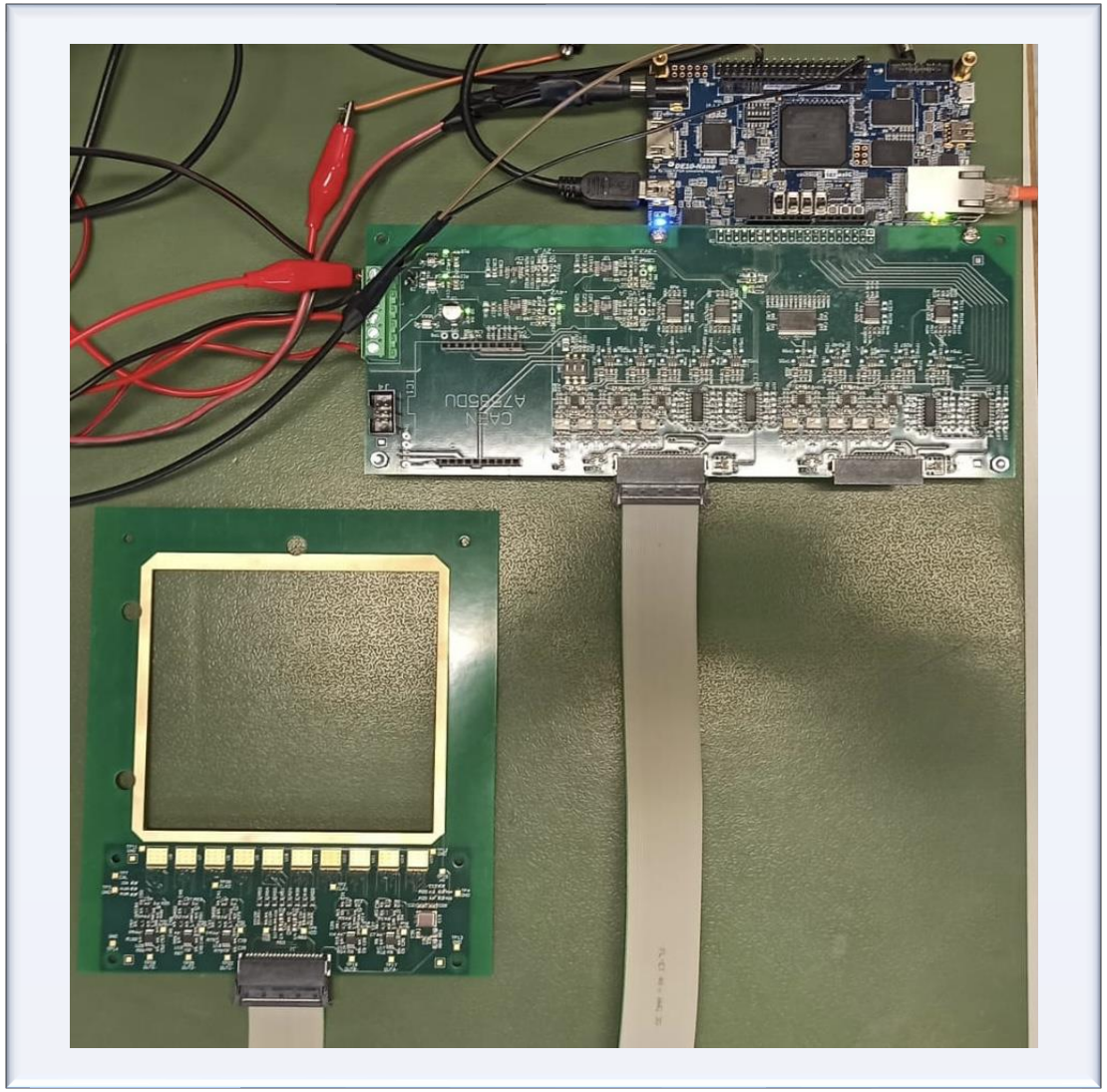


The microstrip_top entity contains all the control signals to the ustrip detector interface and the logic to obtain and deliver the digitized data to the rest of the bologna group daq system.

The outputs of the MICROSTRIP_TOP module were adapted to the inputs of the EVENT_BUILDER module.

DAQ ARCHITECTURE

DE10 NANO



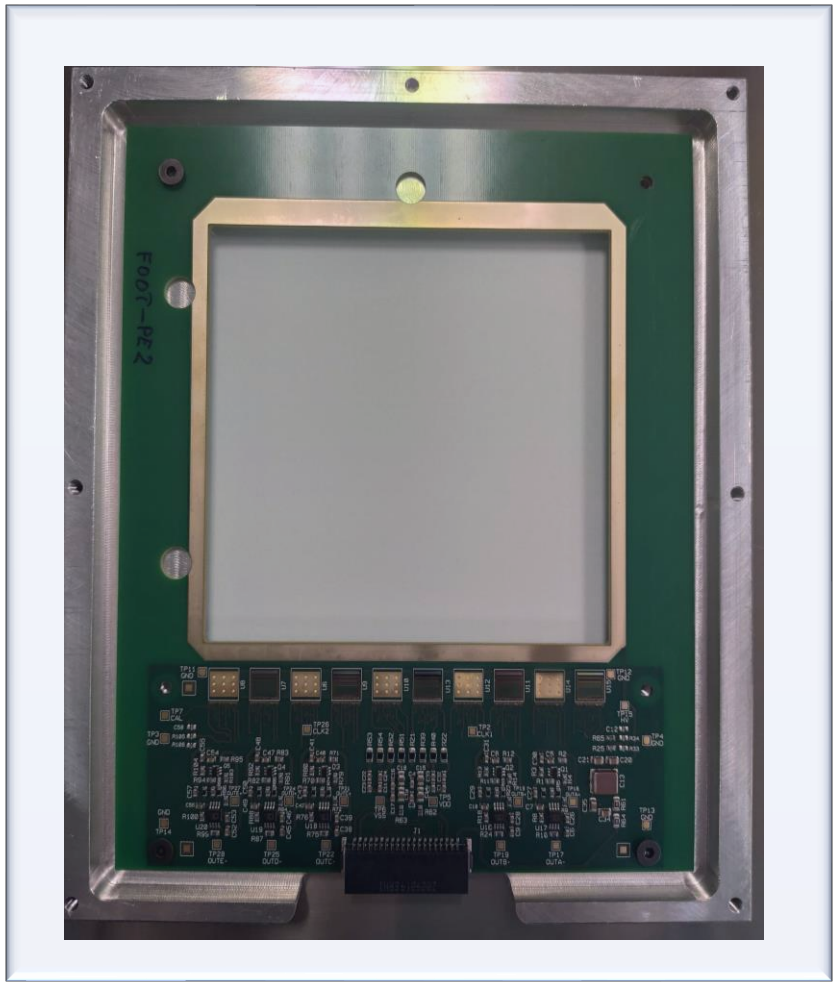
ETHERNET

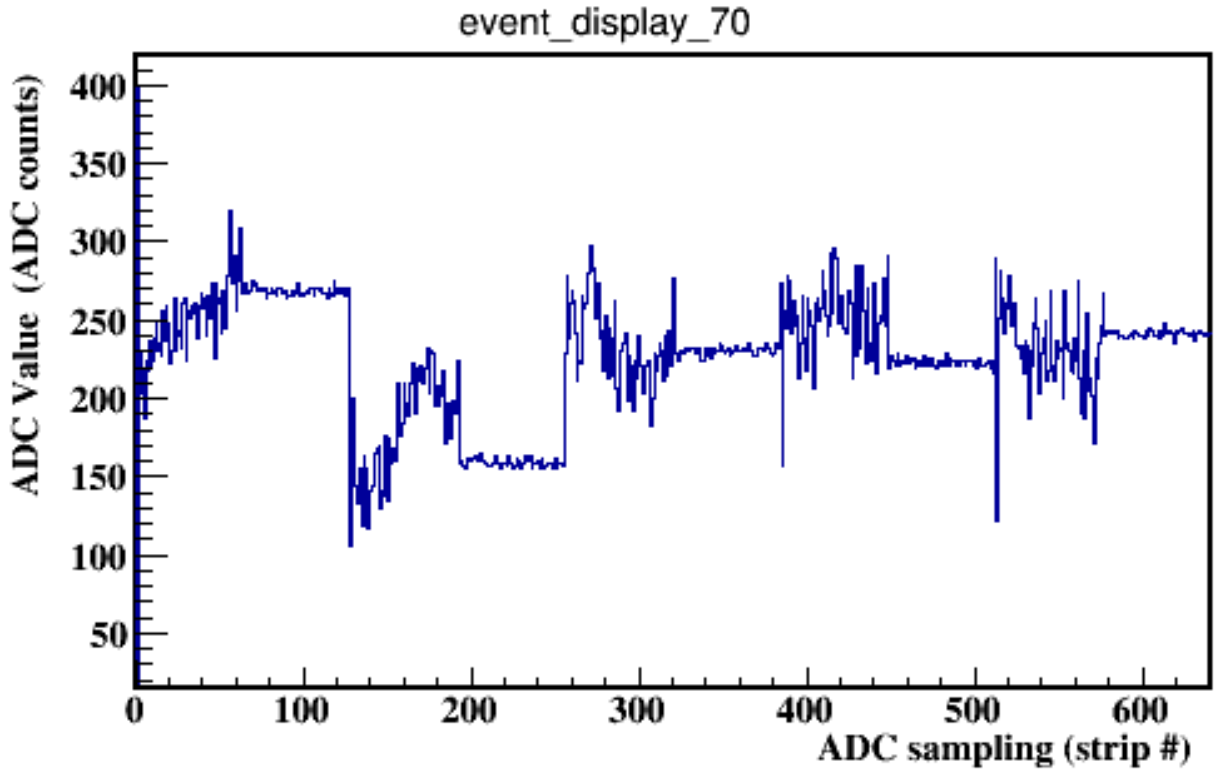
First acquisitions with the DAQ software under the guidance of :

Mauro Villa
Silvia Biondi
(Bologna group)

FIRST DATA ACQUISITION

5 ADC OUT WITH HALF IDE1140 FE





The readout of 5 ADCs, with half IDE1140 glued and bonded as shown in figure

FIRST DATA ACQUISITION

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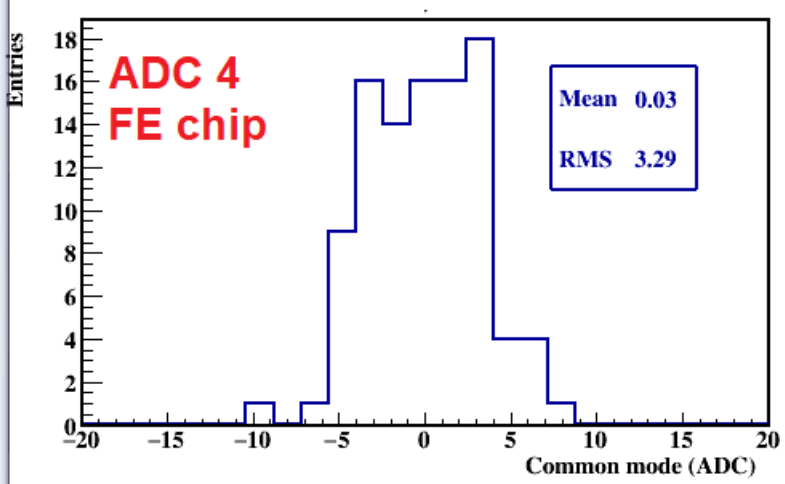
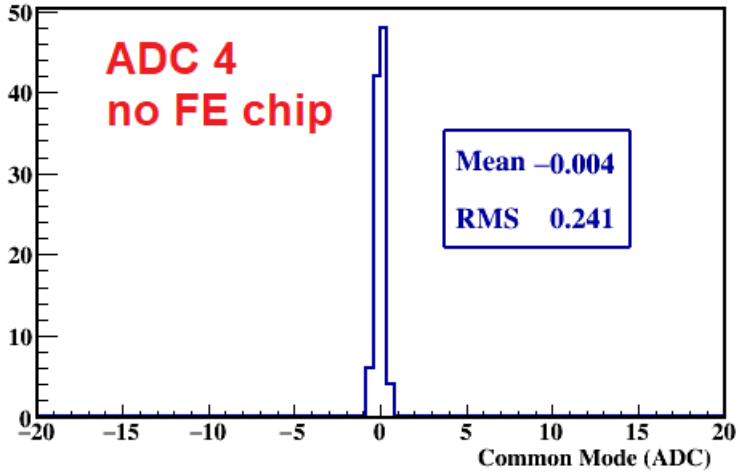
5 ADC OUT WITH HALF IDE1140 FE





Distribution of common mode noise of chip # 7 with FE acquired by ADC 4

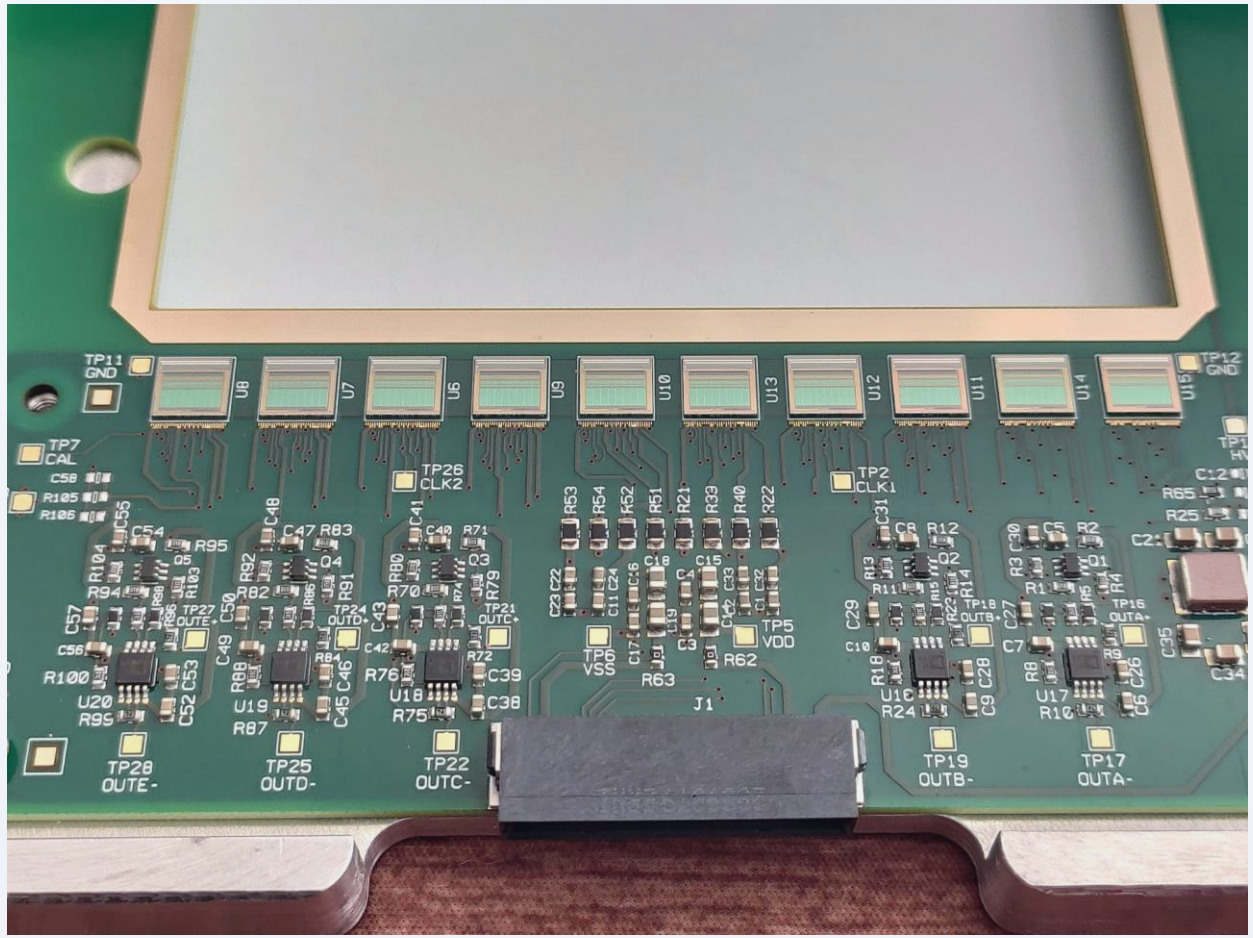
Fluctuations of 3.3 ADC

Distribution of common mode noise of chip # 8 without FE acquired by ADC 4

Fluctuations of 0.2 ADC

FIRST DATA ACQUISITION

WORK IN PROGRESS



- 10 IDE1140 already bonded on the hybrid board
- Tests with DAQ ongoing

TRIGGER BOARD

BLOCK DIAGRAM

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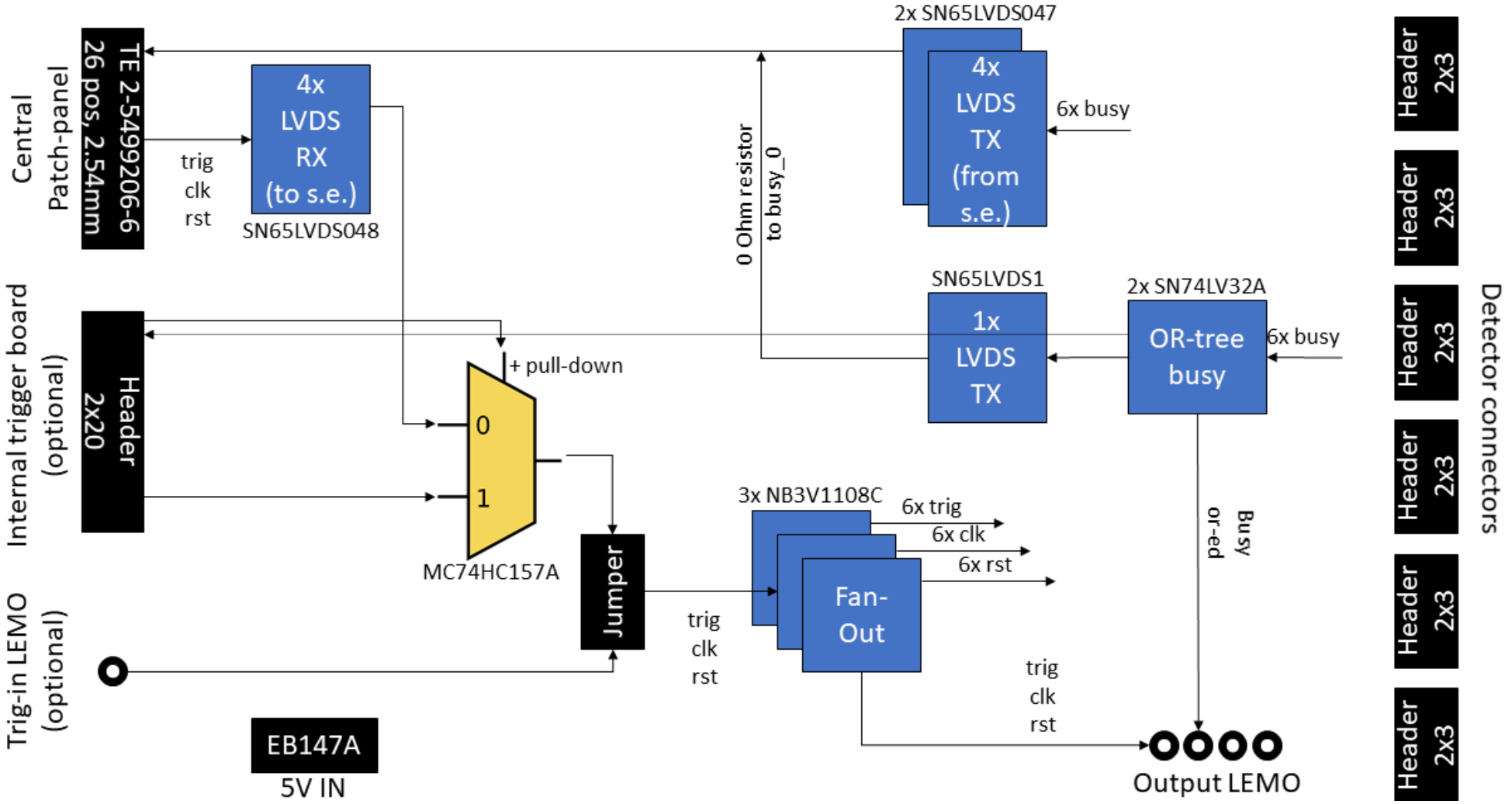

Trigger distribution board:

The design is under finalization.

CONCLUSIONS

RESULTS

MSD HARDWARE

- Several mechanical and assembly steps performed - close to assembling the complete single MSD module
  - Hybrid boards completed with front end chips
- Data acquisition hardware chain completed
  - HYBRIDs, ADCs, DE10-NANO boards
- Trigger distribution board design under finalization

MSD DAQ FIRMWARE

- Firmware development for MICROSTRIP detectors interface and ADC control
- Successfully interfacing the MSD module with the Bologna central DAQ firmware

- First acquisitions with the complete DAQ performed successfully

WHAT'S NEXT

TO DO LIST

MSD HARDWARE

- The first complete "final" module; start of first tests with ionizing radiation sources
- construction of another complete module to carry out the configuration strips facing each other for the x-y plane
- Working to have a one-piece MSD system (1 ethernet cable, 1 flat cable (digital LVDS), 1 power cable)
  - By the end of March development of mechanical support for all the MSD system and interface with general experiment frame

MSD DAQ FIRMWARE

- Optimize the developed firmware
- Develop the zero-suppression algorithm
- Adapt the firmware for the 3-plane x-y MSD data acquisition

- Tests for the reading of two DE10-nano at the same time.
- if possible, by the end of April test beam in Trento or CNAO for sensor characterization with single hadrons


Thank you