Budget

ITEM	WP	Richieste			Assegnati		
		Year 1			Year 1		
		PD	PV	PI	PD	PV	PI
Travels		**2**	**2**	**2**	**1**	**1**	**1**
Irradiation and testing	5	0	0	0	0	0	0
Work between designers	6	1	1	1	1	1	1
General meetings / confere	6	1	1	1	0	0	0
Consumables		**5**	**32**	**89**	**3**	**26**	**74**
EIC submission	3	0	17	34	0	17	34
PIC submission	2	0	0	25	0	0	25
Test boards EIC	3	0	5	10	0	5	5
Test boards PIC	2	0	0	0	0	0	5
X-ray tubes	5	0	0	0	0	0	0
Others (cables, fibers, glues, fluids, powder, renting equipment)	1,2,3,4,5	5	10	20	3	4	5
Access to external irradiati	5	0	0	0	0	0	0
External services		**0**	**0**	**10**	**0**	**0**	**10**
Demonstrator design and a	4	0	0	10	0	0	10
Licenses		**0**	**0**	**8**	**0**	**0**	**8**
PIC design	2	0	0	8	0	0	8
Equipment		**0**	**20**	**35**	**0**	**5**	**18**
FPGA	3	0	5	10	0	5	8
Power supply	3	0	5	0	0	0	0
Laser Source (DFB) x2	2	0	0	10	0	0	10
Workstations / HD / Screer	2	0	0	5	0	0	0
Workstations / HD / Screer	3	0	10	10	0	0	0
TOTAL w/o AdR		**7**	**54**	**144**	**7**	**54**	**111**
Assegni di Ricerca (AdR)		**0**	**60**	**85**			24

Sez. & Suf.	MISS				CON				ALTRICONS				TRA				SEM				PUB				MAN				INV				LIC-SW				APP				SPSERVIZI				TOTALE			
		Sj	Dot.	Ant.		Sj	Dot.	Ant.		Sj	Dot.	Ant.	Sj	Dot.	Ant.		Sj	Dot.	Ant.		Sj	Dot.	Ant.		Sj	Dot.	Ant.		Sj	Dot.	Ant.		Sj	Dot.	Ant.		Sj	Dot.	Ant.		Sj	Dot.	Ant.		Sj	Dot.	Ant.
PD	2.0				5.0																																						7			
	1.0				3.0																																						4.0			0
PI	2.0				79.0				10.0																				35.0				8.0								95.0				229			
	1.0				74.0				0.0	10.0																			8.0	10.0			0.0	8.0							24.0	10.0			107.0	38.0		0
PV	2.0				32.0																								20.0												60.0				114			
	1.0				26.0																								5.0												0.0				32.0			0
TOTALE	6				116				10																				55				8								155				350			
	6				116				10				0				0				0				0				55				8				0				155				350			
	3		0	0	103		0	0	0	10	0	0																	13	10	0	0	0	8	0	0					24	10	0	0	143	38.0	0.0	0.0
	3.0				103.0				10.0				0.0				0.0				0.0				0.0				23.0				8.0				0.0				34.0				181.0			

Assegni

AdR #	Type	Unit	Months	Research Topic	Bandito/ Partenza	Vincitore
1	**J**	**PI**	**30**	**PIC design and test. PIC-EIC integration and test**	**2021**	
2	**S**	**PI**	**24**	**Driver design. PIC-EIC integration and test**	**2020/2021**	**G. Ciarpi**
3	J	PI	12	PLL/CDR design and test	2022	
4	**J**	**PV**	**30**	**DAC design and test**	**2020/2021**	
5	S	PV	12	FE design, test and integration in the demonstrator	2022	
6	J	PD	12	Irradiation tests and analysis	2022	

Gantt chart

Month		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
		Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
WP1 (System Design)	specibenchiver																																				
	Demonstrators																																				
WP2 (PIC)	PIC mini-block																																				
	PIC full-block																																				
WP3 (EIC)	IP and FE 1st																																				
	IP and FE 2nd																																				
	Final EIC																																				
WP4 (EIC-PIC Integration)	1st demo																																				
	final demo																																				
WP5 (Irradiation)																																					
WP6 (Project management & dissemination)																																					

MILESTONES	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
Deliverables	D1.1	D2.1	D3.1/5	D3.1b D5.1	D1.2 D2.2	D4.1	D5.1 D3.6	D5.1 D2.3	D4.1	D4.2 D6.2

Legenda

- Specifications/benchmark/verification
- PIC design & layout
- PIC fabrication
- EIC design & layout
- EIC fabrication
- Integration test
- Integration design
- EIC-PIC Integration
- EIC test
- PIC test
- Irradiation

Milestones

M1 (Definitions of the specs and KPI) (T0+2)
M2 (Silicon Photonics PIC design for the submission of the mini-block chip fabrication) (T0+6)
M3 (1st submission of the High Speed rad-hard block design) (T0+10)
M4 (2nd submission of the High Speed rad-hard block design) (T0+16)
M5 (Final Silicon Photonics PIC design for the submission of the full block chip fabrication) (T0+18)
M6 (First integration EIC+PIC) (T0+21)
M7 (Final, large area EIC submission) (T0+25)
M8 (Qualification of rad-hardness of PIC and EIC) (T0+29)
M9 (Final demonstrator integration) (T0+32)
M10 (Final demonstrator qualification) (T0+36)

Work package details - I

- WP1 (System Design) defines the system specifications and key performance indicators (KPI) as inputs to WP 2 to 5 to outperform state of the art and benchmarking. Designs the final demonstrator together with WP4.
  - D1.1 System specifications and KPI (INFN PV, UNIMI) (T0+2)
  - D1.2 Demonstrator design (INFN PV) (T0+18)

- WP2 (Silicon Photonics) It will develop the SiPh building blocks.including RM, MZM,bus waveguides, optical couplers and splitter, integrated thermal heaters. It will submit the MPW of a mini-block chip (2.5x~5 mm^2). The fabricated mini-block will be characterised, providing information for the design and fabrication of the second full block chip (5x~5 mm^2) that will be tested allowing the final integration with EIC.
  - D2.1 SiPh submissions for the MPW run of the first miniblock including the building blocks (SSSA, INFN PI, UNIPI, UNIMI) (T0+7)
  - D2.2 SiPh submission for the MPW run full final block (SSSA, INFN PI, UNIPI, UNIMI) (T0+19)
  - D2.3 SiPh final PIC characterization (SSSA) (T0+31)

Work package details - II

- WP3 (Electronics) design of the fundamental rad-hard and high-speed electronics and test boards
  - D3.1/3.1b Serdes (INFN PI, UNIPI, UNIMI): 1st/2nd submissions (T0+10, T0+16)
  - D3.2/3.2b Drivers and Tune circuit (INFN PI and PV, UNIPI): 1st and 2nd submissions (T0+10, T0+16)
  - D3.3/3.3b PLL/CDR (UNIPI, INFN PD and PI): 1st/2nd submission (T0+10, T0+16)
  - D3.4/3.4b Front-End circuits (INFN PV): 1st/2nd submissions (T0+10, T0+16)
  - D3.5/3.5b DAC/Bandgap (INFN PV, UNIMI): 1st/2nd submissions (T0+10,T0+16)
  - D3.6 Final large area EIC submission (INFN PV) (T0+25)

- WP4 (EIC-PIC Integration) will develop the integration of the PIC and EIC (akaDemonstrator), together with an external company.
  - D4.1/4.1b Prototypes and final demonstrator system (All) (T0+22, T0+32)
  - D4.2 Demonstrator tests (All) (T0+36)