MAPS (Monolithic Active Pixel Sensor) design: experience at INFN-LNF

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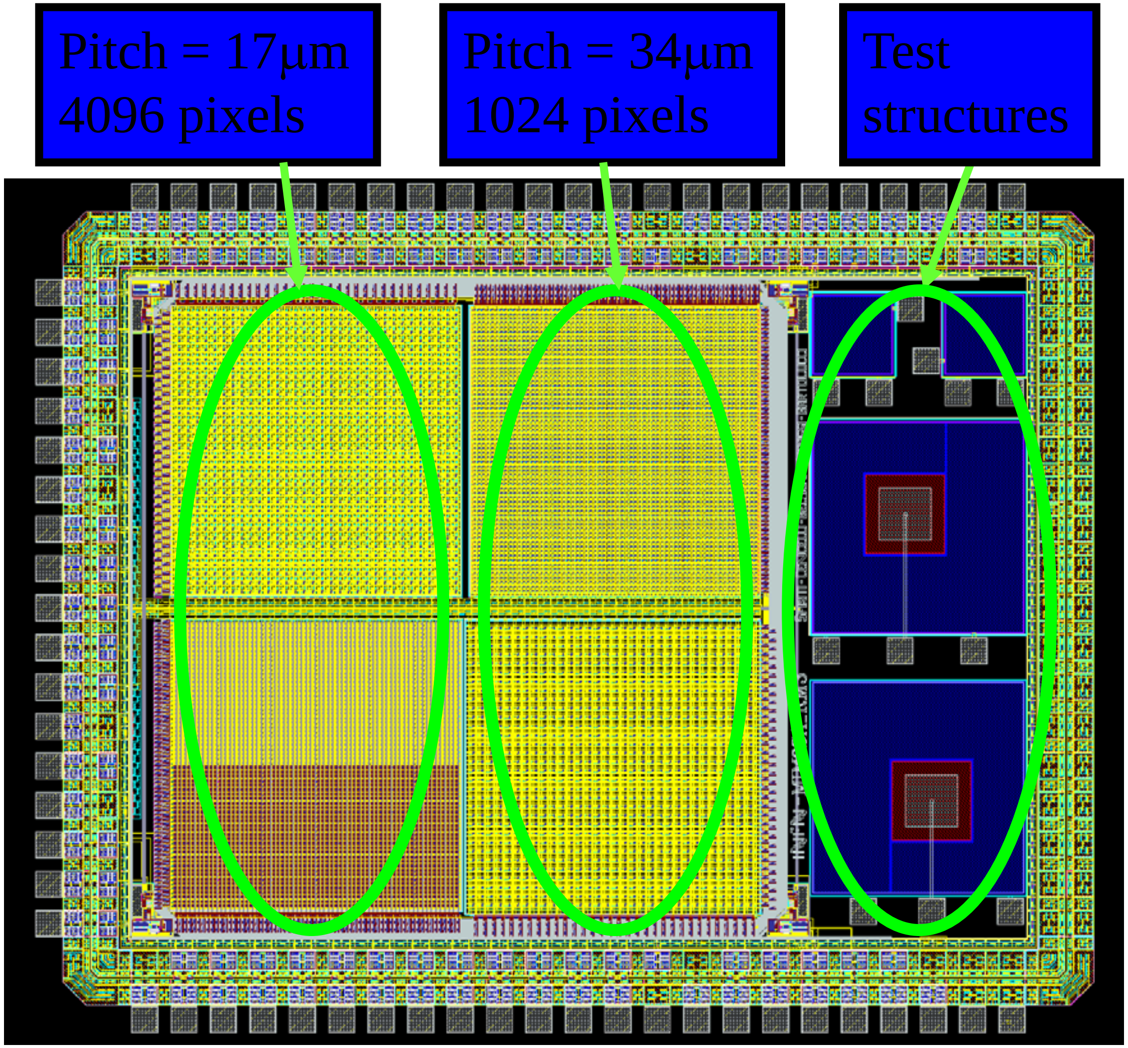
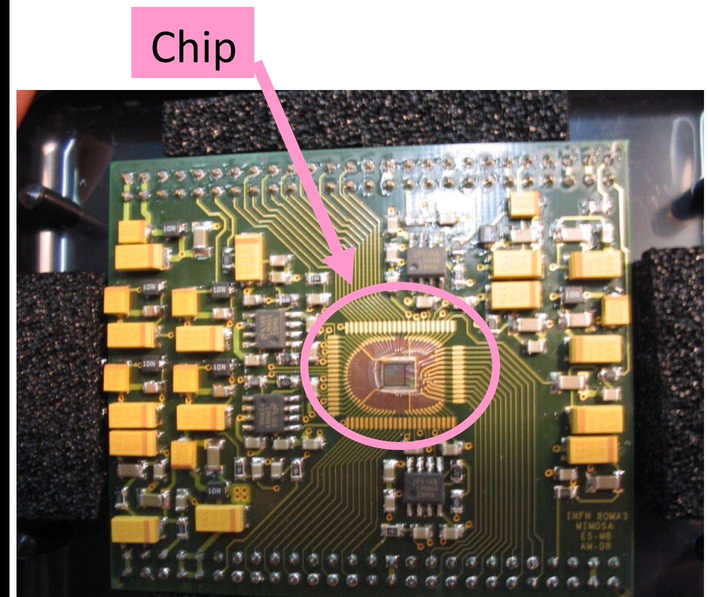
1. A brief history:
   - Mimoroma1
   - Mimoroma2
   - Mimoroma3
2. Further studies for ”Mimoroma4” (not built)
3. Solutions proposed
3. Simulation results: **mismatch, noise, S/N, power, area**.
4. Conclusions

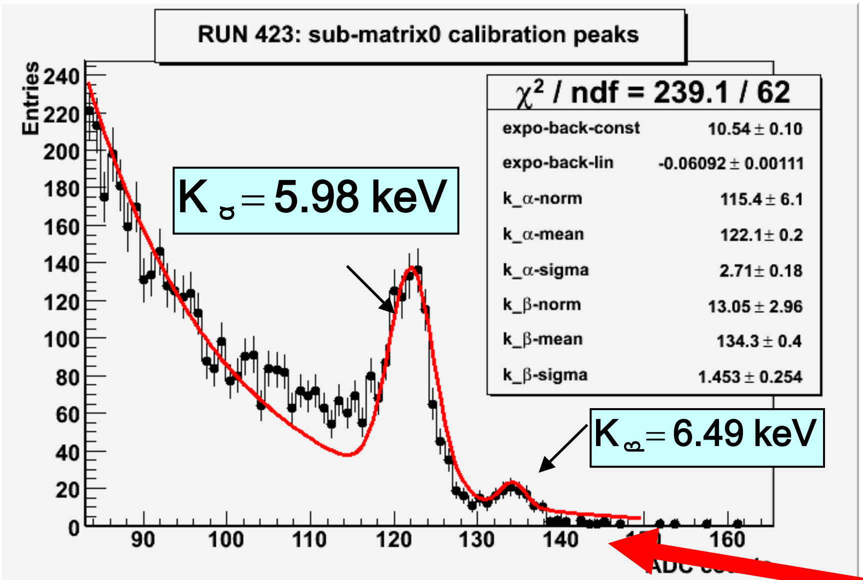
Mimoroma1: the first trial!



- TSMC 0.25 µm
- 8 µm epi thickness
- gate all around design for radiation hardness
- different pixels architecture (different collecting diode number and dimensions)

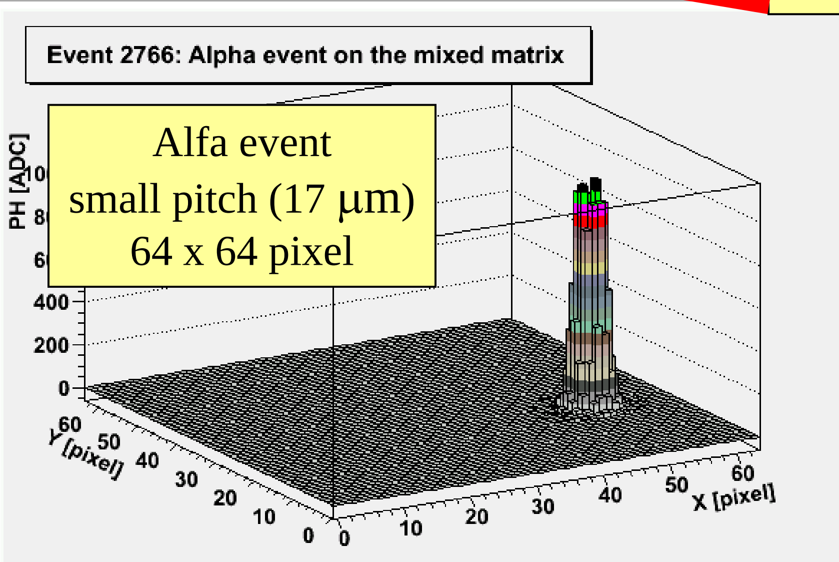


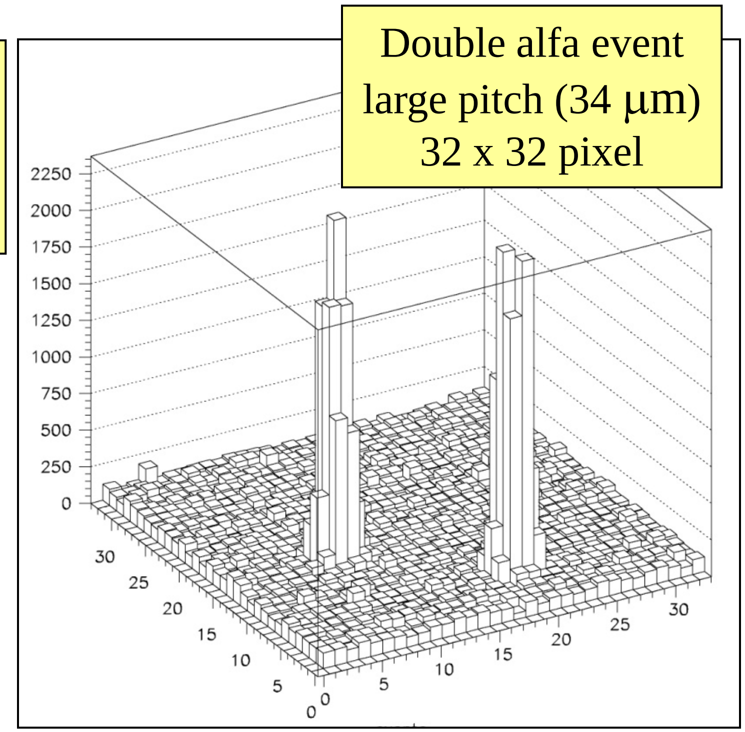
Mimoroma1: the first trial!



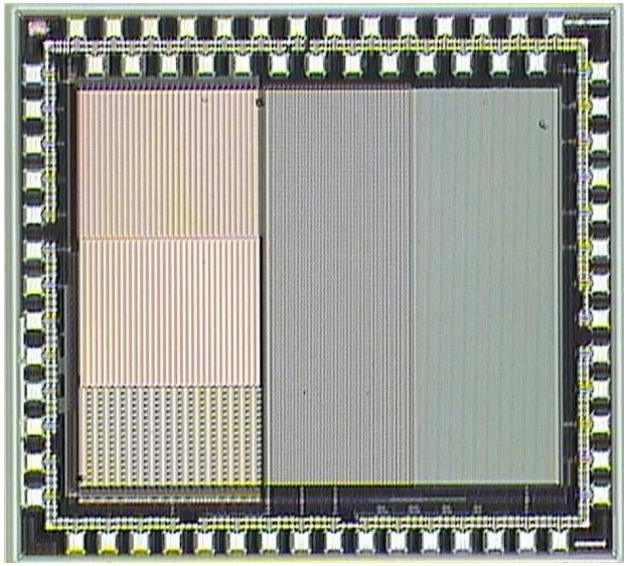
mimoroma1 chip
(first? MAPS designed at INFN)

Fe55 X
X ray
source

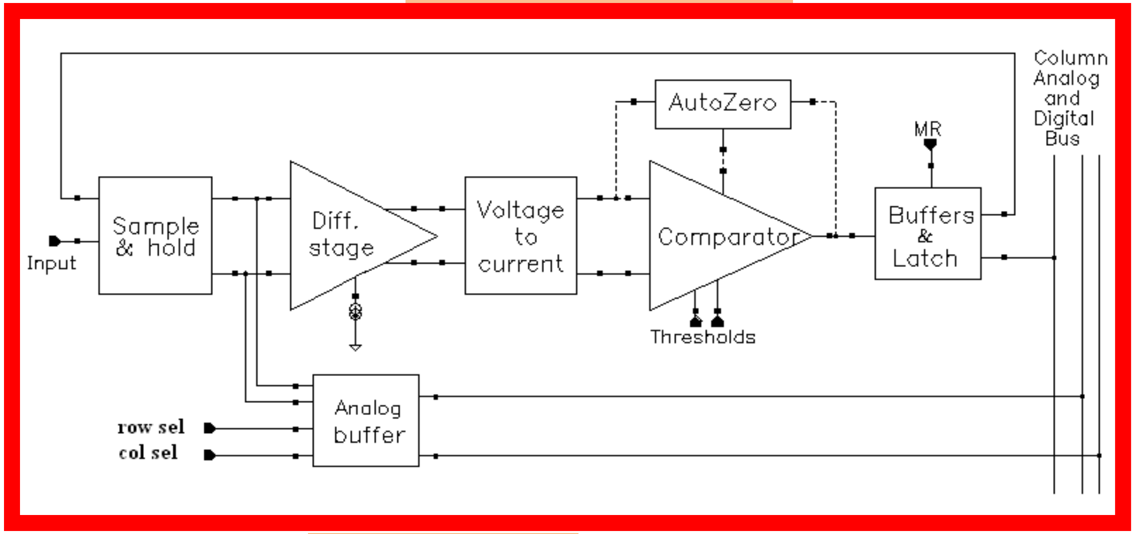




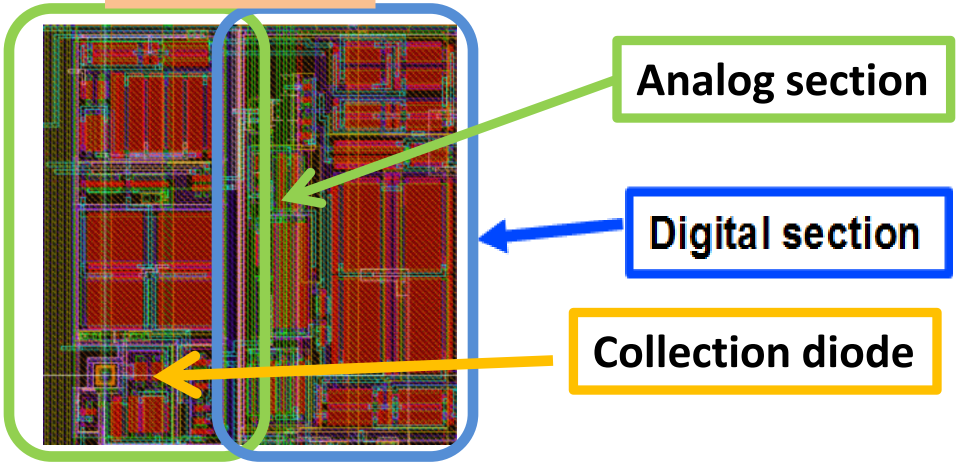
The Mimoroma2 example (only NMOS architecture)



Pixel architecture

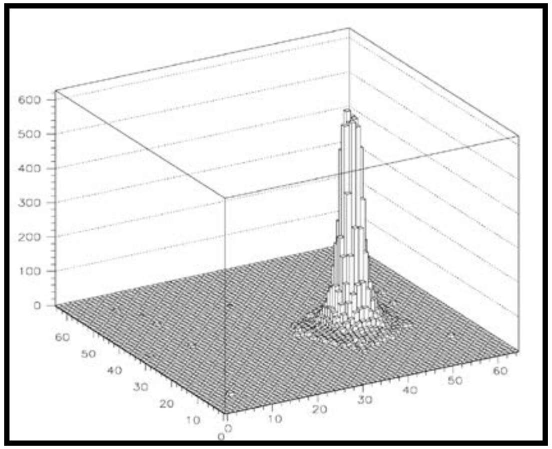


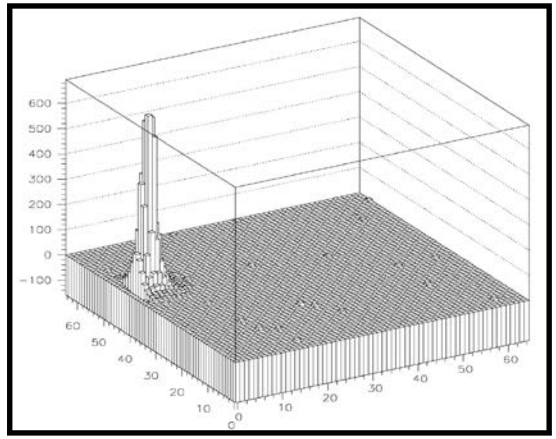
Pixel layout



- STMicroelectronics CMOS 130nm
- Chip size: 2mm x 3mm
- 18 different arrays
- sparsified pixel size: 25µm x 25µm

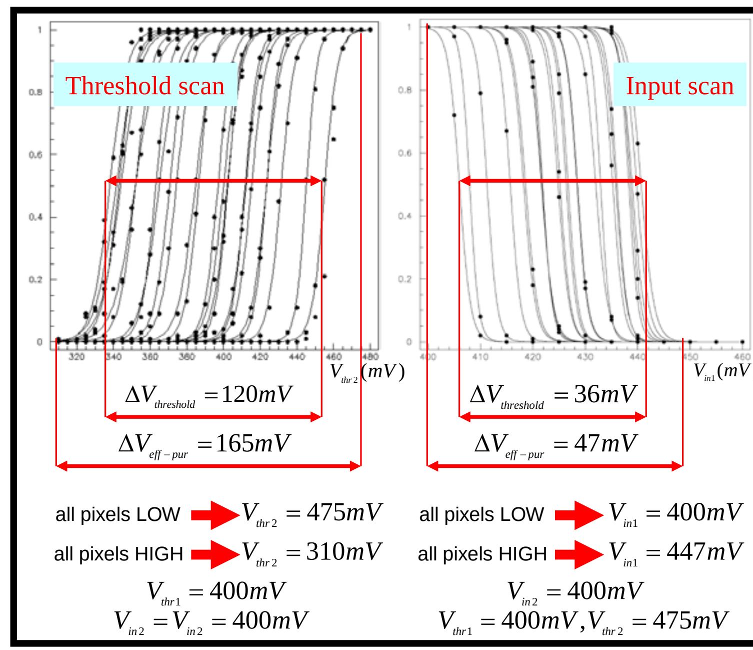
The Mimoroma2 example (only NMOS architecture)





Discriminator threshold dispersion: only NMOS transistor used in the design.

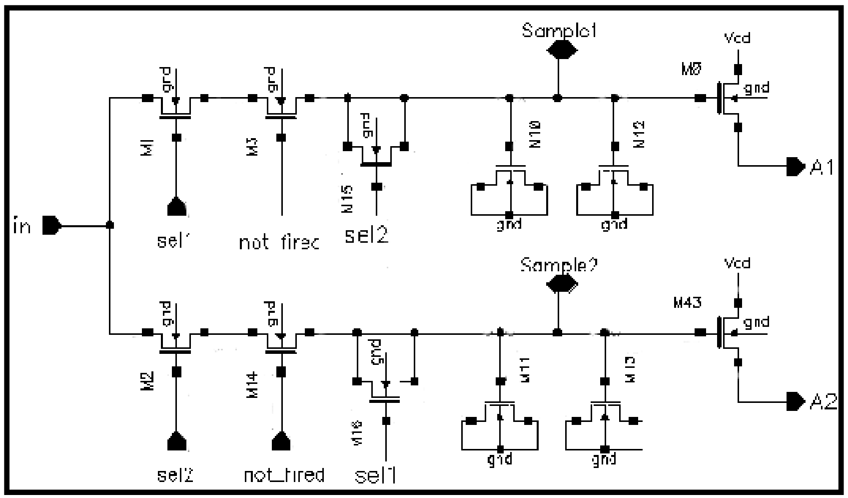
Alpha particles detection: Cluster reconstruction of two events produced by an alpha particle hit on the two 32x64 non-sparsified pixel matrices (HG and LG) by Americium 241 radioactive source.



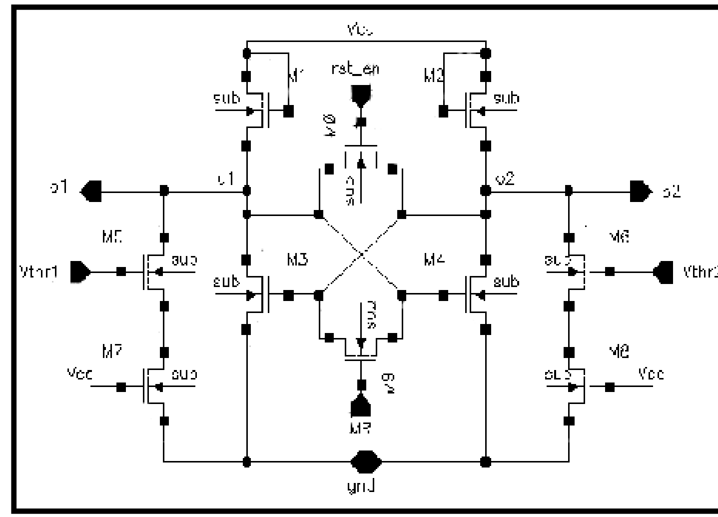
Mimoroma3: a jump into 3D technology (130nm Chartered, GlobalFoundries, Tezzaron)

Input stage 3T configuration

S&H stage configuration



Discriminator stage configuration
Only NMOS configuration in mimoroma2
NMOS/PMOS used in mimoroma3

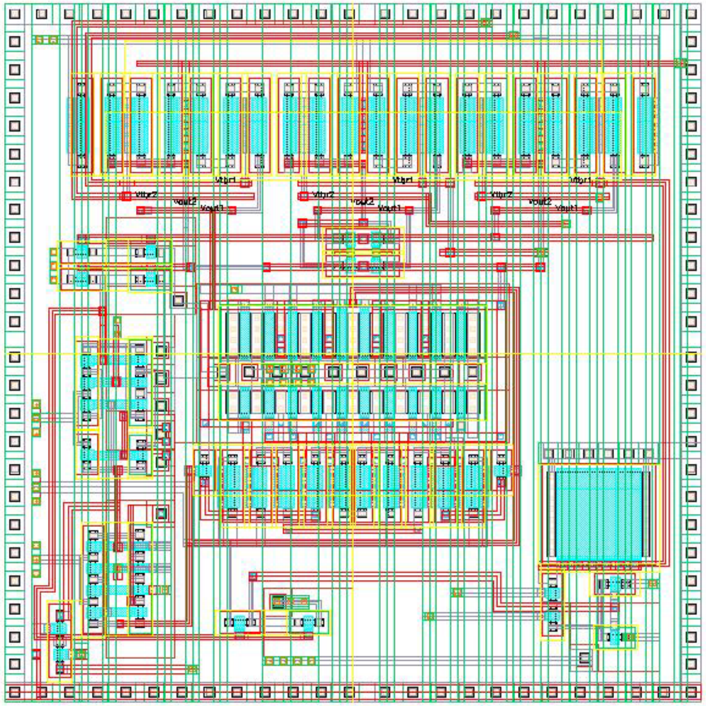


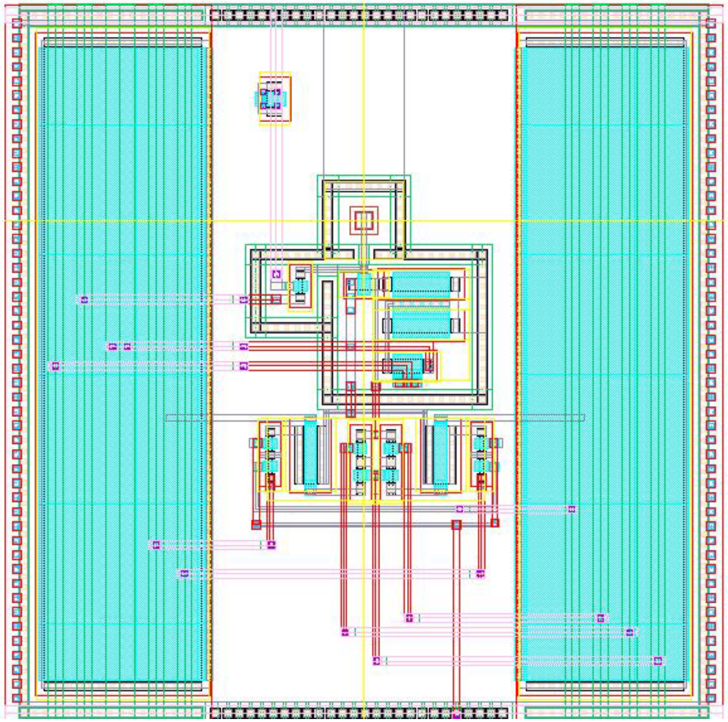
- A. Bulgheroni, E. Spiriti, J. Mlynarczyk, “Design and characterization of a Monolithic Active Pixel Sensor in 0.25µm Technology” Proceedings of the 10th ICATPP Conference. Held 8-12 October 2007, DOI: 10.1142/9789812819093_0156
- J. Mlynarczyk, E. Spiriti, A. Bulgheroni, “Design of a monolithic active pixel sensor in ST 0.13um technology,” Proceedings of the 10th ICATPP Conference, Oct. 2007, pp. 999-1003.
- Mlynarczyk, J., Spiriti, E.; "On pixel xignal processing for MAPS sparsified readout implemented in CMOS VLSI technology"; Signals and Electronic Systems, 2008. ICSES '08. International Conference on; DOI: 10.1109/ICSES.2008.4673359
- Spiriti, E., Mlynarczyk, J.;"Results of an on pixel sparsification architecture in a MAPS test chip in STM 130nm technology"; Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE; DOI: 10.1109/NSSMIC.2008.4774596

Pixel layout area

Mimoroma3 (Chartered 0.13µm) 2*25µm*25µm=1250µm²

25µm x 25µm Digital Tier pixel **25µm x 25µm Analog Tier pixel**





Area estimation:

Mimoroma3 → ∑MOS(wxl)~270 µm² 90% S&H MOS capacitors

Mimoroma4 → ∑MOS(wxl)~135 µm² 85% S&H MOS capacitors

- 50 µm pitch should be NO PROBLEM with 0.13 µm and 0.18 µm technologies
- 25 µm pitch probably possible with 0.13 µm, difficult/impossible with 0.18 µm.

Further studies for "mimoroma4" → modified mimoroma2/3 architecture
only simulations shown from here on!

Constrains

- In single particle application (MIPs) main constrain → rate (100Mhits/s*cm^2)
- signal level → 500-1000 electrons
- if ADC how many bits, dynamic range?
- readout time?
- SDS **S**parse **D**ata **S**can?

Considerations/questions

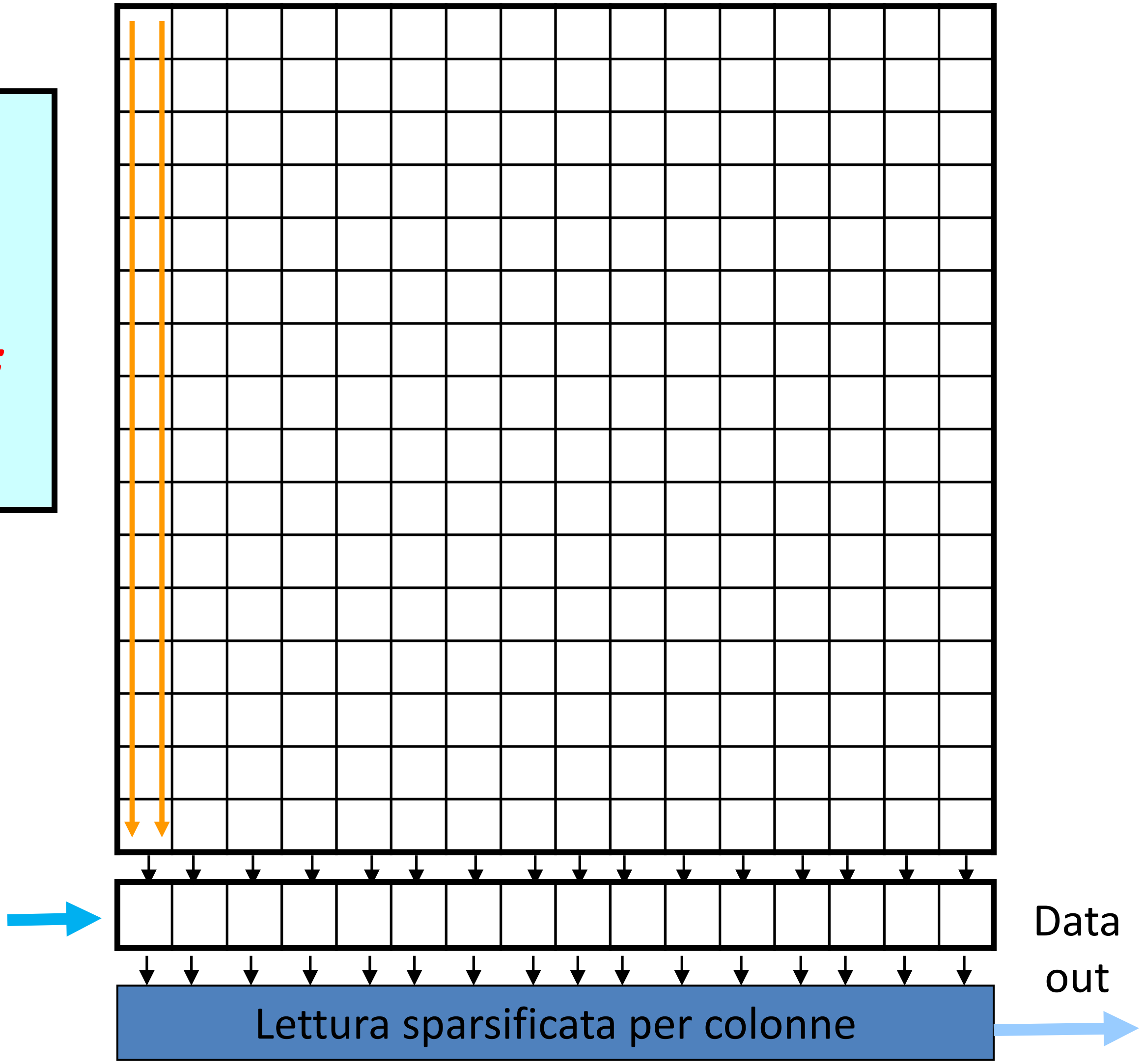
- Digital readout only? → in-pixel discriminator (noise, mismatch, power, area)
  fast column/matrix(?) digital readout?
  only digital logic @ End of Column
- Analog readout only? → discriminator and/or ADC @ End of Column
  "slow" column/matrix(?) analog readout
- Both? → Fast digital and Analog readout (speed factor 10-20)
  fast column/matrix readout
  fast column/matrix readout
- Discriminator → **level sensitive/latch type** (integration time)(?)
  mismatch correction?
- In pixel analog pipeline? → How many stages deep? (one minimum if Analog RO)
- End of Column readout

Matrix readout architecture

Solution based on:

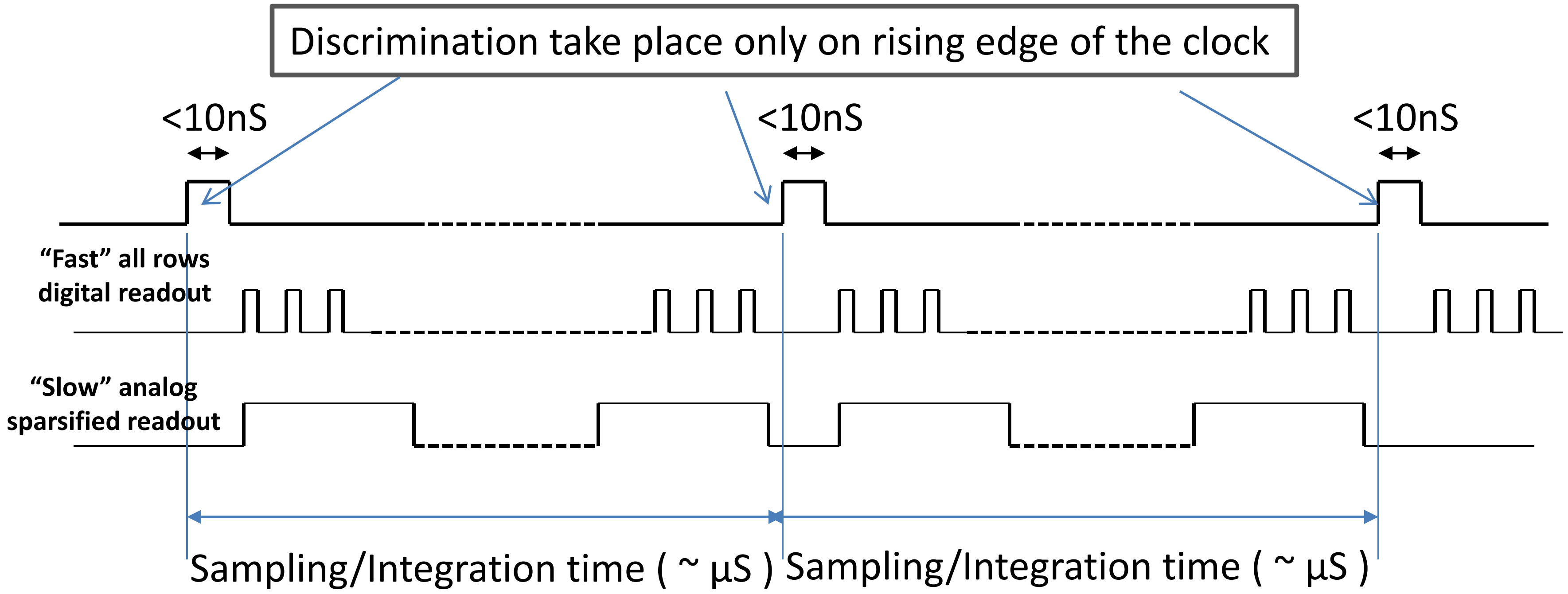
- *in pixel discrimination*
- *in pixel analog memory*
- *column readout*
- *two column readout busses:*
  - *digital on/off (fast)*
  - *analog (slow) sparsified*

End of column digital
(fast synchronous readout)
+
Sparsified (slow) analog/
ADC readout

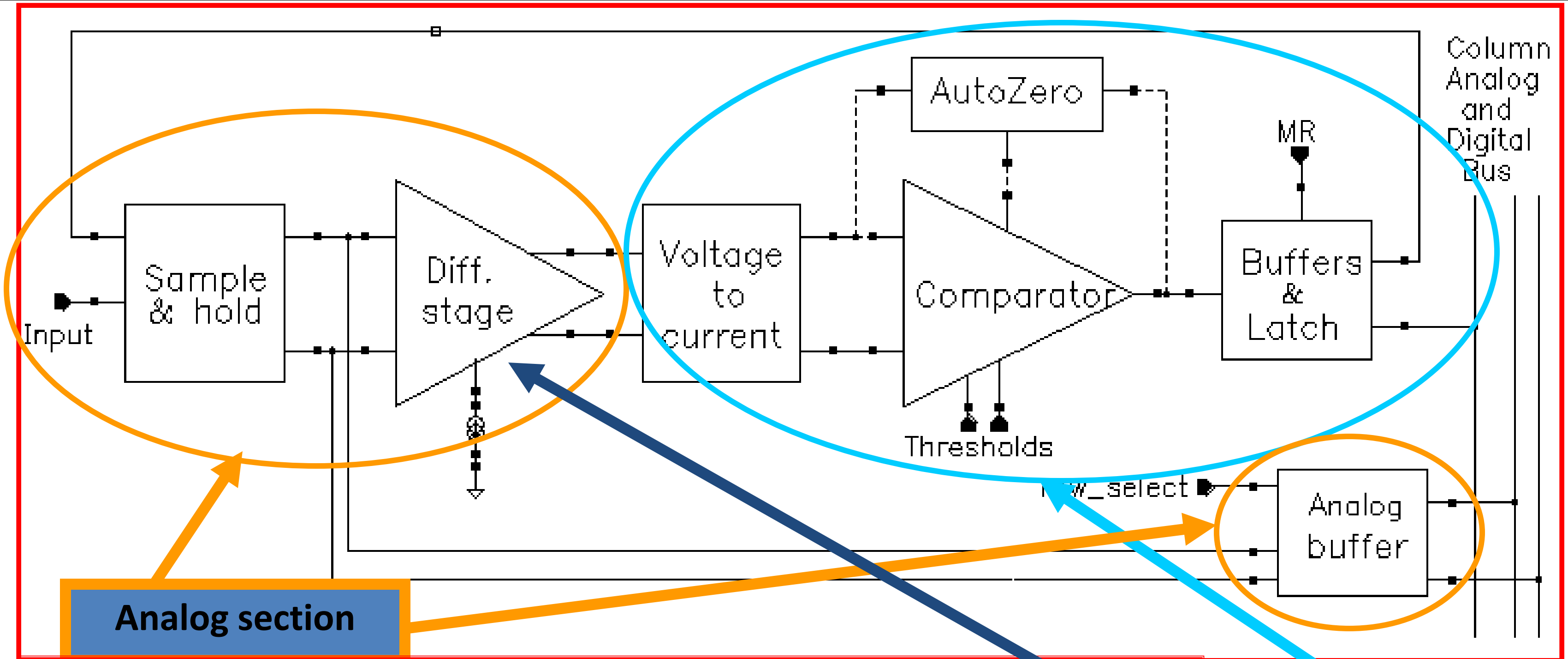


Achitecture: timing!

- Sample & Hold and discriminator sampling @ Integration Time period
- All digital outputs of a column are readout in the integration time (rolling shutter)
- All analog output over threshold are readout in the integration time (token passing) with one level deep analog pipeline (data lost if “high” occupancy)
- Time resolution defined by Integration Time (time stamp resolution)



Pixel architecture



Digital section

- Fully differential (CDS comes naturally) configuration
- Switching technique (fast, small, low power)
- Autozero to compensate mismatch
- Analog signals available (dE/dx possible)
- Discriminator in pixel → sparse data scan
- Sample & hold/discriminator control in rolling shutter mode
- Input from 3T scheme or any integration front-end!!
- 3D coupling to "sensor" layer with or without FE possible

Simulation shows that further gain (differential stage) Is NOT needed!

Architecture manageable rates and readout times.

Rates for the 2 options: **25 µm or 50 µm pitch**:

A - 25 µm pitch

400x400 matrix - 10x10 mm^2 - 160000 pixel

100 Mhits/s*cm^2 - 1 Mhits/s*mm^2 - 625 hits/s*pixel

$\lambda = 250.0*10^3$ hits per second per column in average

T = Column scanning time = 9ns*400=3.6 µs

average number of hits to readout per column per scanning time = λ*T

λ*T = 250.0e3*3.e-6 = **0.9 hits/column*scanning time**

B - 50 µm pitch

200x200 matrix - 10x10 mm^2 - 40000 pixel

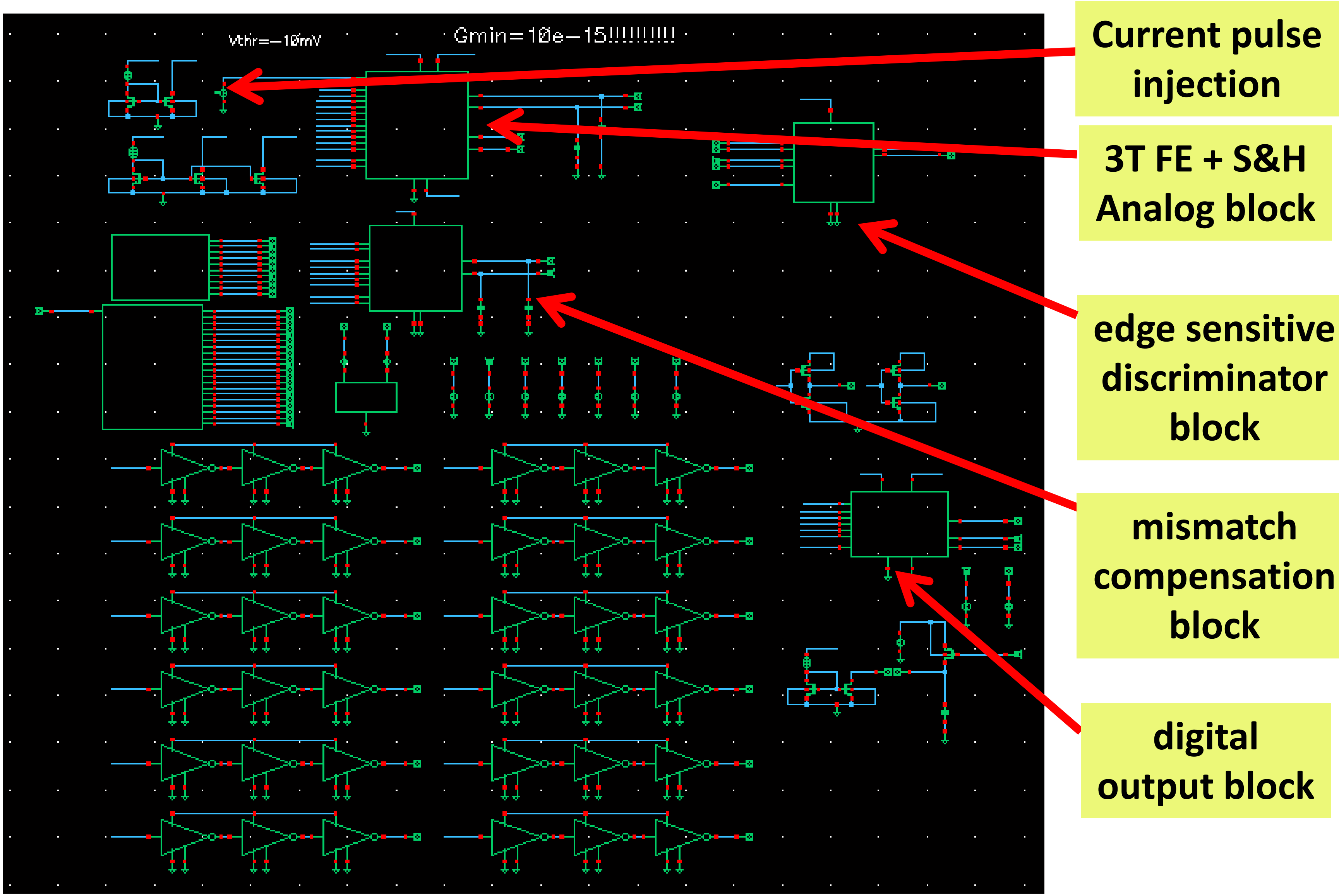
100 Mhits/s*cm^2 - 1 Mhits/s*mm^2 - 2500 hits/s*pixel

$\lambda = 500.0*10^3$ hit per second per column in average

T = Column scanning time = 9ns*200=1.8 µs

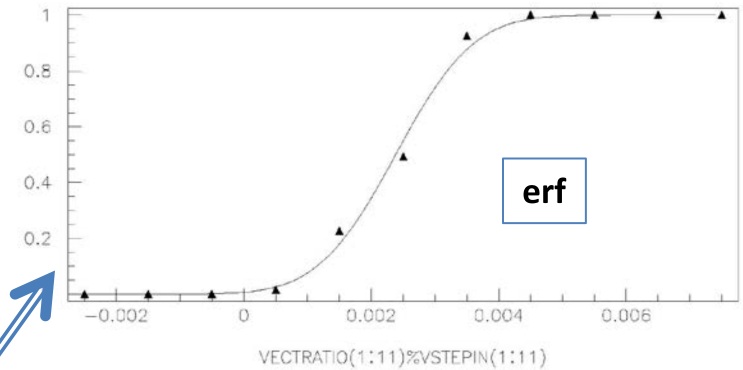
λ*T =500.0e3*1.8e-6 = **0.9 hits/column*scanning time**

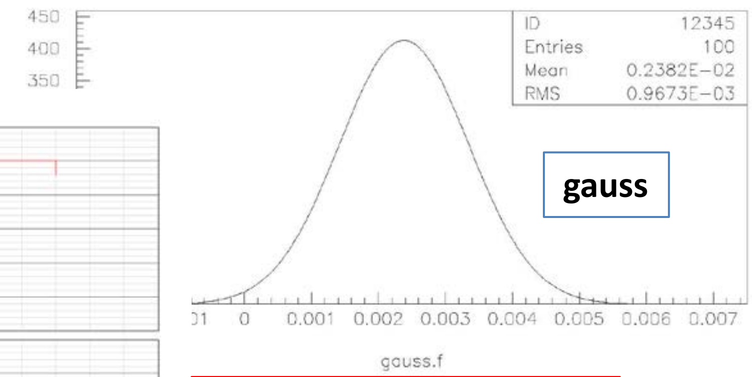
Block schematic of the pixel (GlobalFoundries 0.13 µm, q2v3)

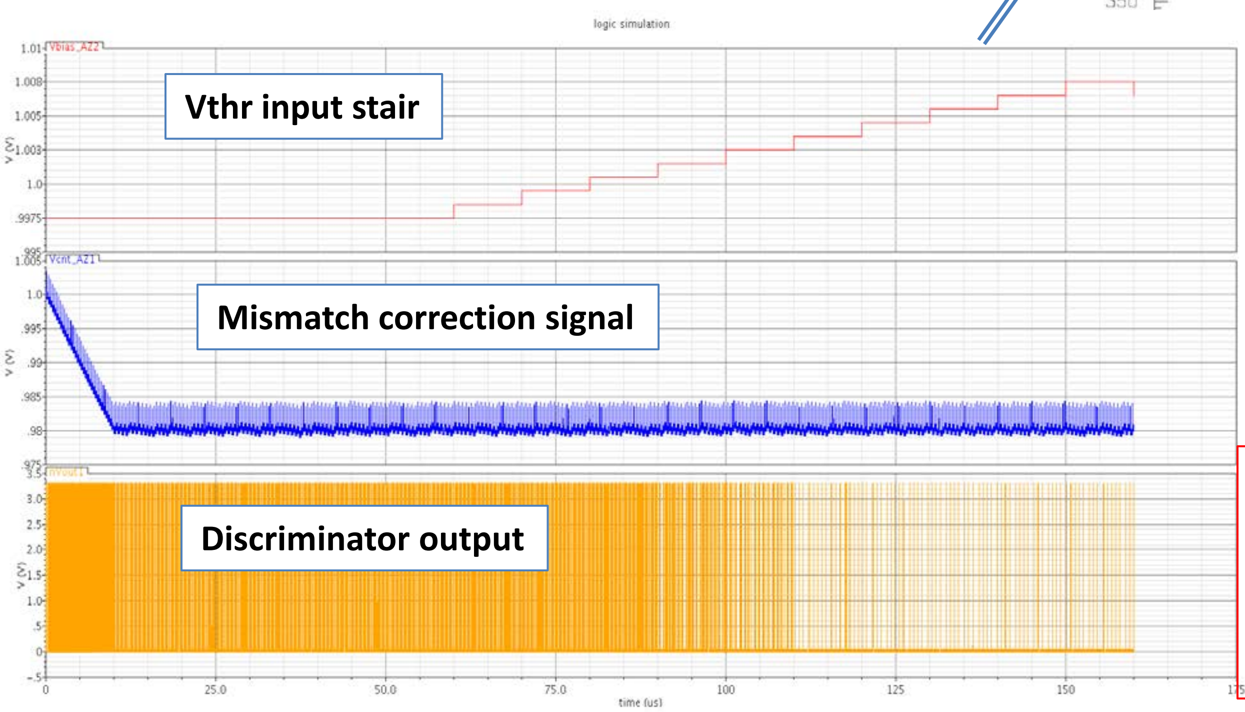


In pixel discriminator MonteCarlo transient noise simulation

Switched capacitor circuit simulation quite tricky:
- Transient noise Monte Carlo simulation needed
- Input threshold reference voltage stair applied after dispersion correction signal stabilization
- Discriminator output counted on each stair step for threshold scan evaluation







Simulation at 100ns Integration time.

Simulated 160 µs in **~80 min** simulation time on a core of a quad CPU/quad core Intel(R) Xeon(R) E5520 @ 2.27GHz

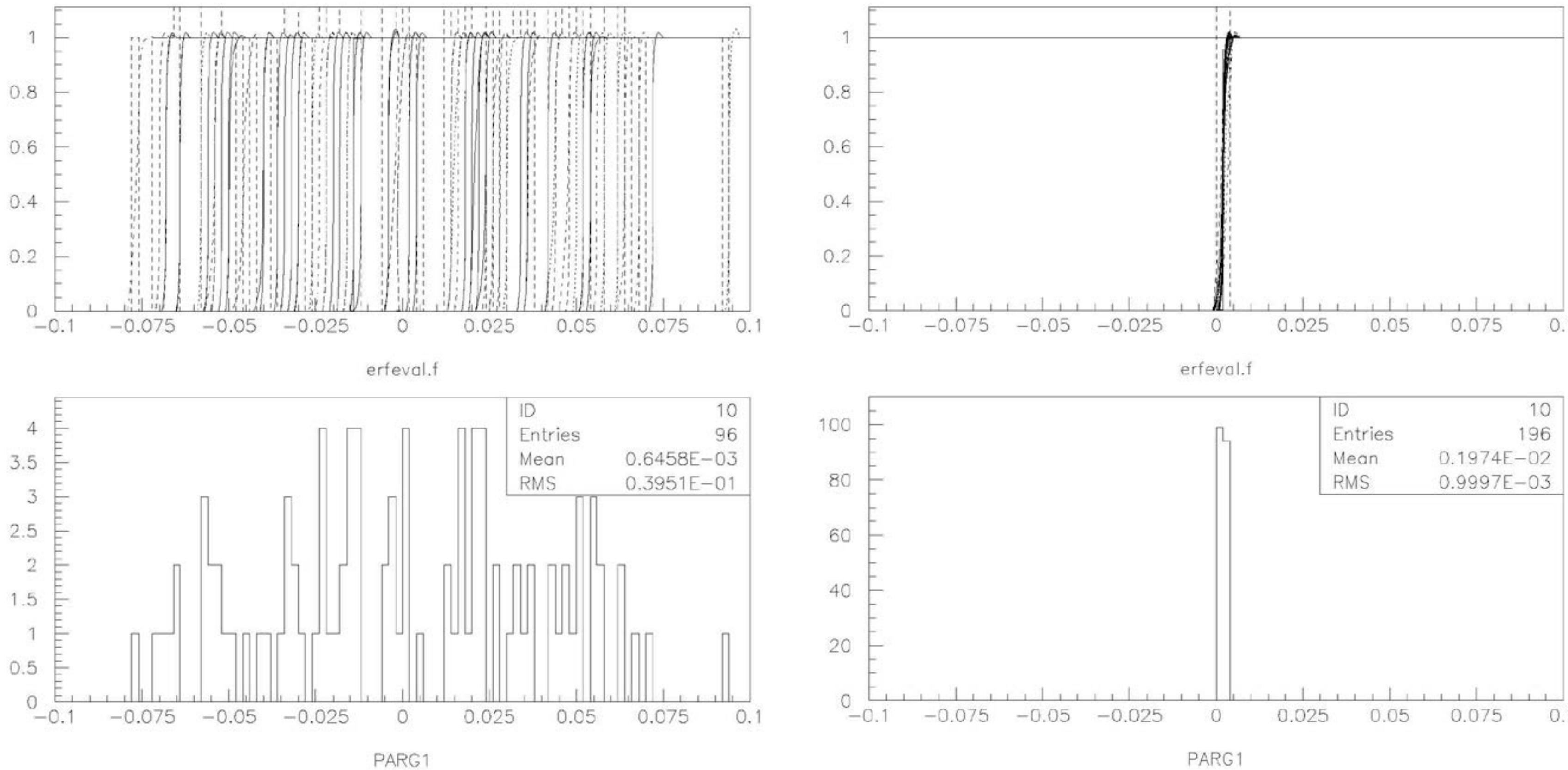
Discriminator threshold dispersion simulation with correction circuit switched off/on

Mismatch correction circuit **off**:

- x-scale ±100 mV
- offset RMS = 39 mV

Mismatch correction circuit **on**:

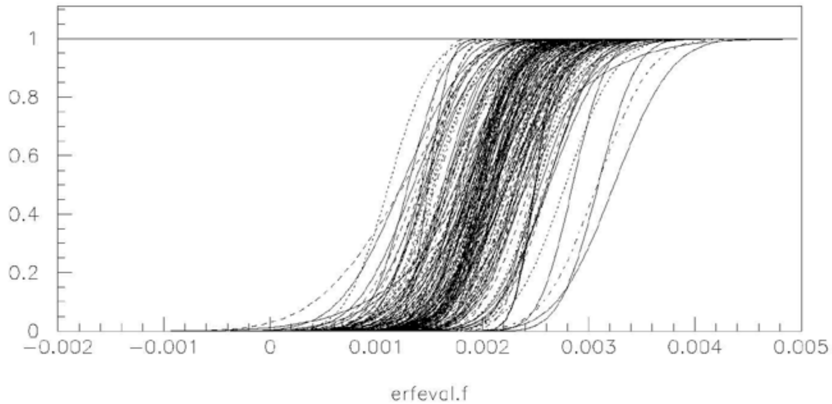
- x-scale ±100 mV
- **offset RMS reduced by 2 orders of magnitude**

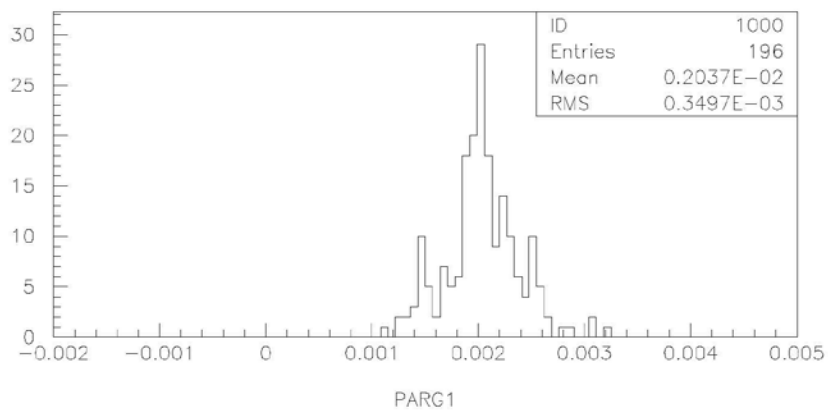


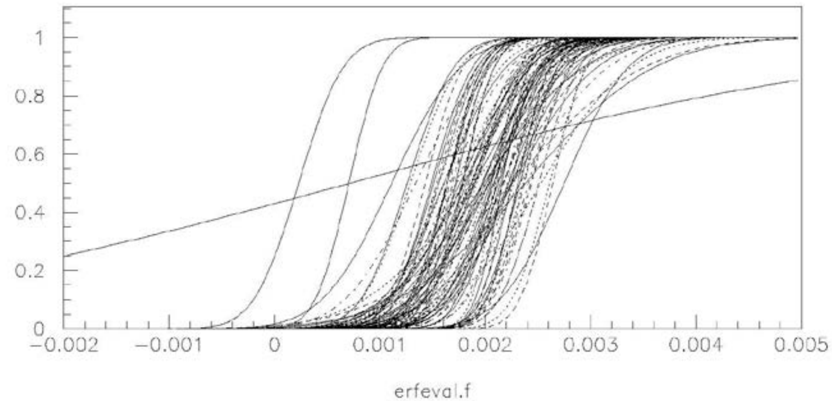
Discriminator/full pixel threshold dispersion with correction circuit on

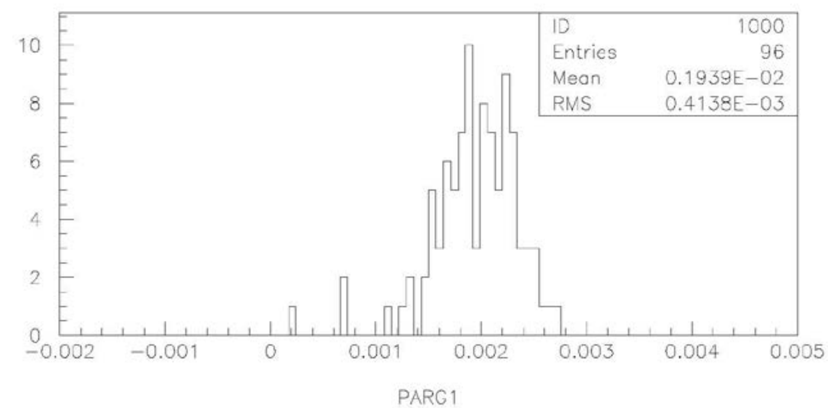
Mismatch correction circuit **on**, **discriminator circuit simulation**:
- x-scale (+5 mV, -2 mV)
- offset RMS = **0.35 mV**

Mismatch correction circuit **on**, **FULL PIXEL circuit simulation**:
- x-scale (+5 mV, -2 mV)
- offset RMS = **0.41 mV**



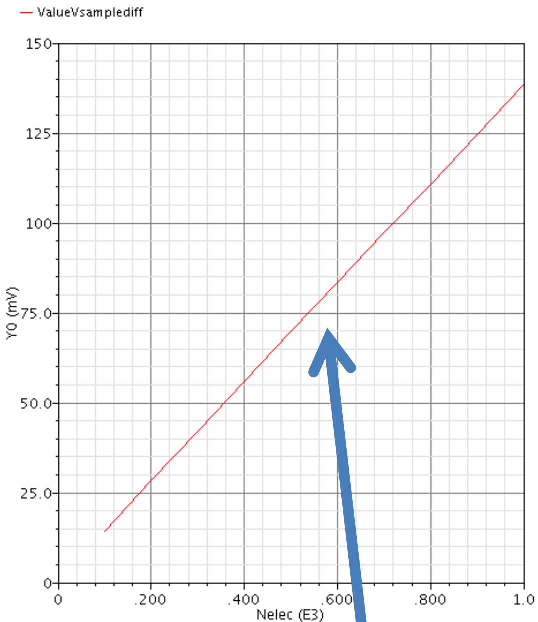


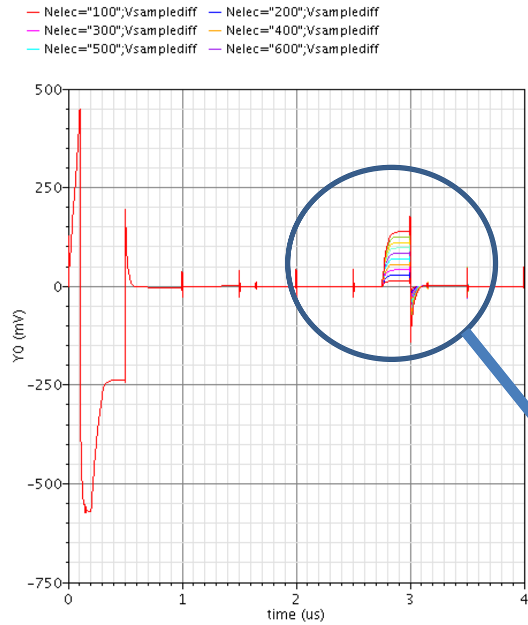




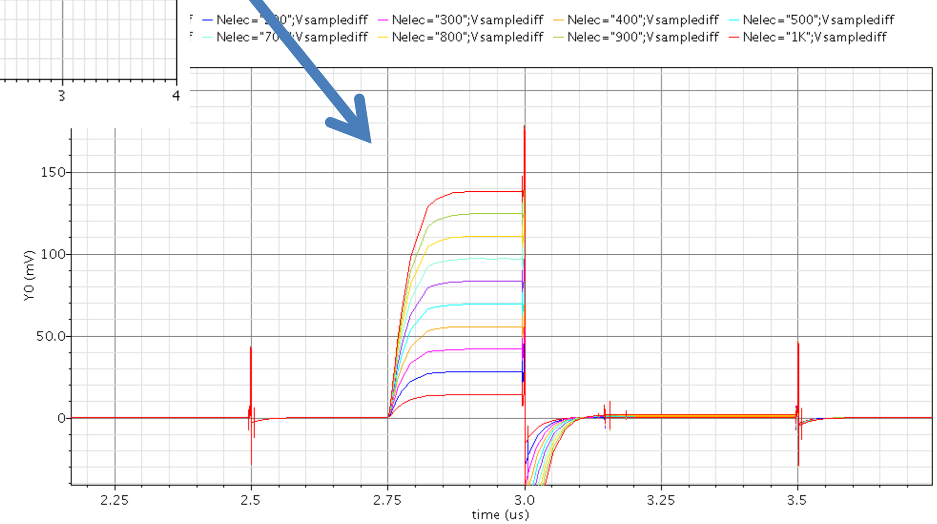
Pixel analog signal response/"calibration"

Parametric transient noise simulation (no MonteCarlo)





1 electron charge = 16pA for 10nS
Scan 100 e → 1000 e in 10 steps
Current pulse on a collecting diode of 3μm x 3μm area

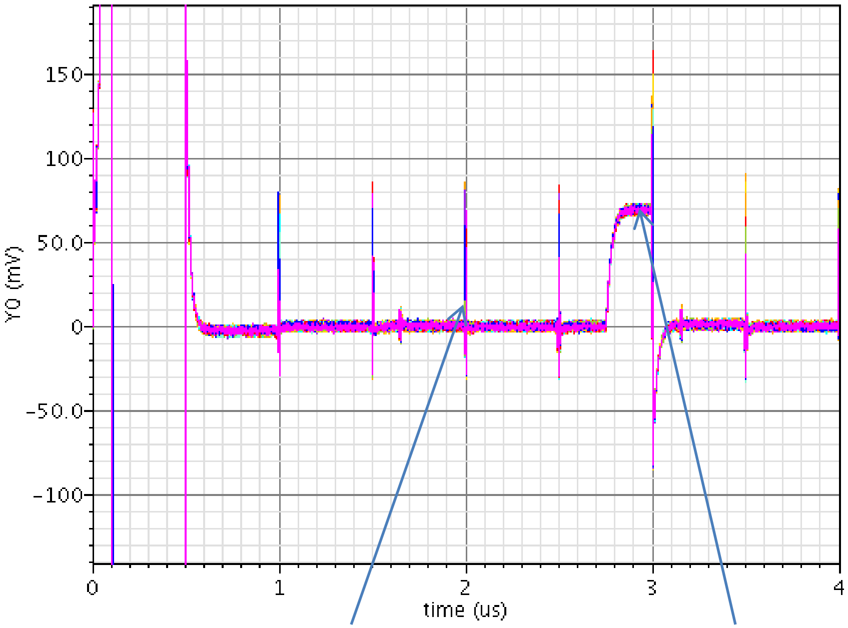


0.137mV/electron

Full pixel (3T configuration FE) signal to noise ratio

Differential input signal to discriminator

100 transient noise simulations



Sample of baseline

Sample of signal

Noise RMS=0.85 mV →

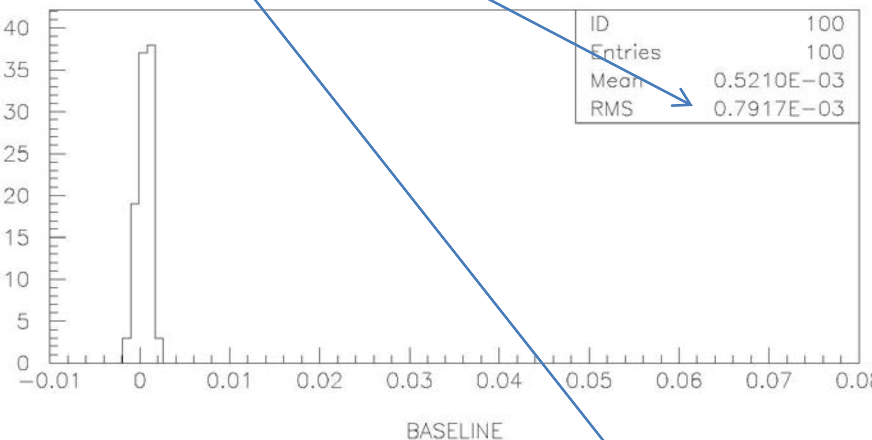
→0.85 mV/(0.137mV/electron)→

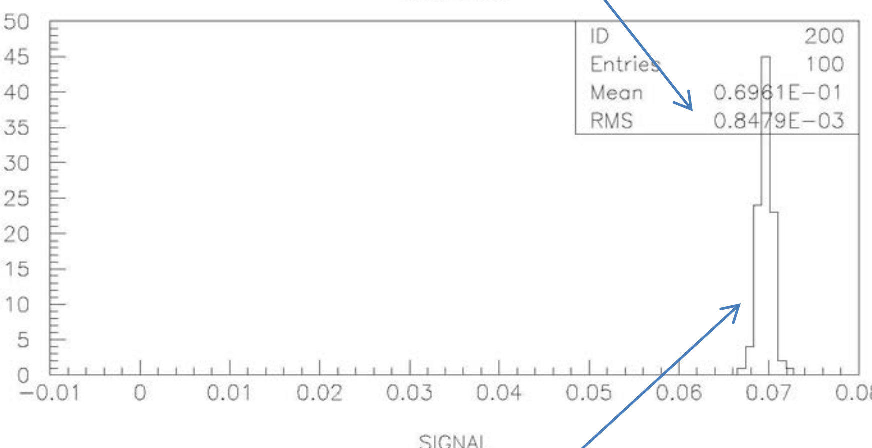
→ 6.2 e ????!!!!!

Residual mismatch noise to be added!

Sqrt(0.85^2+0.41^2)=0.94→ 6.9 e ????!!!!!

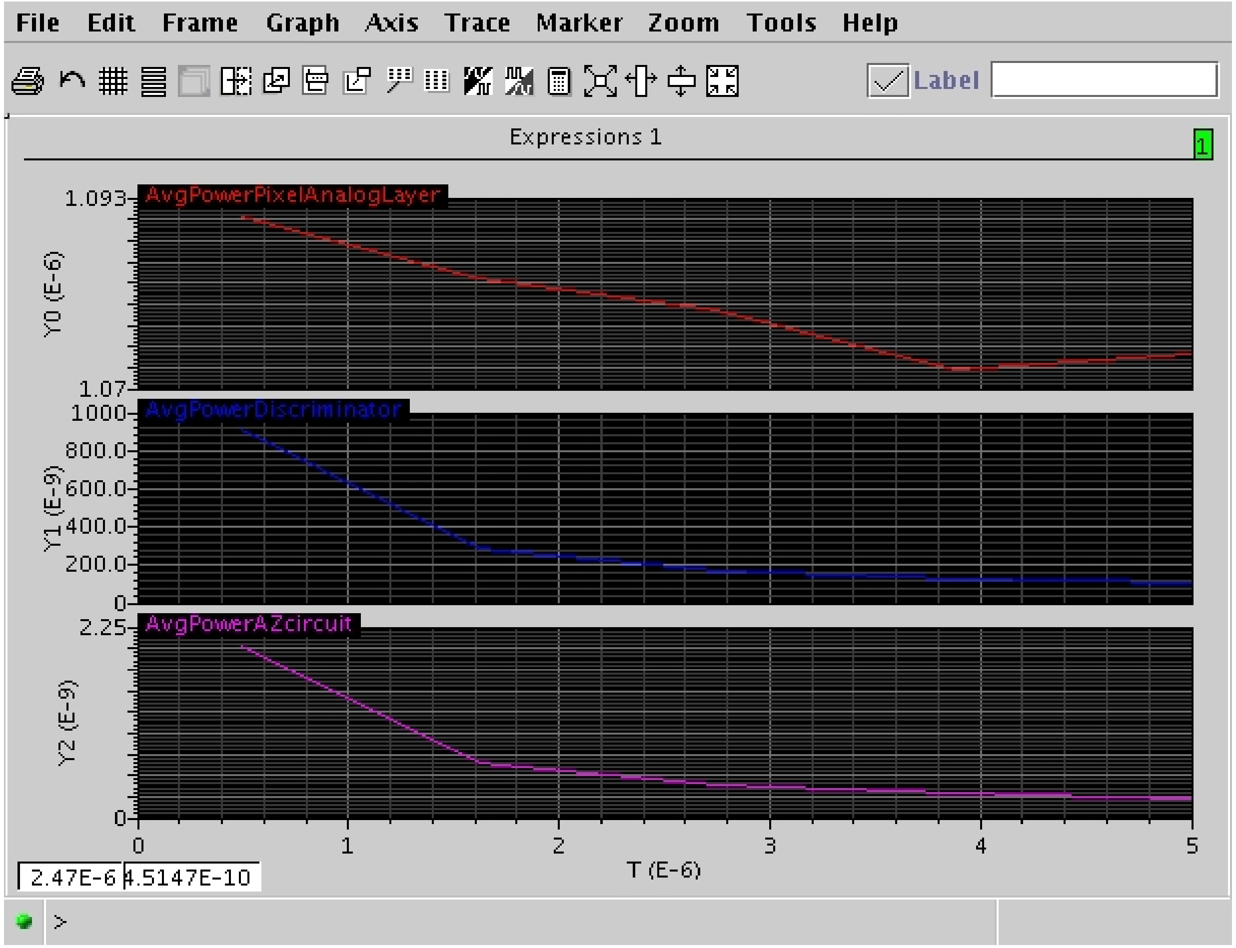
~0.8 mV RMS noise





500 e injected pulse ~ 70 mV

Pixel power consumption @ different integration times (500nS → 5µS)



Analog layer ~ 1µW

Discriminator:
1µW→200nW

Offset compensation:
2.25nW → 0.25 nW ???

Possible approach for column readout from Static RAM designs
(brief bibliography sketch)

SRAM technology bibliography examples:

- H. Nambu, K. Kanetani, K. Yamasaki, K Higea, M. Usami, T. Kusunoki, K. Yamaguchi,and N. Homma, "A 1.8ns Access, 550MHz 4.5Mb CMOS SRAM" in *IEEE Intern. Solid-State Circuits Conference Digest of Technical Papers*. Ieee, Feb. 1998, pp. 360-361.
- T. Uetake, Y. Maki, T. Nakadai, K. Yoshida, M. Susuki, and R. Nanjo, "A 1.0ns Access 770MHz 36Kb SRAM Macro" in *1999 Symp. On VLSI Circuits Digest of Technical Papers*, New York, June 1999, IEEE, pp. 109-110
- H. Nambu, K. Kanetani, K. Yamasaki, K Higeta, M. Usami, TY. Fujimura, K. Ando, T. Kusunoki, K. Yamaguchi, and N. Homma, "A 1.8ns Access, 550MHz 4.5Mb CMOS SRAM" *IEEE Journal of Solid-State Circuits*, vol.33, no. 11, pp. 1650-1657, Nov. 1998.

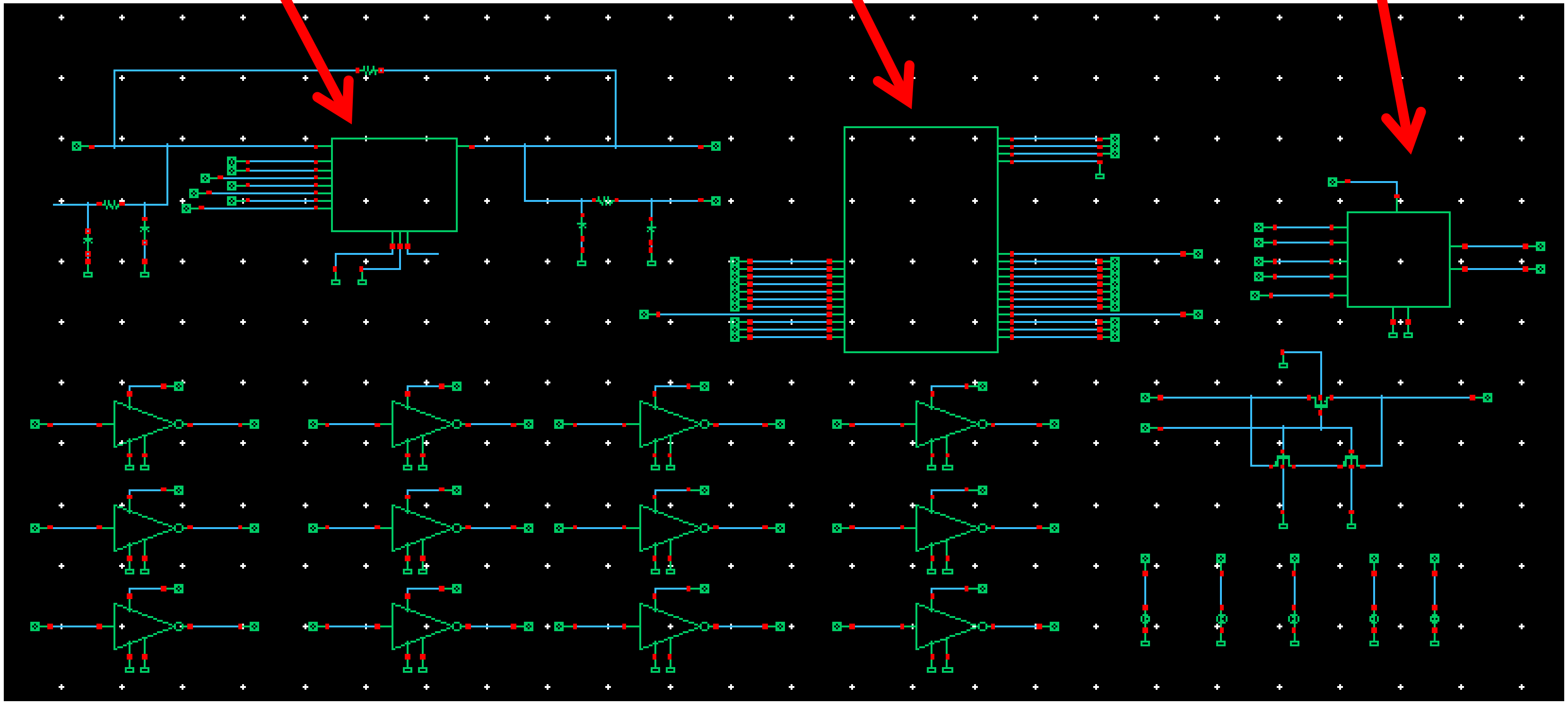
Fast column readout is possible.

End of Column digital readout (bitline bus parasitics included)

128 pixel (only output logic) column.
Signal collecting line parasitic resistance and Capacitance included!

VHDL-AMS Test bench

End of Column digital readout



VHDL-AMS test bench code

Column input pattern to be readout

vhdl.vhms (/mnt/homedir/spiriti/mimoroma4_oa/TB_mimoroma4/selgen1/vhdlams) - gedit (on babydugongo.roma3.infn.it)

```
      ncmp_EN      : out std_logic;
      nfired_read  : OUT std_logic_vector(127 downto 0)
    );
end selgen1;

architecture vhdlams of selgen1 is
-----------------------------------------------------------------------------------------
----  staircase generation constants ----------------------------------------------
   quantity vpos across ipos through Vsc_pos to Vrefanalog;
   quantity vneg across ineg through Vsc_neg to Vrefanalog;
   quantity vmid across imid through Vsc_mid to Vrefanalog;

   constant NcycleDlySC:         natural :=  0;
   constant NcycleStepSC:        natural := 10;
   constant NcycleAZ:            natural :=  1;
   constant VstepSC:             voltage := 10.0e-3;
   constant NumStep:             real := 2.0;
   constant MiddleValue:         voltage := 1.0;
   constant T:                   time     := 100 ns;

   signal pulsepos:          voltage:= MiddleValue;
   signal pulseneg:          voltage:= MiddleValue;
   signal Vrefec:            voltage:= MiddleValue;
-----------------------------------------------------------------------------------------
--                                                                   01234567890123456789012345678901
   constant nVout2_pattern:      std_logic_vector(127 downto 0):=X"AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAF0";
   constant num_row:             NATURAL := 16;
   constant novl:                TIME    := 1 ns;  -- era 4ns.
   constant sample_time:         TIME    := 10 ns;
   constant reset_time:          TIME    := 10 ns;

   constant precharge_time_EC:   TIME    := 1 ns;  -- era 8ns.
   constant sample_time_EC:      TIME    := 3 ns;  -- era 8ns.
   constant equilibrate_time_EC: TIME    := 3 ns;  -- era 8ns.
   constant read_fired_width:    TIME    := precharge_time_EC+sample_time_EC+novl+equilibrate_time_EC;
   constant read_fired_period:   TIME    := read_fired_width + novl ;
--   constant integration_time:    TIME    := (num_row*read_fired_period) + sample_time + novl  ;
   constant integration_time:    TIME    := 700 ns;
-- un ciclo comprende almeno un sample time + i tempi per leggere tutte le righe!!!
```

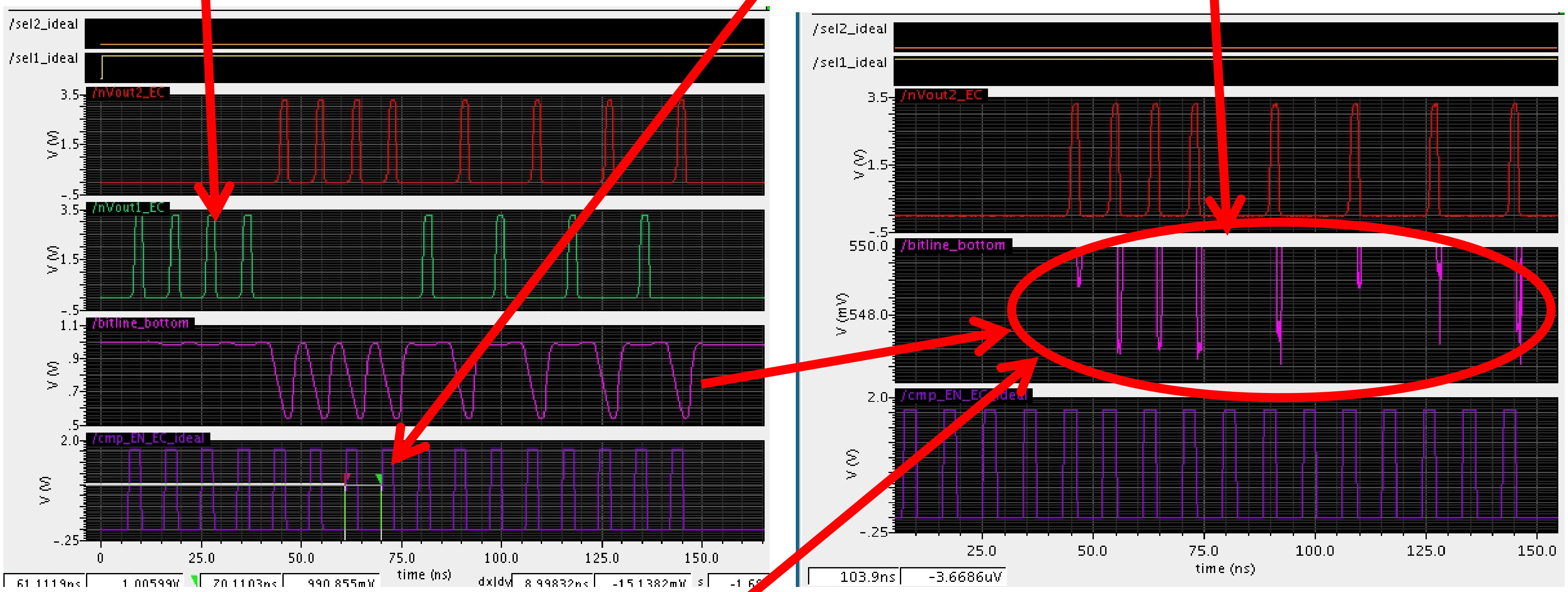
Ln 62, Col 100 | INS

Column readout timing simulation

Read out of first 16 bits. Pattern AAF0 correctly reproduced!

Read out time = 9 ns
9 nS→ ~111 MHz
Can be improved!

Transient noise Simulation
(no MonteCarlo)
Low frequency noise effect!



Static RAMS usually work with a signal also 10 times lower!!

Power consumption summary (NO OPTIMIZATION AT ALL)

Pixel power consumption summary (pitch 25 µm) = 335.2 -> 201.6 mW/cm*2

Integration time	500 nS	5 µS
Analog layer	1.093 µW	1.070 µW
Discriminator	1 µW	190 nW
Offset compensation	2.25 nW	0.25 nW

No power cut

End of Column digital readout power consumption summary (111MHz)

# Column	1	400 column => 1 cm 25 µm pitch
EC readout	36.7 µW	14.68 mW
Bitline	10.8 µW	4.32 mW
Pixel output buffers	6.7 µW *	2.68 mW

*** All output buffers in the column**

End of columnn analog readout power consumption to be evaluated. Order of magnitude lower than the analog one due to the sparsified readout!

Conclusions:

What, if any, of this work could be useful in the framwrork of the ALICE ITS upgrade project?

- **known-how?**
- **ideas?**
- **experience in testing?**