PRIN 2020 ideas: Background

Recall: KLEVER-CaI project for 2017 highly rated

- 74/75 for quality of research project (16/25 for PI CV in preselection)
- Continued progress on KLEVER
  - 2018 KLEVER test beam
  - AIDAinnova project
  - Tests of shashlyk at Protvino and DESY
  - Outcome of European Strategy
- Convergence with NA62x4
  - NA62x4 piggybacks completely on KLEVER for calorimetry and vetoes
  - More interest from NA62: new readout projects, including IRC/SAC

Structure a new proposal along similar lines, with significant updates:

“Development of calorimeters and veto detectors for experiments with high-intensity kaon beams”

WP1: Shashlyk	**WP3: SAV**
WP2: LAV	**WP4: Readout**

WP1: Shashlyk/MEC

Construction of a larger romashka prototype (e.g. 9x9) and test with beams at LNF/DESY/CERN starting from end 2022

1. Current tests and simulations show promise, but module has too much leakage to judge time performace
2. Simulation studies for performance optimization
3. Engineering studes for spy fiber routing, mechanics
4. Readout with FADCs as per WP4
5. Endpoint: full validation of MEC solution for NA62x4/KLEVER

WP2: LAV

Constuction of a few test sectors of a LAV module, to install next to NA62 for testing by 2023

1. Simulation and engineering studies
2. Readout with FADCs as per WP4
3. Critical need to understand if the LAVs need to be fully digitizied and at what rate
4. Possible to contemplate digitizing one or more LAV layers in NA62
5. Endpoint: fill validation of LAV solution for NA62x4/KLEVER

WP3: SAV

Construction of a fast Cerenkov SAC prototype, with multiple layers and possibly with oriented crystals

1. Similar in structure to our AIDAinnova project proposal
   NB: Our actual role in AIDAinnova is much more limited to material studies
2. Validation of materials (PbF2 vs PWO, etc.)
3. Choice of photodetectors
4. Validation of layer structure: study γ/n separation with simulation
5. Beam tests with photon and neutral hadron beams
6. Verify γ/n separation
7. Readout with FADCs as per WP4
8. If fully validated by 2023, possible use of new SAC in NA62
9. Question of oriented crystals to be coordinated with Laura
10. Endpoint: full validation of prototype for NA62x4/KLEVER

WP4: Readout

1. Demonstration of a WFD readout at 1 GHz with Gandalf, CAEN 27xx, DRS4, or similar board
   - Data reduction (at least zero suppression) implemented in FPGA
   - To be used immediately (2021) to read out the IRC and SAC in NA62, as well as in all tests in WPs 1-3
2. Conceptual design of a DAQ architecture for NA62x4/KLEVER incorporating such readout
3. Endpoint: Conceptual design of DAQ architiecture, proof of principle, and identification of all performace parameters necessary to guide choices for implementaion in NA62x4/KLEVER

IRC/SAC readout with FADCs

Make contact with discussions about future readout for NA62x4

- Presentation by Giovanna at Future meeting, 04 Sep 20
  - General characteristics of triggerless readout architecture
  - Implicit assumption of non-digitizing readout: TDCs
- Follow-up meeting 14 Oct 20
  - Persuasive case for FADCs for main calorimeter, SAV at ~1 GHz
    - Time resolution < 200 ps
    - Double-pulse separation ~ 1 ns
  - Skepticism of need for FADCs e.g. for STRAWS
  - No conclusions about LAVs (possible FADC digitization at lower rate)
  - Need to gain experience with use of high-speed FADCs e.g. in NA62

IRC/SAC readout with FADCs

Dust-off idea of FADCs for IRC/SAC in NA62 for 2021

- Acquire data in parallel with at least one of two existing readout schemes
- Study utility of reducing random-veto in NA62
- Possible study of data-reduction algorithms
  - E.g.: zero-suppression with minimal loss

Possible test of FADC readout for LAVs in 2022+

- LAV prototype in area e.g. as part of new PRIN project
- Partial instrumentation of one of existing LAVs

Possible digitizers

CAEN 27xx

- Built-in SoC (ZYNC Ultrascale+) with FPGA for user programming
- Could implement data-reduction in front-end
- Ideal: V2751: 16 ch, real 1 GS/s sampling, 14 bit – not available
- Current availability: V2740: 64 ch, 125 GS/s, 14 bit: €14750 + tax

Gandalf

- In our possession – acquired in 2012 (?) for this purpose!
- Based on Virtex-5 FPGA (Xilinx)
- ADC mezzanine card: 8 ch, 500 GS/s, 12 bit: possible to interleave?
- Mezzanine card with Spartan 6 FPGA and 4 SFP ports
- Basic work on incorportation with DAQ done by Ven:
- Lock NA62 clock, receive L0 triggers up to 1 MHz, prepare minimal output data
- Need to fully integrate with DAQ for high-throughput readout

DRS4

- High-speed, high-analog bandwidth, low cost
- 4-ch evaluation board with USB interface available from PSI
- Suitable for experimentation but can’t be incorporated in readout as is