

CYGNO

Photomultiplier DAQ development

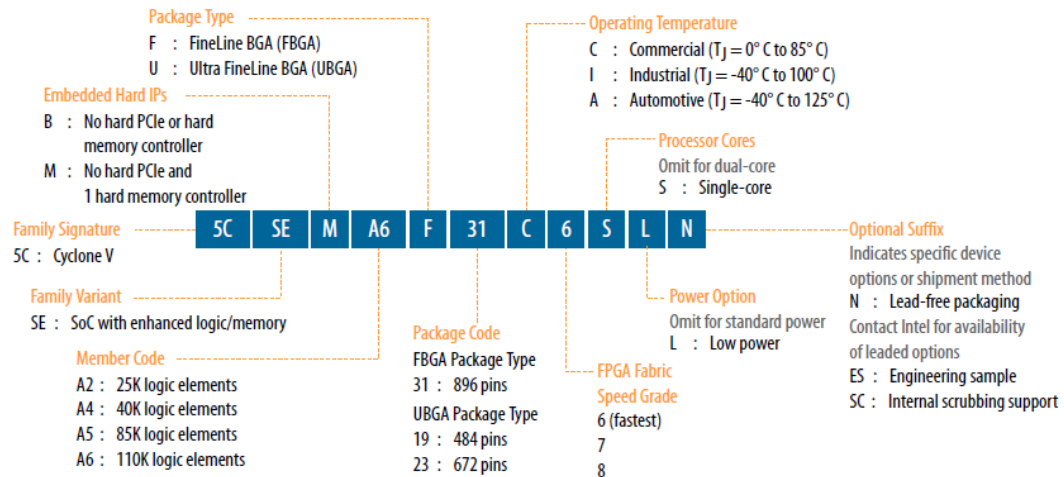
Herman Pessoa Lima Jr
Danilo Cardoso
Tiago Oliveira

28 Oct 2020

- Survey and selection of technologies/devices: ADC, FPGA, μ C. **DONE**
- Drawing electrical schematics: analog input circuit, ADC connections, microcontroller circuit. **DONE**
- Survey of other FPGA due to software licence issue (Quartus Prime). New FPGA family selected: **Cyclone V**. **DONE**
- Second ADC option selected due to transceiver speed limitation in Cyclone V.
- Drawing electrical schematics: FPGA circuit. **DOING**
- Possible design change: ~~4 input channels instead of 8 because of routing restrictions with new ADC.~~ → **8 channels is possible (bigger FPGA package)**
- **Defining and drawing ADC to FPGA data buses (16 x 4 LVDS channels). DOING**
- **Learning how to use the ARM processor in the FPGA to implement the Ethernet and USB module interfaces. No need of the PIC controller. DOING**

Cyclone V SoC

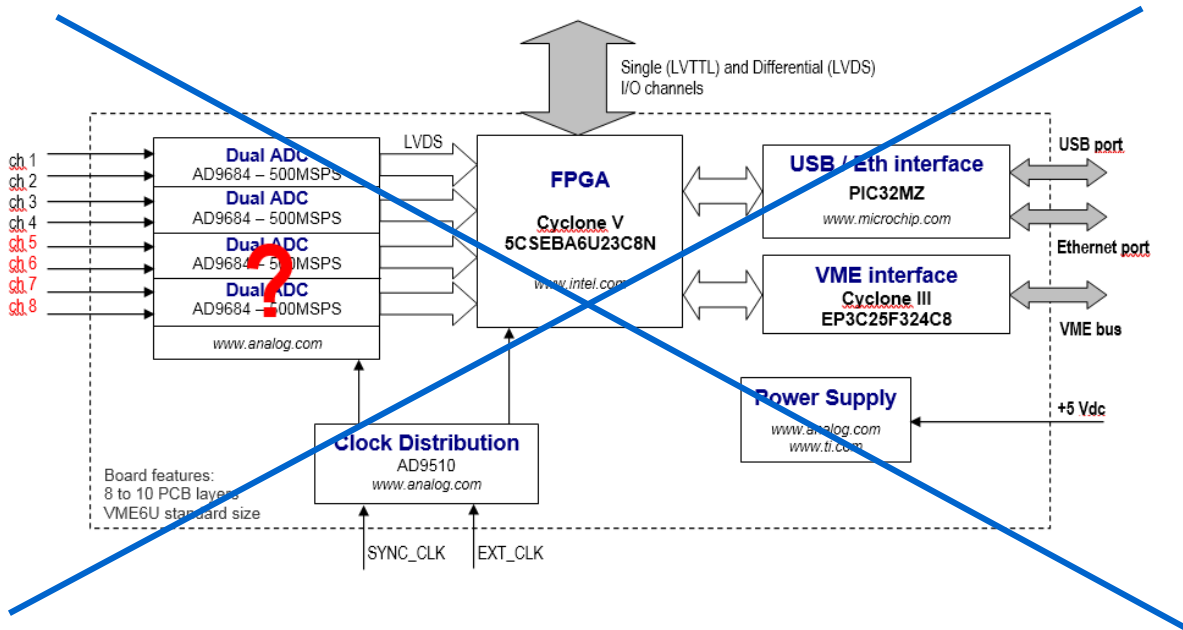
Variant	Description
Cyclone® V E	Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications
Cyclone® V GX	Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications
Cyclone® V GT	The FPGA industry's lowest cost and lowest power requirement for 6.144 Gbps transceiver applications
Cyclone® V SE	SoC with integrated Arm® -based HPS
Cyclone® V SX	SoC with integrated Arm® -based HPS and 3.125 Gbps transceivers
Cyclone® V ST	SoC with integrated Arm® -based HPS and 6.144 Gbps transceivers



final choice

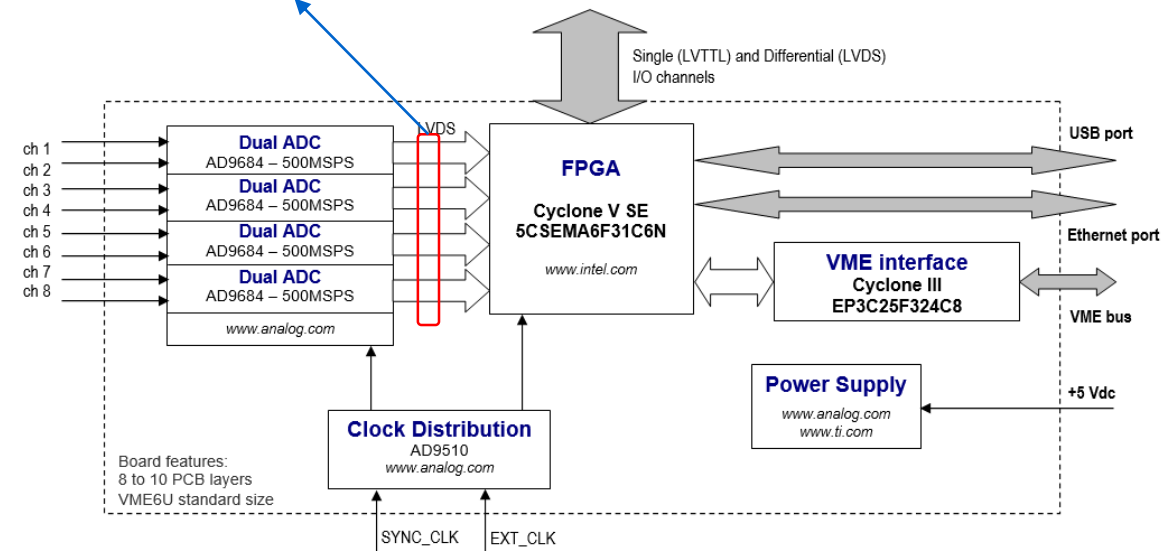
Mouser.com	Date	USD
5CSXFC6C6U23C8N 110k LEs, 288 IOs, 72 LVDS inputs 6 x 3,125Gbps, UBGA 672 pins	06/10/20	209,78
5GSTFD6D5F31I7N 110k LEs, 288 IOs, 9 x 6,144Gbps, FBGA 896 pins	06/10/20	386,83
5CSEBA6U23C8N 110k LEs, 288 IOs, 37 LVDS inputs no transceivers, UBGA 672 pins	13/10/20	164,28
5CSEMA6F31C6N 110k LEs, 288 IOs, 72 LVDS inputs no transceivers, FBGA 896 pins	23/10/20	279,33

* ALL with a 'Dual ARM Cortex-A9 925 MHz' processor



Last meeting

next slides

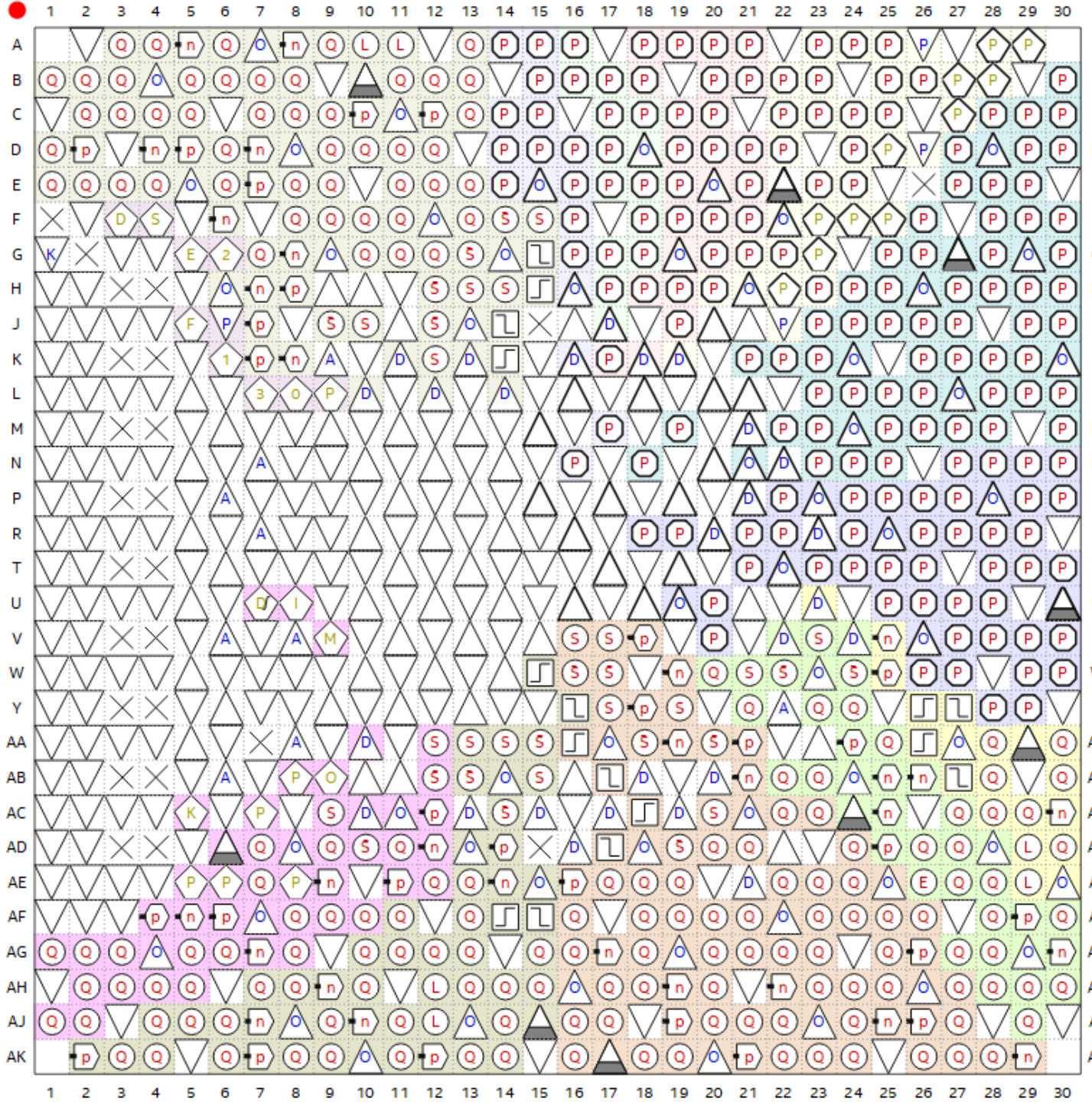


TODAY

Cyclone V SoC 5CSEMA6F31C6N

Package: FBGA
896 pins, 31x31mm
72 LVDS input channels
(DIFFIO_RX_)

Dedicated Tx/Rx Channel	F896	Bank Number
DIFFIO_RX_B1n	AE12	3A
DIFFIO_RX_B1p	AD11	3A
DIFFIO_RX_B3n	AD10	3A
DIFFIO_RX_B3p	AC9	3A
DIFFIO_RX_B5n	AE7	3A
DIFFIO_RX_B5p	AD7	3A
DIFFIO_RX_B7n	AF5	3A
DIFFIO_RX_B7p	AF4	3A
DIFFIO_RX_B10n	AH2	3A
DIFFIO_RX_B10p	AG1	3A
DIFFIO_RX_B11n	AB12	3A
DIFFIO_RX_B11p	AA12	3A
DIFFIO_RX_B14n	AJ2	3A
DIFFIO_RX_B14p	AJ1	3A
DIFFIO_RX_B15n	AD12	3A
DIFFIO_RX_B15p	AC12	3A
DIFFIO_RX_B18n	AG11	3B
DIFFIO_RX_B18p	AF11	3B
DIFFIO_RX_B19n	AB13	3B
DIFFIO_RX_B19p	AA13	3B
DIFFIO_RX_B22n	AF13	3B
DIFFIO_RX_B22p	AE13	3B
DIFFIO_RX_B23n	AE14	3B
DIFFIO_RX_B23p	AD14	3B
DIFFIO_RX_B26n	AG13	3B
DIFFIO_RX_B26p	AG12	3B
DIFFIO_RX_B27n	AC14	3B
DIFFIO_RX_B27p	AB15	3B
DIFFIO_RX_B30n	AH14	3B
DIFFIO_RX_B30p	AH13	3B
DIFFIO_RX_B31n	AF15	3B
DIFFIO_RX_B31p	AF14	3B
DIFFIO_RX_B34n	AK11	3B
DIFFIO_RX_B34p	AJ11	3B
DIFFIO_RX_B35n	AA15	3B
DIFFIO_RX_B35p	AA14	3B
DIFFIO_RX_B38n	AH15	3B
DIFFIO_RX_B38p	AG15	3B
DIFFIO_RX_B39n	Y16	3B
DIFFIO_RX_B39p	W15	3B
DIFFIO_RX_B42n	AF18	4A
DIFFIO_RX_B42p	AE17	4A
DIFFIO_RX_B43n	W16	4A
DIFFIO_RX_B43p	V16	4A
DIFFIO_RX_B46n	AH20	4A
DIFFIO_RX_B46p	AG21	4A
DIFFIO_RX_B47n	AB17	4A
DIFFIO_RX_B47p	AA16	4A
DIFFIO_RX_B50n	AK18	4A
DIFFIO_RX_B50p	AJ17	4A



Connections ADC->FPGA (LVDS)

DIFFIO_RX_B51n	W17	4A	DIFFIO_RX_R23p	Y26	5B
DIFFIO_RX_B51p	V17	4A	DIFFIO_RX_R23n	Y27	5B
DIFFIO_RX_B54n	AG20	4A	DIFFIO_RX_T1p	H15	8A
DIFFIO_RX_B54p	AF19	4A	DIFFIO_RX_T1n	G15	8A
DIFFIO_RX_B55n	AD17	4A	DIFFIO_RX_T3p	C13	8A
DIFFIO_RX_B55p	AC18	4A	DIFFIO_RX_T3n	B12	8A
DIFFIO_RX_B58n	AE19	4A	DIFFIO_RX_T5p	F15	8A
DIFFIO_RX_B58p	AE18	4A	DIFFIO_RX_T5n	F14	8A
DIFFIO_RX_B59n	AA18	4A	DIFFIO_RX_T7p	D11	8A
DIFFIO_RX_B59p	Y17	4A	DIFFIO_RX_T7n	D10	8A
DIFFIO_RX_B62n	AF21	4A	DIFFIO_RX_T9p	K14	8A
DIFFIO_RX_B62p	AF20	4A	DIFFIO_RX_T9n	J14	8A
DIFFIO_RX_B63n	AA19	4A	DIFFIO_RX_T11p	E9	8A
DIFFIO_RX_B63p	Y18	4A	DIFFIO_RX_T11n	D9	8A
DIFFIO_RX_B66n	AF24	4A	DIFFIO_RX_T13p	H14	8A
DIFFIO_RX_B66p	AF23	4A	DIFFIO_RX_T13n	G13	8A
DIFFIO_RX_B67n	AD19	4A	DIFFIO_RX_T15p	F13	8A
DIFFIO_RX_B67p	AC20	4A	DIFFIO_RX_T15n	E13	8A
DIFFIO_RX_B70n	AE23	4A	DIFFIO_RX_T17p	H8	8A
DIFFIO_RX_B70p	AE22	4A	DIFFIO_RX_T17n	G8	8A
DIFFIO_RX_B71n	W19	4A	DIFFIO_RX_T19p	E12	8A
DIFFIO_RX_B71p	V18	4A	DIFFIO_RX_T19n	D12	8A
DIFFIO_RX_B74n	AD21	4A	DIFFIO_RX_T21p	H13	8A
DIFFIO_RX_B74p	AD20	4A	DIFFIO_RX_T21n	H12	8A
DIFFIO_RX_B75n	AA20	4A	DIFFIO_RX_T23p	F11	8A
DIFFIO_RX_B75p	Y19	4A	DIFFIO_RX_T23n	E11	8A
DIFFIO_RX_B78n	AC23	4A	DIFFIO_RX_T25p	J7	8A
DIFFIO_RX_B78p	AC22	4A	DIFFIO_RX_T25n	H7	8A
DIFFIO_RX_B79n	AB21	4A	DIFFIO_RX_T27p	B6	8A
DIFFIO_RX_B79p	AA21	4A	DIFFIO_RX_T27n	B5	8A
DIFFIO_RX_R2n	AC25	5A	DIFFIO_RX_T29p	K12	8A
DIFFIO_RX_R4p	W20	5A	DIFFIO_RX_T29n	J12	8A
DIFFIO_RX_R4n	Y21	5A	DIFFIO_RX_T31p	G12	8A
DIFFIO_RX_R6p	W21	5A	DIFFIO_RX_T31n	G11	8A
DIFFIO_RX_R6n	W22	5A	DIFFIO_RX_T33p	K7	8A
DIFFIO_RX_R8p	AB22	5A	DIFFIO_RX_T33n	K8	8A
DIFFIO_RX_R8n	AB23	5A	DIFFIO_RX_T35p	G10	8A
DIFFIO_RX_R9p	AA24	5A	DIFFIO_RX_T35n	F10	8A
DIFFIO_RX_R9n	AB25	5A	DIFFIO_RX_T37p	J10	8A
DIFFIO_RX_R11p	Y23	5A	DIFFIO_RX_T37n	J9	8A
DIFFIO_RX_R11n	Y24	5A	DIFFIO_RX_T39p	F9	8A
DIFFIO_RX_R13p	V23	5A	DIFFIO_RX_T39n	F8	8A
DIFFIO_RX_R13n	W24	5A			
DIFFIO_RX_R15p	AD26	5A			
DIFFIO_RX_R15n	AC27	5A			
DIFFIO_RX_R17p	W25	5B			
DIFFIO_RX_R17n	V25	5B			
DIFFIO_RX_R19p	AB30	5B			
DIFFIO_RX_R19n	AA30	5B			
DIFFIO_RX_R21p	AA26	5B			
DIFFIO_RX_R21n	AB27	5B			

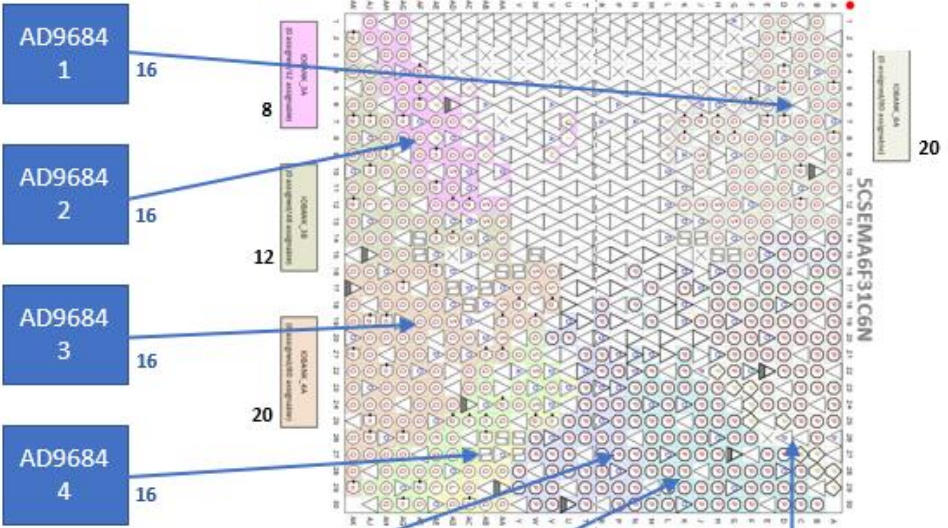
FRONT PANEL

CLOCK
sector

POWER
sector

VME FPGA

BACK PANEL

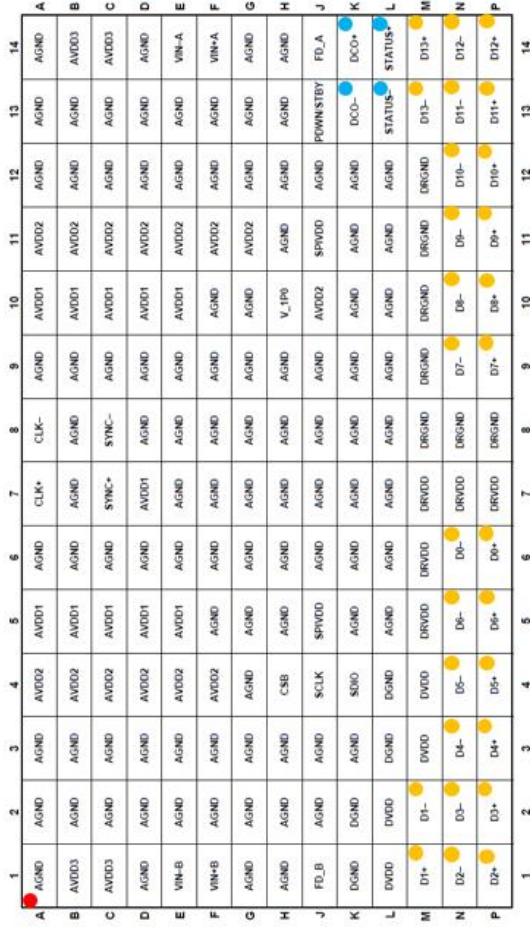


Ethernet
conn

USB
conn

GPIO
conn

ADC connections being defined



ADC data	ADC pin	FPGA pin ADC 1	FPGA pin ADC 2	FPGA pin ADC 3	FPGA pin ADC 4
DCO+	K14	K14	AF14		
DCO-	K13	J14	AF15		
STS+	L14	F9	AG1		
STS-	L13	F8	AH2		
D13+	M14	H8	AJ1		
D13-	M13	G8	AJ2		
D12+	P14	J7	AF4		
D12-	N14	H7	AF5		
D11+	P13	K7	AD7		
D11-	N13	K8	AE7		
D10+	P12	J10	AC9		
D10-	N12	J9	AD10		
D9+	P11	G10	AF11		
D9-	N11	F10	AG11		
D8+	P10	E9	AJ11		
D8-	N10	D9	AK11		
D7+	P9	K12	AA12		
D7-	N9	J12	AB12		
D6+	P6	H13	AC12		
D6-	N6	H12	AD12		
D5+	P5	G12	AD11		
D5-	N5	G11	AE12		
D4+	P4	F11	AA13		
D4-	N4	E11	AB13		
D3+	P3	D11	AE13		
D3-	N3	D10	AF13		
D2+	P2	H14	AG12		
D2-	N2	G13	AG13		
D1+	P1	F13	AA14		
D1-	M1	E12	AB15		
	M2	D12	AC14		

