CYGNO
Photomultiplier DAQ development status

Herman Pessoa Lima Jr
Danilo Cardoso
Tiago Oliveira

14 Oct 2020

CBPF
Centro Brasileiro de Pesquisas Físicas

CBPF
Centro Brasileiro de Pesquisas Físicas

Summary

- Survey and selection of technologies/devices: ADC, FPGA, µC. **DONE**
- Drawing electrical schematics: analog input circuit, ADC connections, microcontroller circuit. **DONE**
- Survey of other FPGA due to software licence issue (Quartus Prime). New FPGA family selected: **Cyclone V**. **DONE**
- Second ADC option selected due to transceiver speed limitation in Cyclone V.
- Drawing electrical schematics: FPGA circuit. **DOING**
- Possible design change: 4 input channels instead of 8 because of routing restrictions with new ADC.

Cyclone V SoC

	Product Line	Cyclone V SE SoCs[1]				Cyclone V SX SoCs[1]				Cyclone V ST SoCs[1]	
		5CSEA2	5CSEA4	5CSEA5	5CSEA6	5CSXC2	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
Resources	LEs (K)	25	40	85	110	25	40	85	110	85	110
	ALMs	9,434	15,094	32,075	41,509	9,434	15,094	32,075	41,509	32,075	41,509
	Registers	37,736	60,376	128,300	166,036	37,736	60,376	128,300	166,036	128,300	166,036
	M10K memory blocks	140	270	397	557	140	270	397	557	397	557
	M10K memory (Kb)	1,400	2,700	3,970	5,570	1,400	2,700	3,970	5,570	3,970	5,570
	MLAB memory (Kb)	138	231	480	621	138	231	480	621	480	621
	Variable-precision DSP blocks	36	84	87	112	36	84	87	112	87	112
	18 x 18 multipliers	72	168	174	224	72	168	174	224	174	224
Clocks, Maximum I/O Pins, and Architectural Features	Processor cores (ARM Cortex-A9)	Single or dual	Single or dual	Single or dual	Single or dual	Dual	Dual	Dual	Dual	Dual	Dual
	Maximum CPU clock frequency (MHz)	925	925	925	925	925	925	925	925	925	925
	Global clock networks	16	16	16	16	16	16	16	16	16	16
	PLLs[2] (FPGA)	5	5	6	6	5	5	6	6	6	6
	PLLs (HPS)	3	3	3	3	3	3	3	3	3	3
	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5,3.3									
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12, HiSpi, SLVS, Sub-LVDS									
	LVDS channels (receiver/transmitter)	37/32	37/32	72/72	72/72	37/32	37/32	72/72	72/72	72/72	72/72
	Transceiver count (3.125 Gbps)	–	–	–	–	6	6	9	9	–	–
	Transceiver count (6.144 Gbps)[3]	–	–	–	–	–	–	–	–	9[4]	9[4]
	PCIe hardened IP blocks (Gen1)[5]	–	–	–	–	2	2	2	2	–	–
	PCIe hardened IP blocks (Gen2)	–	–	–	–	–	–	–	–	2	2
	GPIOs (FPGA)	145	145	288	288	145	145	288	288	288	288
	GPIOs (HPS)	181	181	181	181	181	181	181	181	181	181
	Hard memory controllers[6] (FPGA)	1	1	1	1	1	1	1	1	1	1
	Hard memory controllers[6] (HPS)	1	1	1	1	1	1	1	1	1	1
	Memory devices supported	DDR3, DDR2, LPDDR2									
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count											
U484 pin (19 mm, 0.8 mm pitch)		66, 151 0	66, 151 0	66, 151 0	66, 151 0						
U672 pin (23 mm, 0.8 mm pitch)		145, 181 0	145, 181 0	145, 181 0	145, 181 0	145, 181 6	145, 181 6	145, 181 6	145, 181 6		
F896 pin (31 mm, 1.0 mm pitch				288, 181 0	288, 181 0			288, 181 9	288, 181 9	288, 181 9	288, 181 9

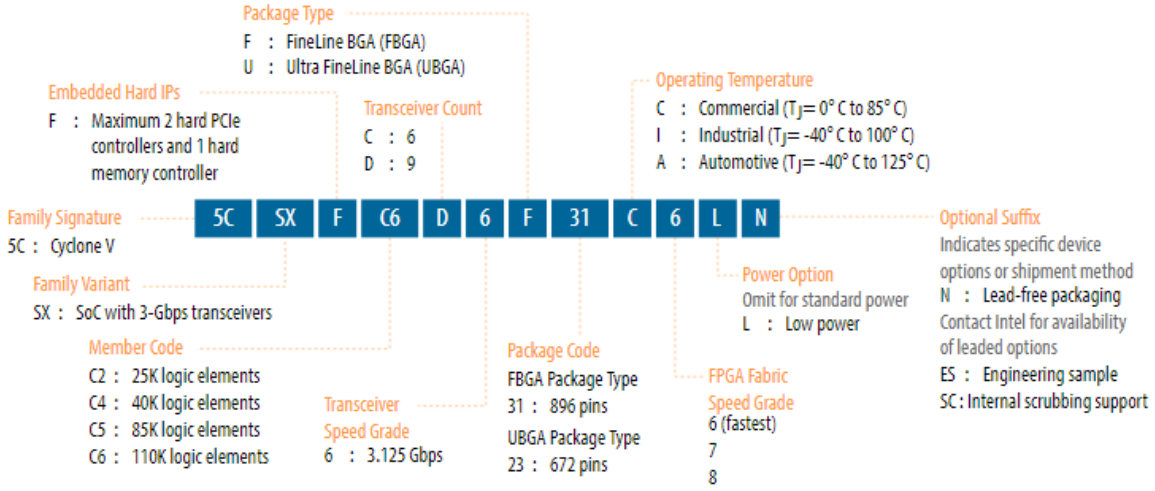
Notes:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.
2. The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.
3. Automotive grade Cyclone V GT FPGAs include a 5 Gbps transceiver.
4. Transceiver counts shown are for ≤ 5 Gbps.
   The 6 Gbps channel count support depends on package and channel usage.
   Refer to Cyclone V Device Handbook Volume 2: Transceivers for guidelines.
5. One PCIe hard IP block in U672 package.
6. With 16 and 32 bit ECC support.

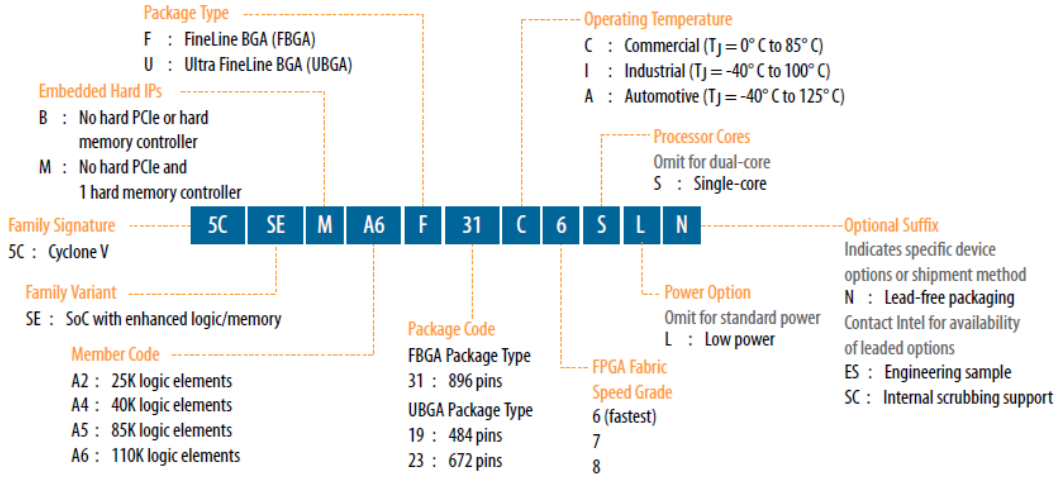
66, 151 / 0 — Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 3.125 Gbps or 5 Gbps transceiver count.

Pin migration (same V_{cc}, GND, ISP, and input pins). User I/O pins may be less than labelled for pin migration.

For SoCs: Pin migration is only possible if you use only up to 138 GPIOs.

Cyclone V SoC





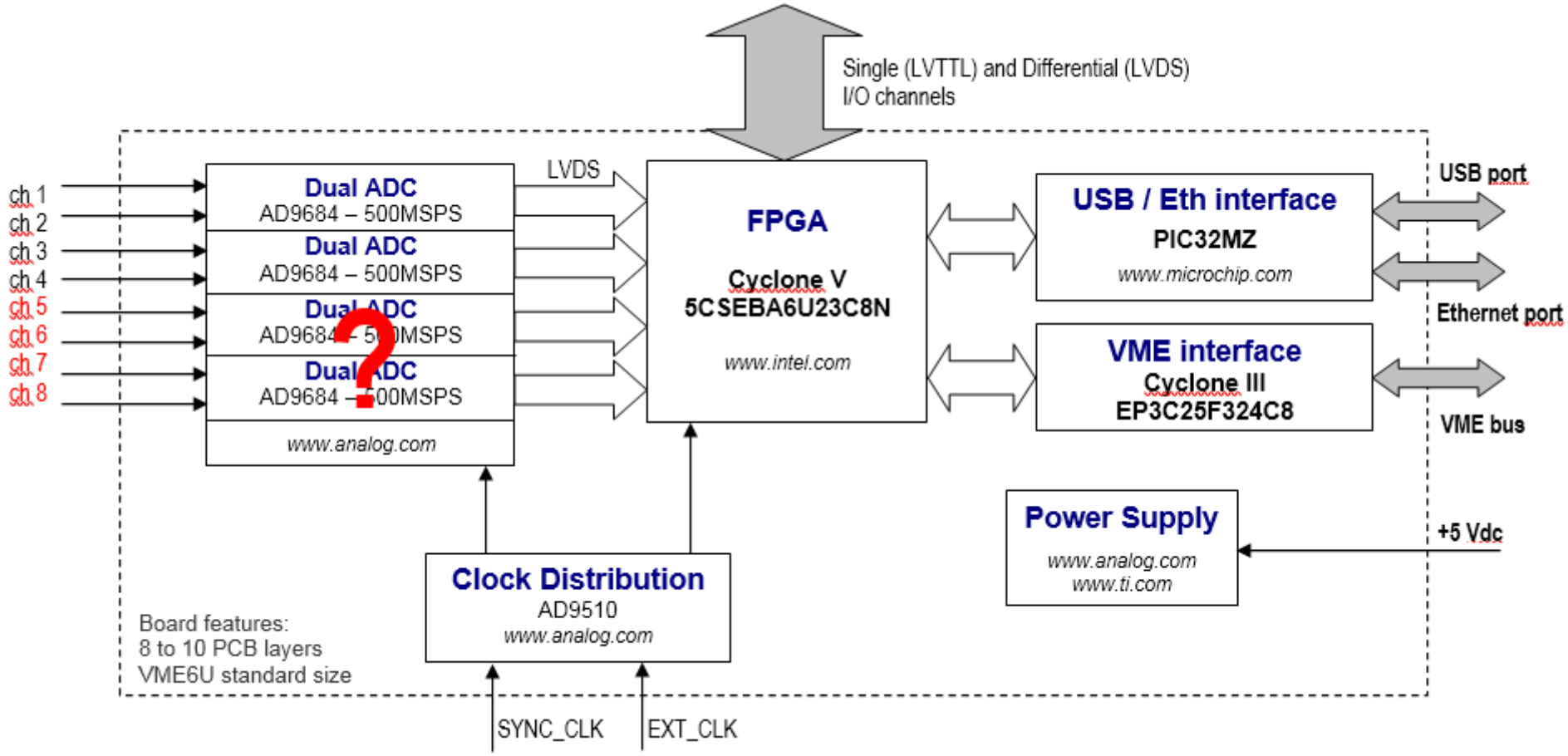
Variant	Description
Cyclone® V E	Optimized for the lowest system cost and power requirement for a wide spectrum of general logic and DSP applications
Cyclone® V GX	Optimized for the lowest cost and power requirement for 614 Mbps to 3.125 Gbps transceiver applications
Cyclone® V GT	The FPGA industry's lowest cost and lowest power requirement for 6.144 Gbps transceiver applications
Cyclone® V SE	SoC with integrated Arm® -based HPS
Cyclone® V SX	SoC with integrated Arm® -based HPS and 3.125 Gbps transceivers
Cyclone® V ST	SoC with integrated Arm® -based HPS and 6.144 Gbps transceivers

Mouser.com	Date	USD
5CSXFC6C6U23C8N 110k LEs, 288 IOs, 72 LVDS inputs 6 x 3,125Gbps, UBGA 672 pins	06/10/20	**209,78**
5CSTFD6D5F31I7N 110k LEs, 288 IOs, 9 x 6,144Gbps, FBGA 896 pins	06/10/20	**386,83**
5CSEBA6U23C8N 110k LEs, 288 IOs, 72 LVDS inputs no transceivers, UBGA 672 pins	13/10/20	**164,28**

* ALL with a 'Dual ARM Cortex-A9 925 MHz' processor

best choice

Module overview



Development tools

These tools could be useful for helping and to speed-up the development of firwmare and hardware, as well as to evaluate the ADC performance

CYGNO Photomultiplier DAQ - Priority List for development and tests

Herman Lima - CBPF

	Mouser #	Mfr. #	Manufacturer	Description	Qty	Price (USD)	Ext.: (USD)	Ext.: (Euro)
1	579-DM320007	DM320007	Microchip	Development Boards & Kits - PIC / DSPIC PIC32 Starter Kit with FPU (EF)	1	106,22	106,22	106,22
2	584-AD9684-500EBZ	AD9684-500EBZ	Analog Devices	Data Conversion IC Development Tools Dual 14b 500MS/s evaluation board	1	894,38	894,38	787,84
3	584-HSC-ADC-EVALEZ	HSC-ADC-EVALEZ	Analog Devices	Data Conversion IC Development Tools	1	1.494,29	1.494,29	1316,29
						TOTAL	**2.494,89**	**2210,35**

Ref prices: www.mouser.com - 13 Oct 2020