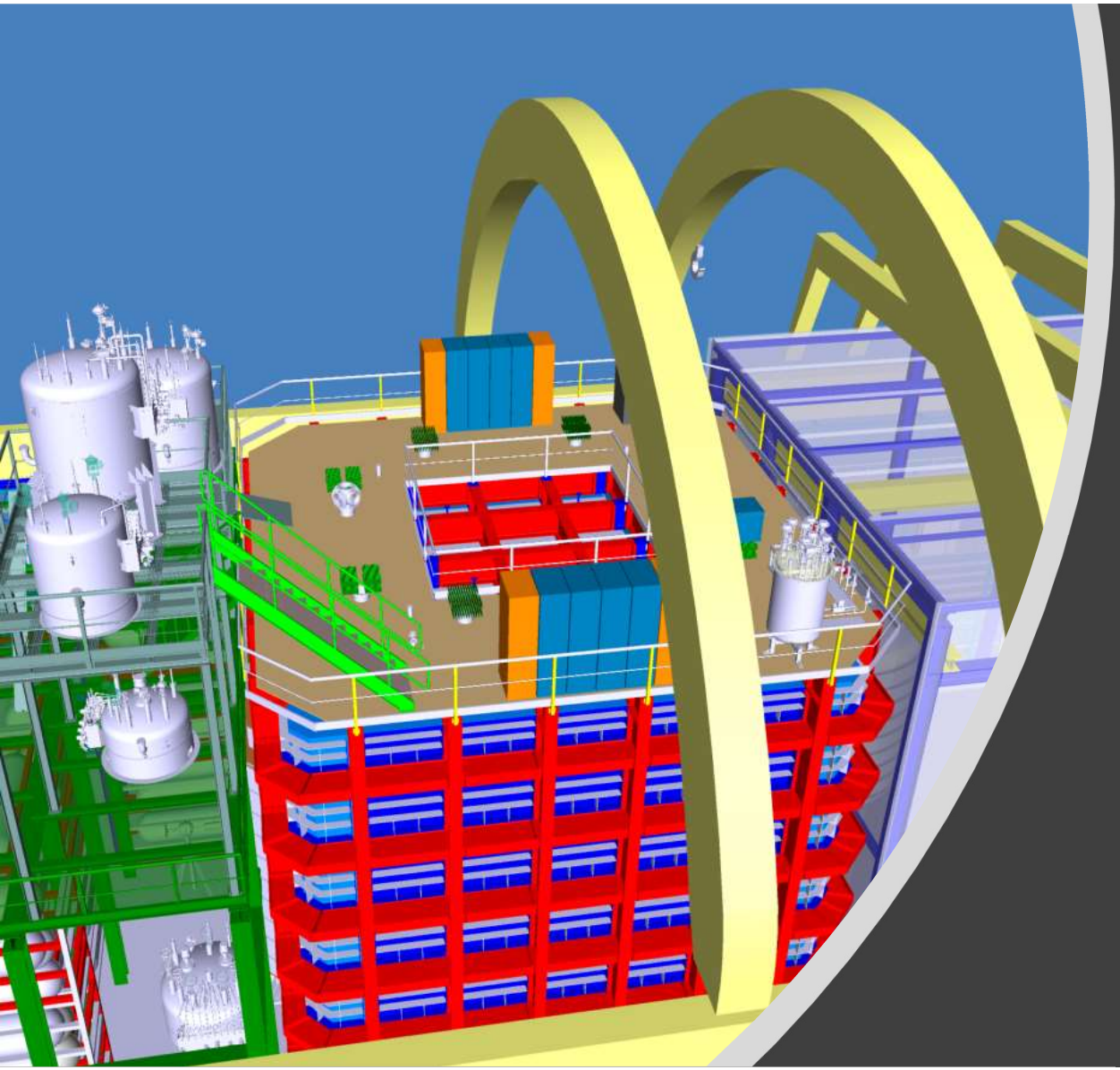


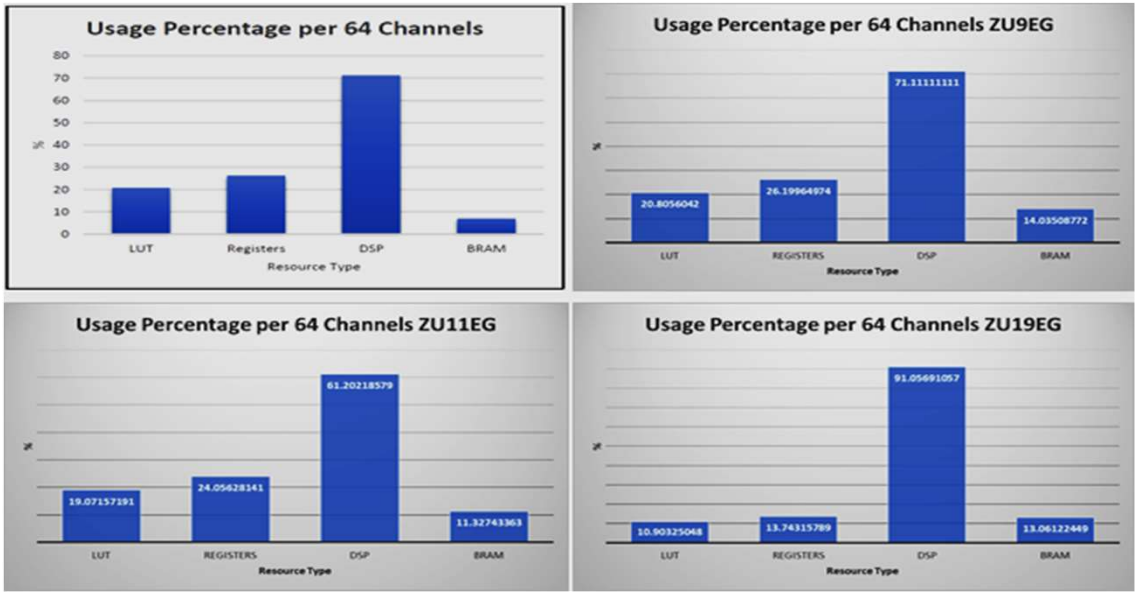
DarkSide-20K DAQ/CAEN meeting

- Current State of the VX2740
    - Issues?
        - PCB manufacture, problem resolved, expect 5, 12 later on
    - New FW availability?
        - New FW include DPP/DAW
    - Board availability?
        - 5 soon, ordered 1+6 for DS
    - Chip selection (see next slide)
        - Use of the large FPGA (-19)
        - Triumf has one of the small FPGA (-11)

- Resource issue for the DSP section
- DSP used for FIR filter (Masoud)

- Include CAEN infrastructure occupancy
- 50% URAM, 19% BRAM, 5% DSP, 3%LUT

- Need further investigation for the DS VX2740 selection
- PCB layout identical
  - Is -11 purchase an option for DS?



Source: Masoud Mokhtari

- Development / Operation at Triumf

  - Dynamic Acquisition Window (DAW) already available on the Triumf board?
  - ➢ NO, initial FW doesn't have the DAW

  - Re-start FW build through CAEN facility (from Triumf)
    - For user code integration – Luca(CAEN), Bryerton, Lars, Erick –
  - ➢ Already working on it

  - Hooks(User block interface) documentation
    - ADC output format passed to the USER block?
    - Fixed Event format at the DDR4?
      - ➢ Use the current data format for any other type of info that need to be added
    - Additional user interface to GPIO and SYNCIN
    - Local bus interface: AXI-4?
      - ➢ AXI-4 for registers, AXI wide bus for data

  - ➢ Documentation will be produced for FW and ARM description/usage

- DS-1T prototype (late spring'21 at the earliest)

  - Use scope mode in long waveforms (~6ms)
  - ➢ In scope mode, data are streamed directly to the DDR4
  - ➢ Need to test this configuration with our Triumf -11 board

  - External trigger on all boards (6 units)
  - ➢ Std external Trigger available on the VX2740, Trigger combination can be done as for the V1725 (ds-proto)

- DS Requests/ Questions:

  - DAW/DPP mode: Additional "virtual channels", containing waveform-like data, for derived quantities like "sums of the input signals over subset of channels"?
  - ➢ NO… requires major FW rework.
  - ➢ Option to use one of the 64 ch for the sum64 (“loose” a channel)

  - DAC output: Doc: selection of a channel as analog output. Is sum of channels possible?
  - ➢ DAC access from User code, make digital sum and send it to DAC

  - Proposal for Signal interface to VX2740 in the DS-20k configuration (see below)
    - Use of the SYNCIN for encoded trigger
    - Additional user interface to GPIO

- **Firmware development**

  - Masoud Mokhtari
    - FIR code development (comparison LUTs vs DSPs)
    - Optimization of resource use (minimal)
    - Data extraction through Midas DAQ.

  - Continuation of Masoud work with students, supervised by Lars Martin, Bryerton Shaw
    - Kota Chang / part-time (Sep'20-Dec'20)
    - Erick Chmelyk / full-time (Sep'20-Dec'20)
    - Tyler Verwoerd / full-time (Jan'21-Apr'21)
      - Filtering algorithms
      - Code integration (FPGA)
      - Acquisition testing

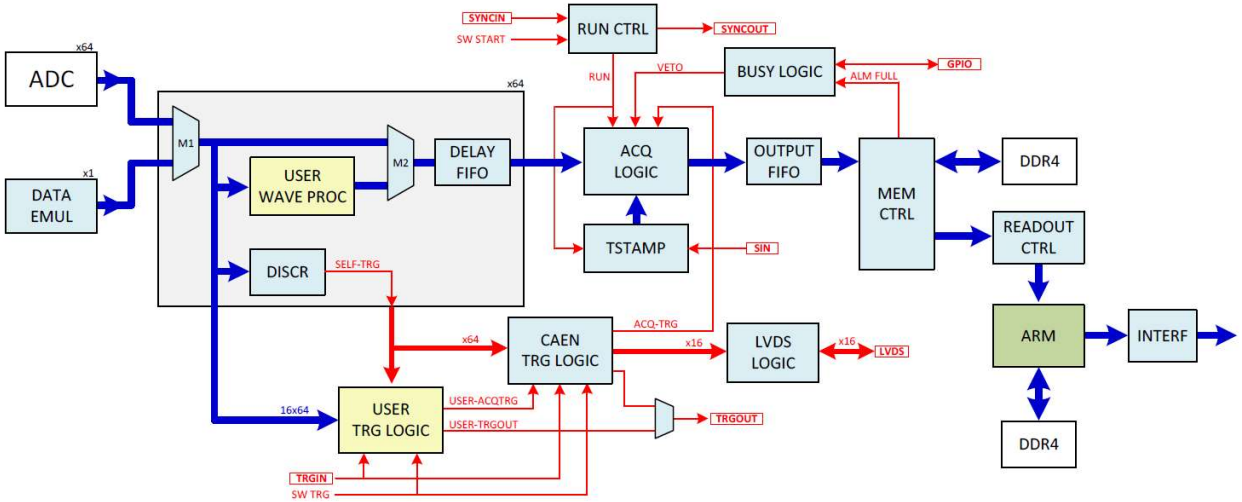


Fig. 2.1: Block Diagram of the FW "Scope"

New current FW:
64x4096 per channel
50% URAM
1 URAM block per channel
1 URAM -> 131 us

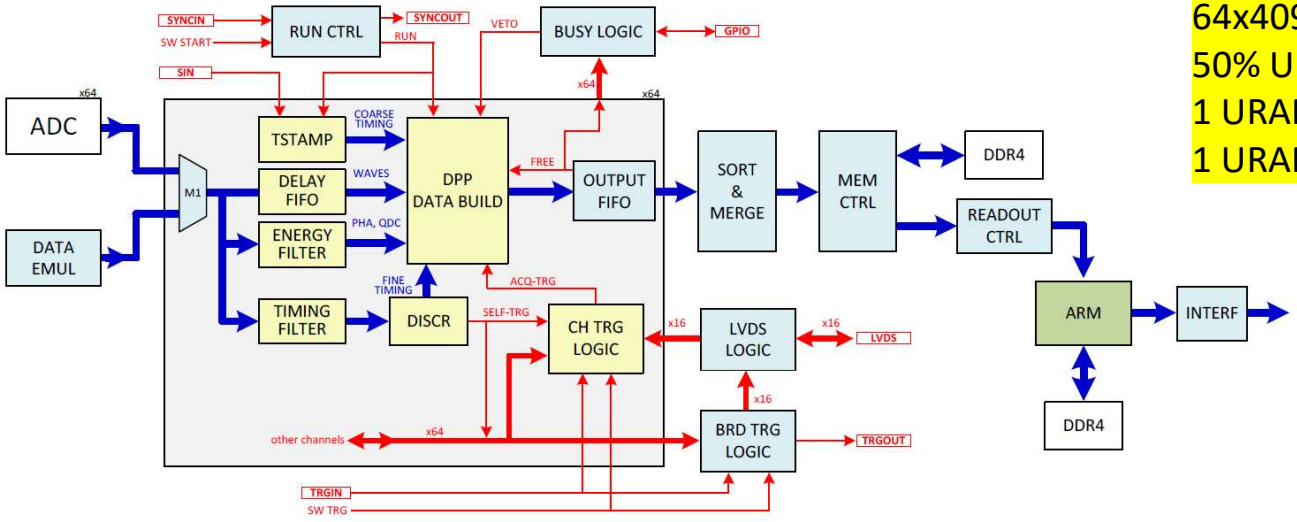
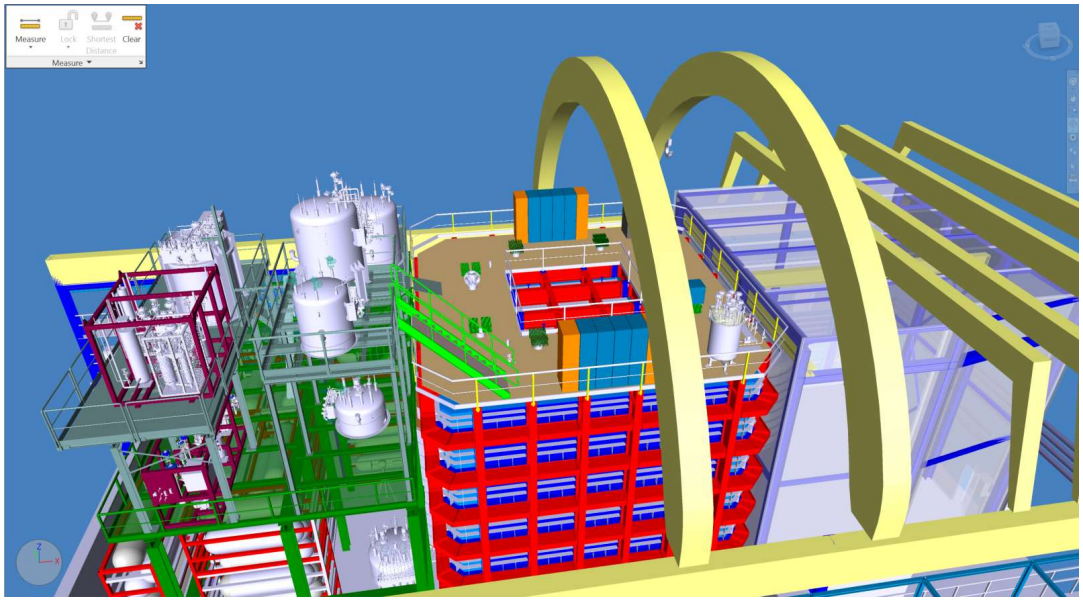
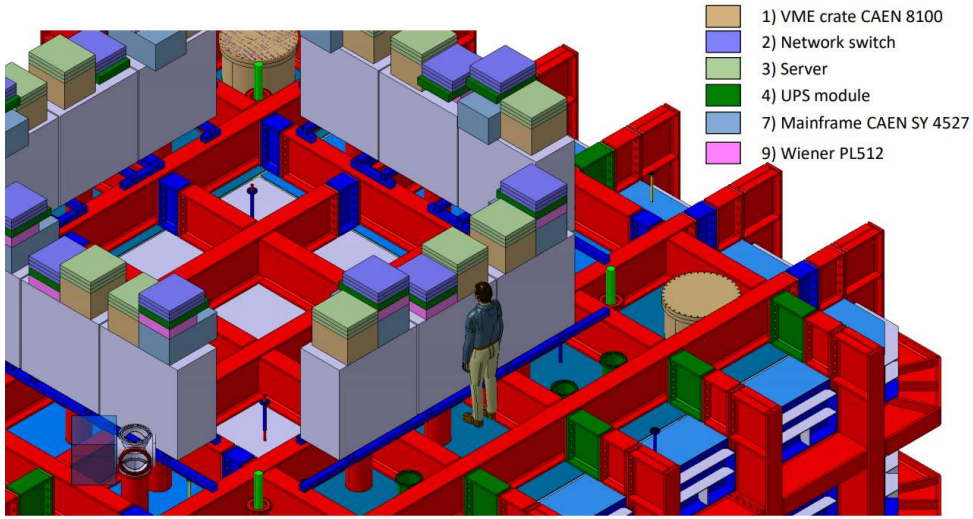


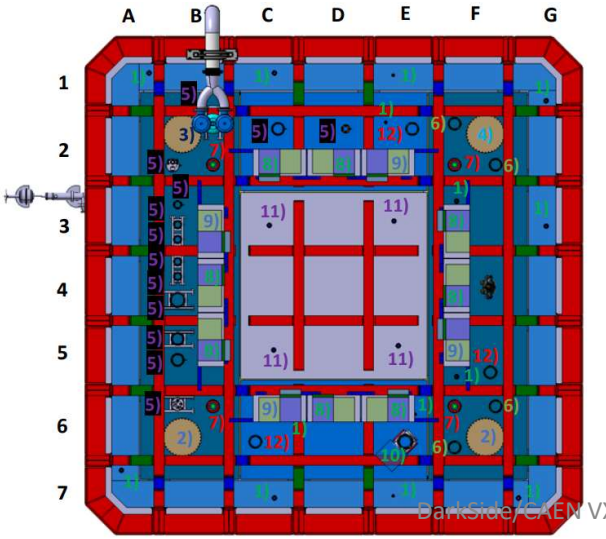
Fig. 3.1: Block Diagram of the DDP firmware

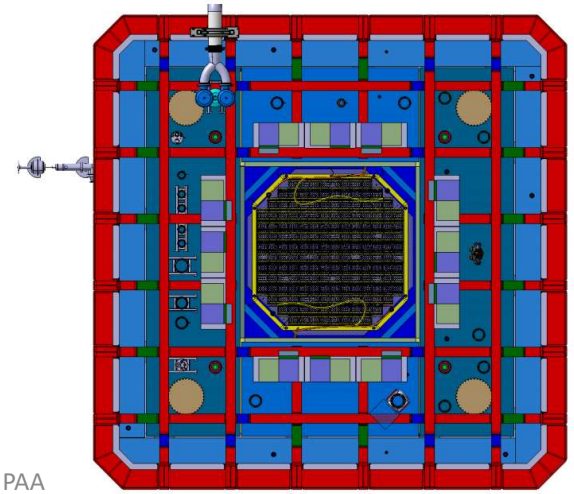




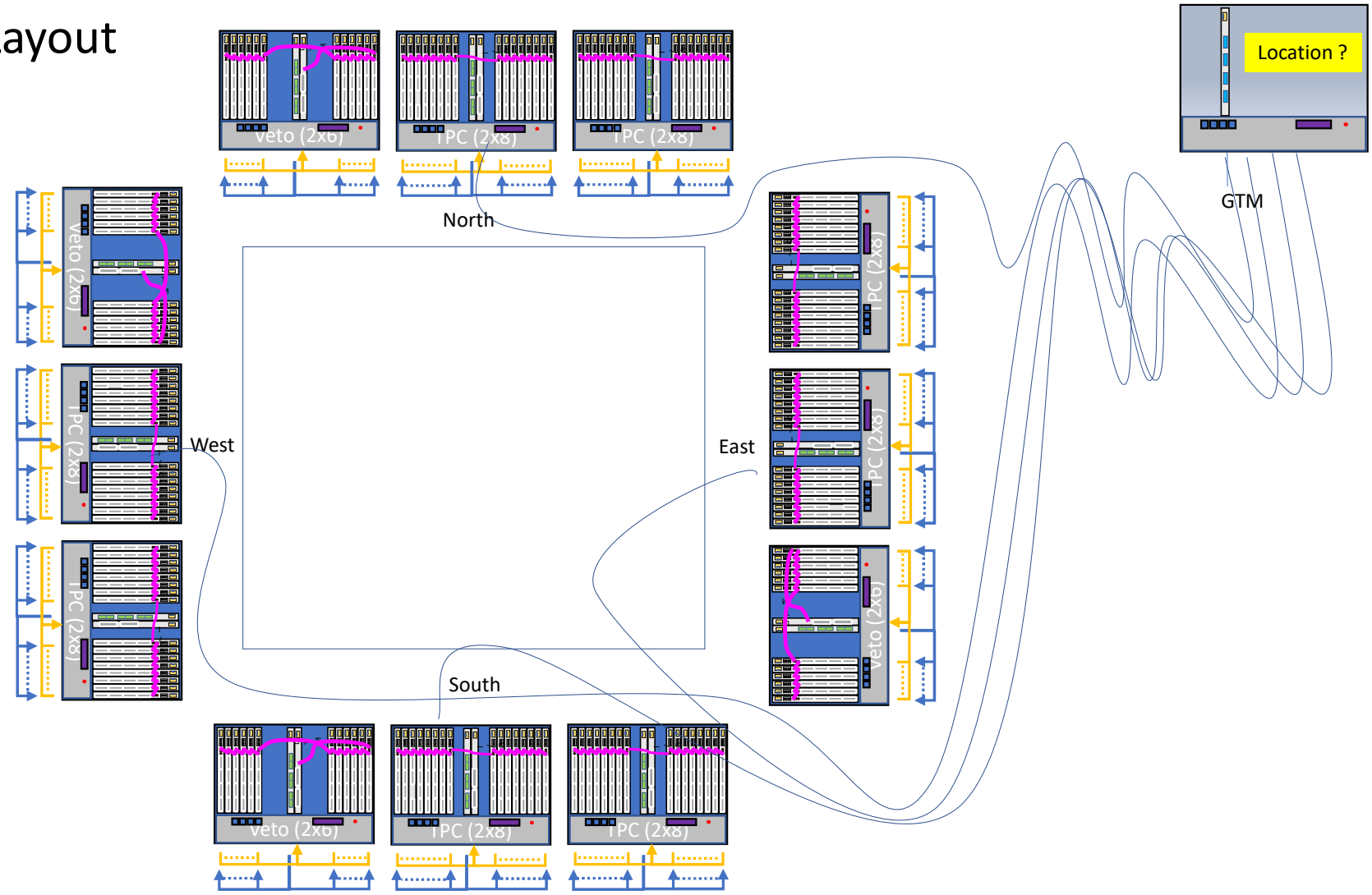
Penetrations layout - 14/07/2020

1)	Penetrations to the insulation	14x
2)	Manholes	2x
3)	AAr heat exchangers support	1x
4)	UAr heat exchangers support	1x
5)	AAr cryogenics	13x
6)	UAr cryogenics	4x
7)	Detector supports	4x
8)	TPC fibers and power supply	8x
9)	Veto fibers and power supply	4x
10)	TPC High Voltage	1x
11)	Calibration	4x
12)	Spare	3x

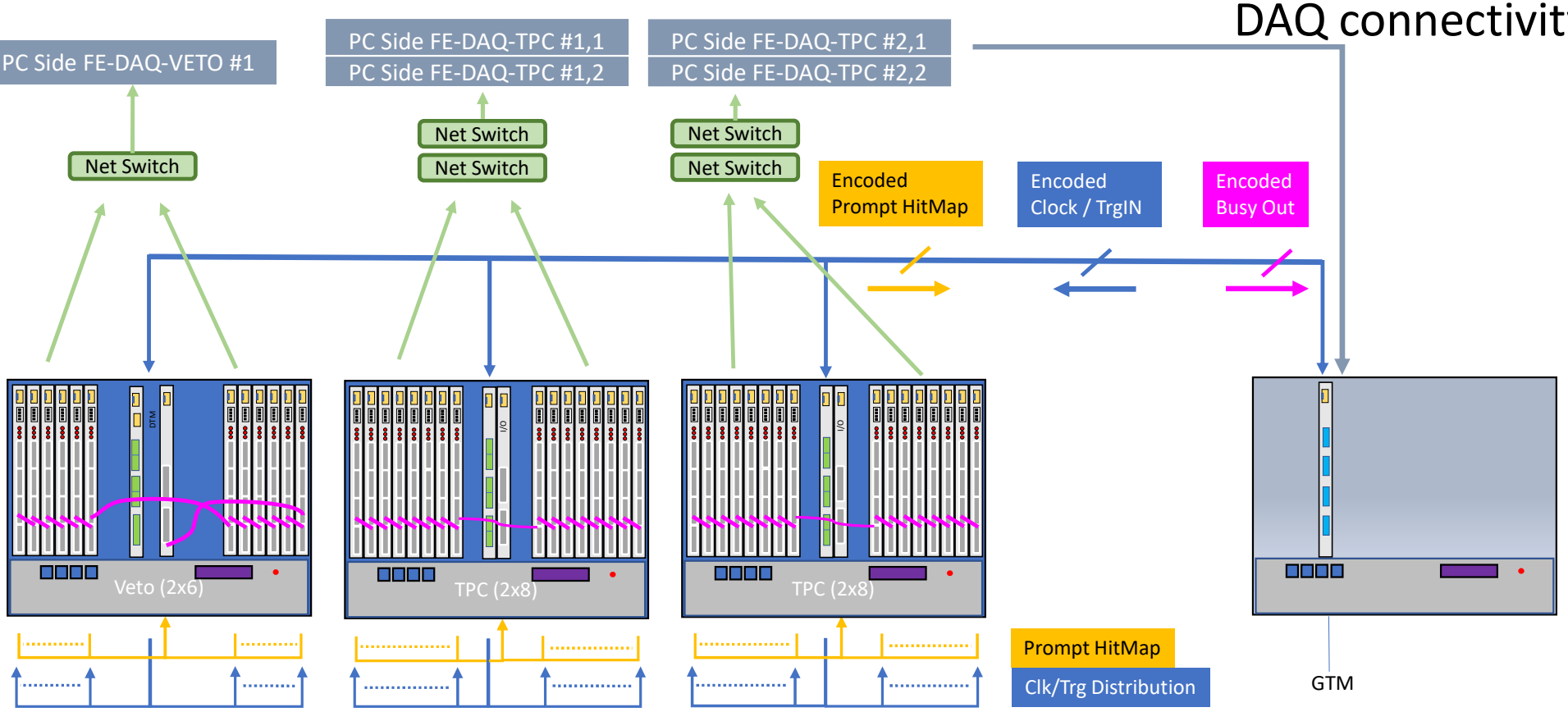




DAQ Physical Layout



DAQ connectivity



MPO: Multi-Fiber Push On
MTP: Multi-Fiber Pull Off
CML: Current Mode Logic

MPO Type A: Straight (extension)
MPO Type B: reverse (Tx/Rx, 1-12 -> 12-1)
MPO Type C: pair flipped

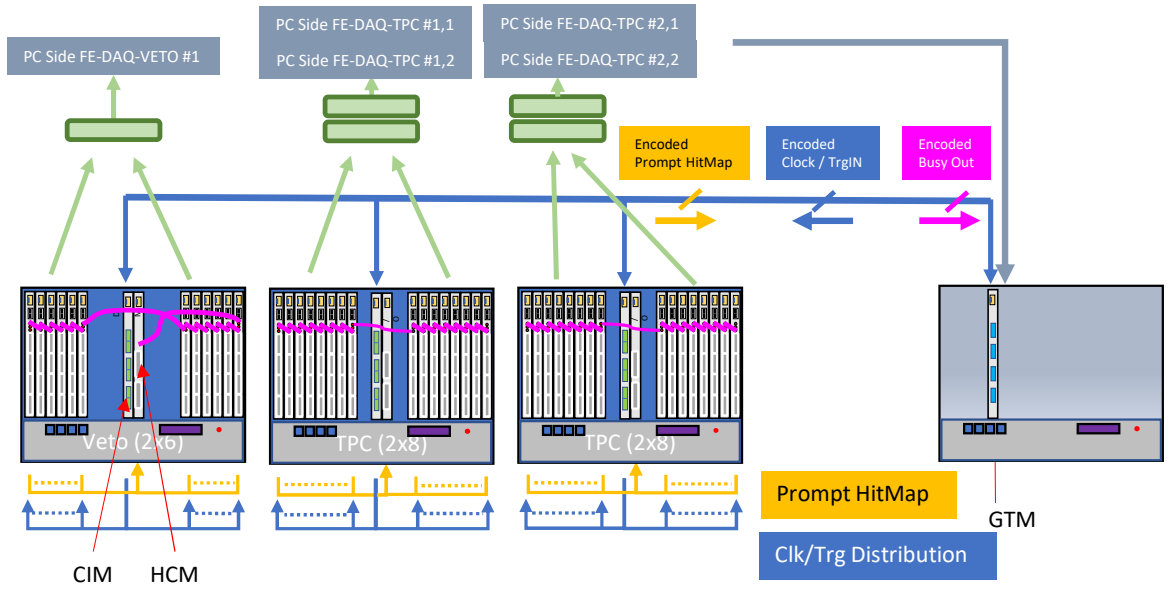
OS: Optical Single Mode (OS2 core 9um)
OM: Optical Multi Mode (OM3 core 63.5/125um)
OM-1,2 : LED, 1Gbps
OM3,4,5: Laser 10,40,100Gbps

(DWDM: Dense Wavelength Division Multiplexing
Up to 192 simultaneously
CDWDM : Coarse DWDM (cheaper))

DAQ Functions

Global Trigger Module Functions (GTM)

- Transmits Reference clock
- Transmits Time Sync Reset (BOR)
- Transmits Fragment Time Stamp (Time Slice marker)
- Receives V2740 Busy Logic Signal
- Receives V2740 aggregate Prompt HitMap
- Receives FEP Busy flag (ETH)
- Transmits Trigger decision



Deals with busy and prompt signals

Can be combined

Communication channel to the global/Central module

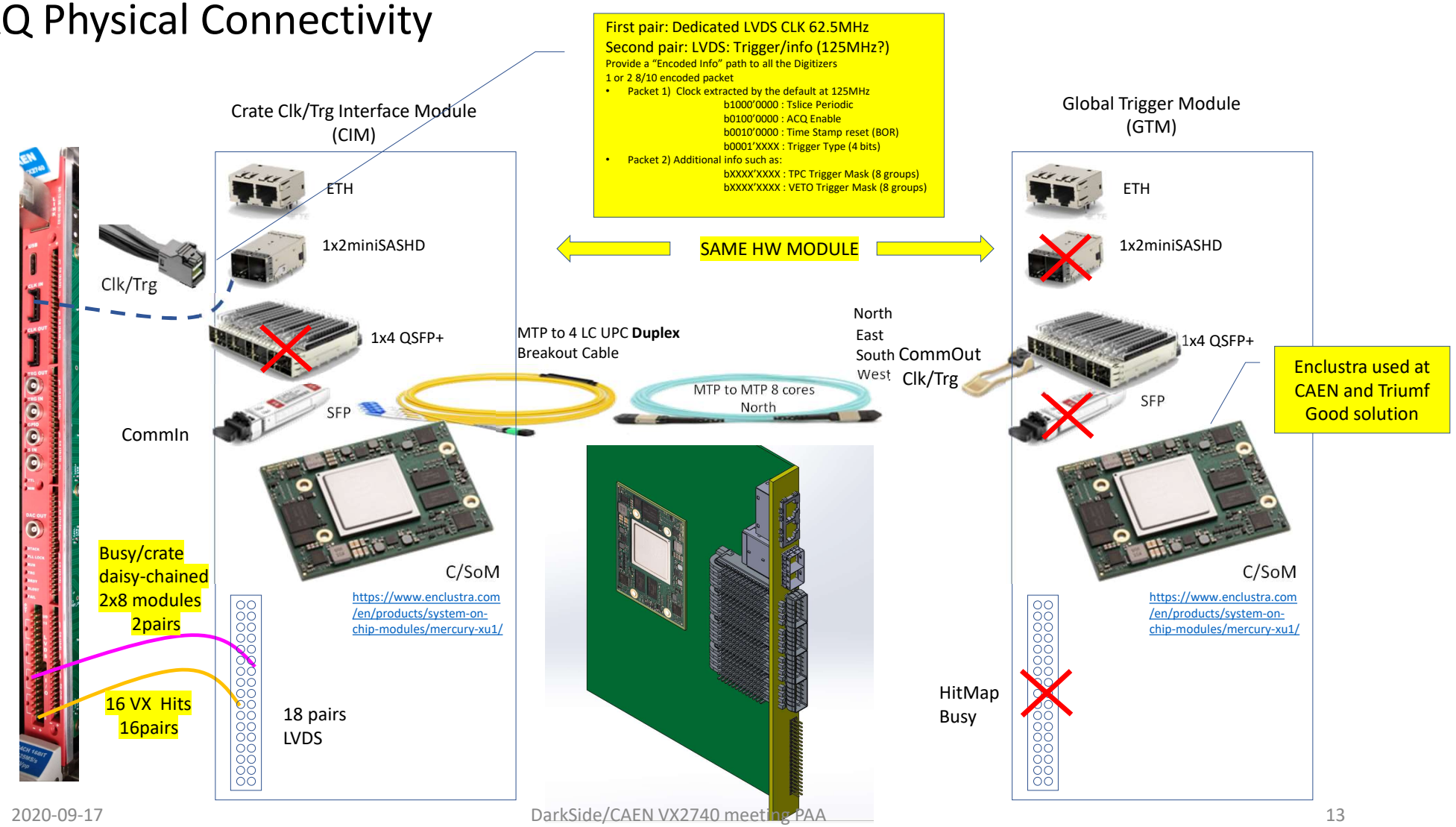
Hit Collector Module (HCM)

- Receives V2740 LVDS Prompt Hitmap
- Receives V2740 LVDS Busy signal
- Transmits aggregate Prompt Hitmap (crate level)
- Transmits Ored LVDS busy signal (crate level)

Crate Interface Module (CIM)

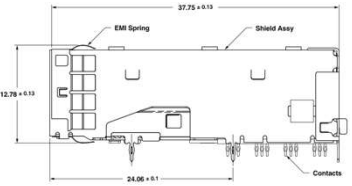
- Receives GTM Encoded Clock/Trigger
- Transmits Clock and Trigger to the V2740s
- Receives HCM LVDS aggregate Prompt Hitmap signals
- Receives HCM LVDS Busy signal
- Transmits encoded Prompt Hitmap
- Transmits encoded Ored Busy signal

DAQ Physical Connectivity



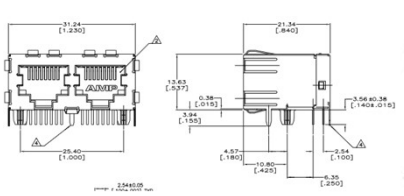
5m, MTP Female to 8 LC UPC, 8 Fiber QSFP Multimode OM3 50/125 Fanout Cable

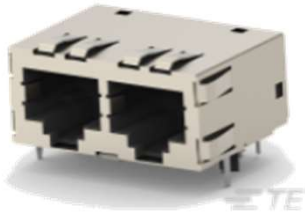
Cisco SFP-H10GB-CU50CM Compatible 10G SFP+ Passive Direct Attach Copper Twinax Cable



MiniSASHD
4HP=20.32 (5.08/HP)

- Mini-SAS HD
- TE Internal #: 2149966-1
- TE Internal Description: MiniSAS HD, 1x2 Rec Assy
- All Mini-SAS HD Cages (12)
- **Number of Ports : *2***
- **Included Lightpipe : *No***
- **Connector System : *Cable-to-Board***
- **Number of Positions : *72***
- **Centerline (Pitch) : *.029 mm [.75 in]***



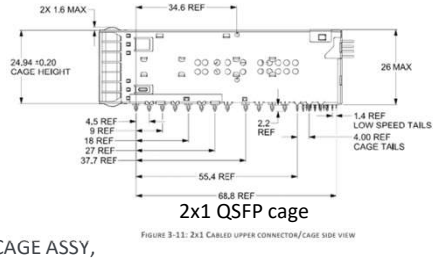


- TE Internal #: 5406566-1
- TE Internal Description: MJ ASSY,2PORT,8POS,SHLD
- Alias #:CA5823-000 PER-5406566-1
- **Modular Jack & Plug Interface Type : *RJ45***
- **Port Configuration : *Multiple Ports***
- **Port Matrix Configuration : *1 x 2***
- **Modular Jacks & Plugs Products : *RJ Type Jacks & Plugs***
- **Connector Contact Density : *Standard***

50/125 MTP TO MTP 8 STRAND MTP (F-F) ARMORED TRUNK CABLE OM3

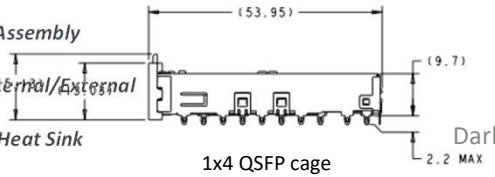
1m (3ft) Cisco QSFP-4SFP10G-CU1M Compatible 40G QSFP+ to 4x10G SFP+ Passive Direct Attach Copper Breakout Cable
#30894

TE ENG_DS_7-1773461-9_MINI_SAS_HD_INTERCONNECT_0918.pdf



2x1 QSFP cage

- TE Internal #: 4-2170808-6
- TE Internal Description: QSFP28, 1X2, CAGE ASSY, SPRING, HS, LP
- **Pluggable I/O Product Type : *Cage Assembly***
- **Port Matrix Configuration : *1 x 2***
- **EMI Containment Feature Type : *Internal/External EMI Springs***
- **Thermal Accessory Type Included : *Heat Sink***
- **Included Lightpipe : *Yes***



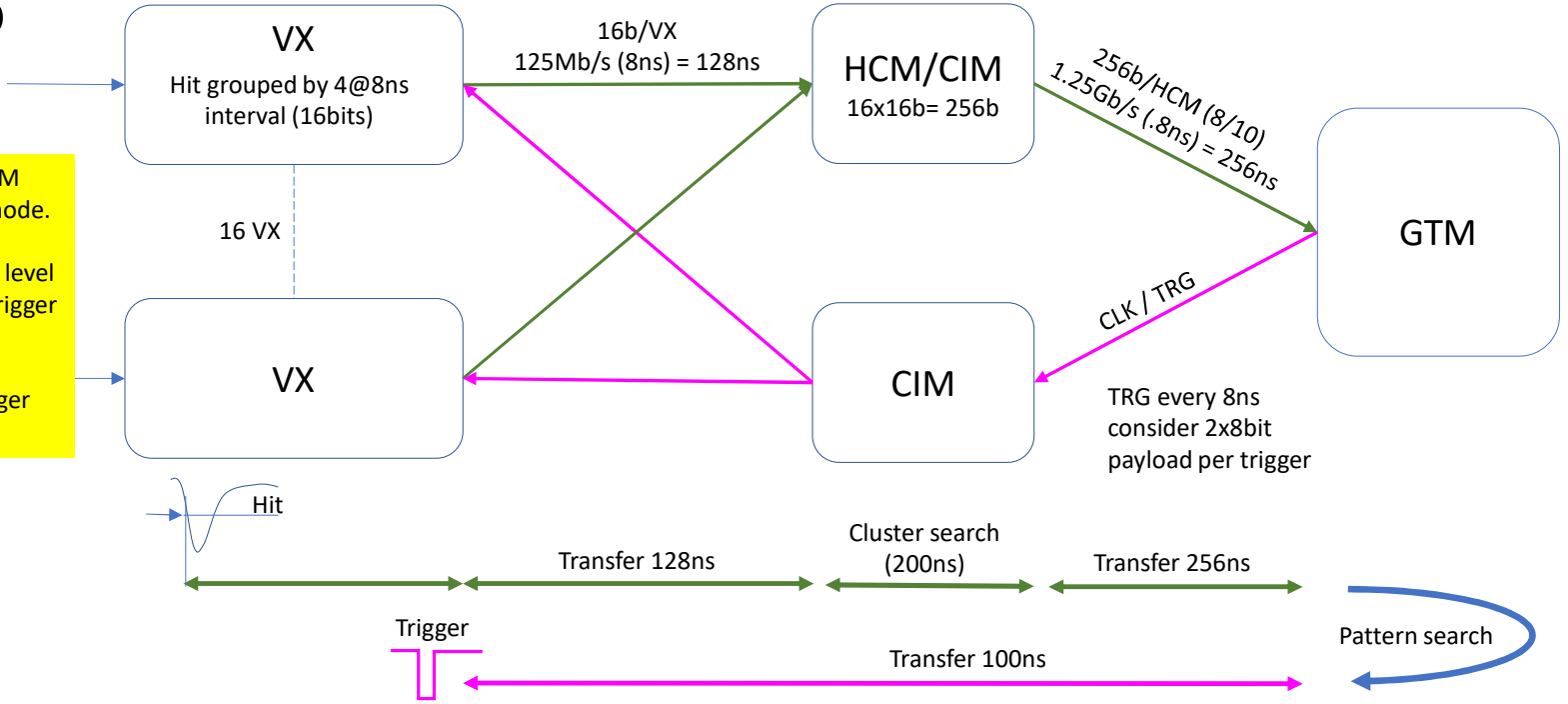
1x4 QSFP cage

Trigger round trip

Study operation of hitmap trigger to GTM and its implementation in Triggerless mode.

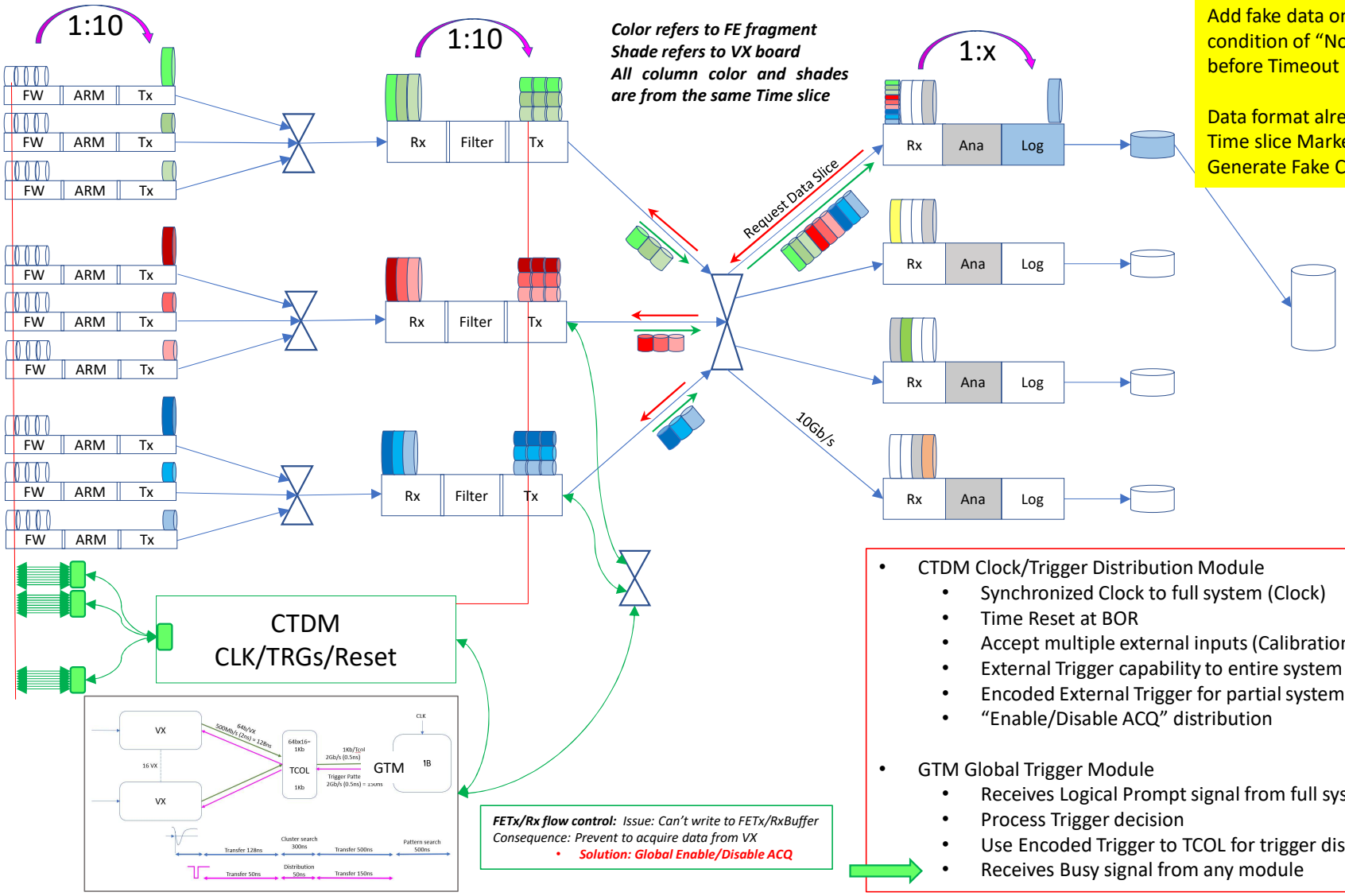
Possible discarding of event at the ARM level if TimeStamp can be correlated to the trigger (allows longer decision time).

Consider validity of partial detector trigger for calibration, test.



- VX provide 1bit per group of four channels based on filtered threshold trigger
- Group of 4 ch to reduce latency between trigger as the transmission link is 125MHz (8ns per bit means 64ch->512ns transmission)
- Cluster search if needed
- Pattern search for trigger generation. Preferred Bottom and Top separate (S1, S2)
- Round trip : ~ 500ns + pattern search

- Provide a "Encoded Info" path to all the Digitizers
  - 1 or 2 8/10 encoded packet
  - Packet 1) Clock extracted by the default at 125MHz
    - b1000'0000 : Tslice Periodic
    - b0100'0000 : ACQ Enable
    - b0010'0000 : Time Stamp reset (BOR)
    - b0001'XXXX : Trigger Type (4 bits)
  - Packet 2) Additional info such as:
    - bXXXX'XXXX : TPC Trigger Mask (8 groups)
    - bXXXX'XXXX : VETO Trigger Mask (8 groups)



Add fake data on all the channels under condition of "No physics event produced" before Timeout

Data format already support that option
Time slice Marker injection from GTM
Generate Fake Ch0 data as described above

FETx/Rx flow control: *Issue: Can't write to FETx/RxBuffer*
Consequence: Prevent to acquire data from VX
- ***Solution: Global Enable/Disable ACQ***

- CTDM Clock/Trigger Distribution Module
  - Synchronized Clock to full system (Clock)
  - Time Reset at BOR
  - Accept multiple external inputs (Calibration, Test pulse, System Trigger)
  - External Trigger capability to entire system (TSSync)
  - Encoded External Trigger for partial system
  - "Enable/Disable ACQ" distribution
- GTM Global Trigger Module
  - Receives Logical Prompt signal from full system
  - Process Trigger decision
  - Use Encoded Trigger to TCOL for trigger distribution
  - Receives Busy signal from any module