Silicon Pixels and Strips

RD_FCC Referees Meeting September 16th, 2020 Remote Connection

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Istituto Nazionale di Fisica Nucleare

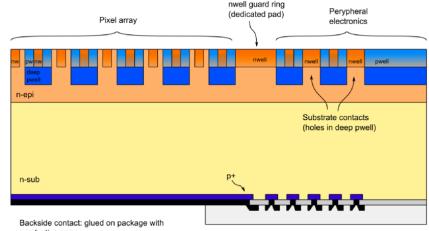
ARCADIA (INFN CSNV Call Project 2019-2021)

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays



Ongoing activity towards a CMOS sensor design and fabrication platform allowing for:

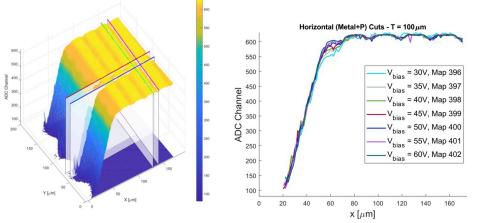
- Active sensor thickness in the range 50 μ m to 500 μ m or more; ¥
- Operation in full depletion with fast charge collection only by drift, small charge collecting electrode for * optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability (O(10 mW/cm2)); ⋇
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure *(SEED), technology demonstration with large area sensors (ARCADIA)
- Technology: 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk *
- Custom patterned backside, patented process developed in collaboration with LFoundry



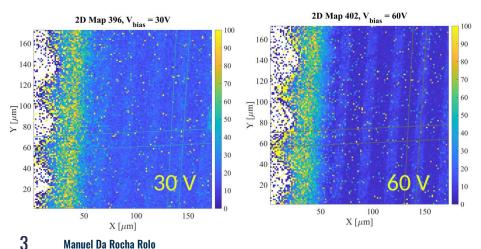
Characterisation with SEED pseudo-matrices



Cuts along the Metal + P and Metal + N lines on the energy map with varying bias voltages show uniform CCE above FD with ~1.7 % loss over metals (100 µm thick)



Standard deviation maps show the expected higher electronic noise when the sensor is not depleted (below 30 V), due to the higher top capacitance.



(RUĐER BOŠKOVIĆ INSTITUTE)* Zagreb, Croatia

- 600 keV to 2 MeV Tandetron 0
- TANDEM 1-6 MeV proton source 0
- LASER TCT laboratory \bigcirc

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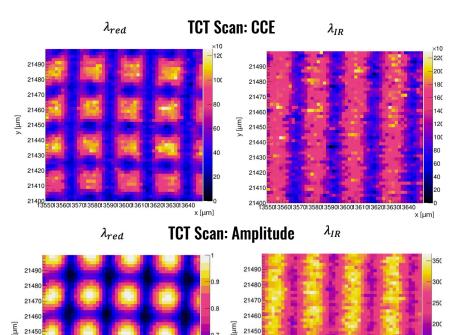
21450

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21420

2141

21400



21450 21440

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21410

x [µm]

21400

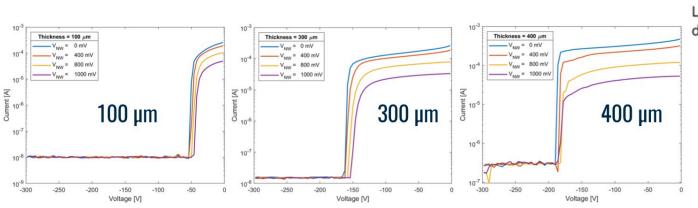
2020-09-16 RD FCC Meeting

x [µm]

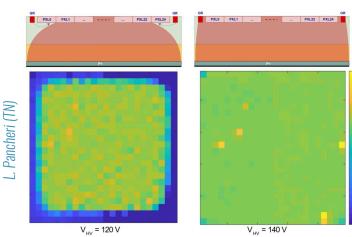
Characterisation with SEED MATISSE

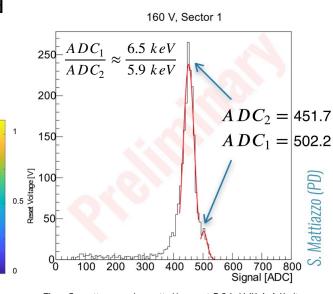
Full depletion studies in 100-300-400 µm prototypes



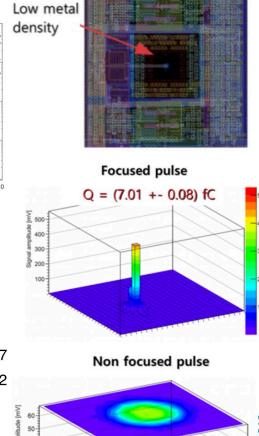


Map of pixel reset voltage (MATISSE 24x24 pixel matrix) as a function of the back-side voltage applied to the sensor. Depletion starts from the back-side.





Preliminary results with ⁵⁵Fe

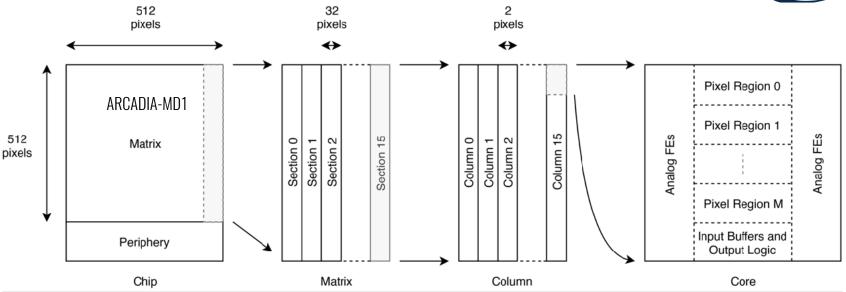


40 30 20 Olave FEE2018

The ⁵⁵Fe emits monochromatic X-rays at 5.9 keV (K_{a}). A K_{e} line at 6.5 keV is also emitted with a relative probability below 5%.

ARCADIA - Demonstrator Chip





- Pixel size 25 μm x 25 μm: process, back-side pattern and geometry validated in silicon (both MATISSE and pseudo-matrices, electrical, laser, radioactive source and microbeam).
- Matrix core 512 x 512, "side-abuttable" to accomodate a 1024 x 512 silicon active area (2.56 x 1.28 cm²).
 Matrix and EoC architecture, data links and payload ID: scalable to 2048 x 2048*
- Triggerless binary data readout, event rate up to 10-100 MHz/cm²
- ★ First <u>engineering run with ARCADIA-MD1 by 09/2020</u>, second full CMOS maskset during spring 2021, funding available for 3 engineering runs (secured over <u>0.4M€ extra funding</u> from synergy with EU Projects)



Rimosso materiale "Internal Use Only", contattare darochar@to.infn.it

ATLASpix3 Large Silicon Systems



* R&D for the large are part of the detector:

◆ All Si-tracker or Si-Wrapper for IDEA and TPC based tracking systems: 50-100 m2

* Proposal submitted to CEPC including interests from Italian groups:

 China: Harbin, IHEP, NWPU, Shandong, SJTU, Tsingua, UTSTC: Germany: KIT; Italy: Milano, Pisa, Torino; UK: Bristol, Daresbury, Edinburgh, Lancaster, Liverpool, RAL, Sheffield, Warwick

* Develop a full CMOS pixel solution:

- Full CMOS technology costs and power consumptions are becoming nearer to the strips
- ◆ If trend continues, it may effectively replace them with a more performant detector

| CMS Upgrade | Double Strips | Macropixels+Strips | Hybrid Pixels | DMAPS@FCCee |
|----------------------|-------------------------|-------------------------|--------------------------|-----------------------------|
| Area | 192 m ² | 25 m ² | 4.9 m ² | 100-200 m ² |
| Power density | 27 mW/cm ² | 89 mW/cm ² | 700 mW/cm ² | <150 mW/cm ² |
| Module cost (TDR) | 26990 kCHF | 20780 kCHF | 11691 kCHF | |
| | 140 kCHF/m ² | 830 kCHF/m ² | 2400 kCHF/m ² | 400-500 kCHF/m ² |

ATLASpix3 R&D plans

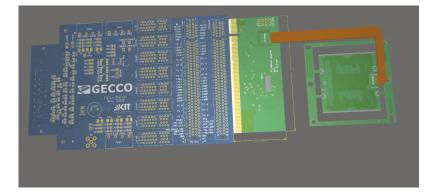


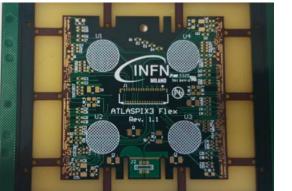
* Initial prototyping using ATLASPIX3

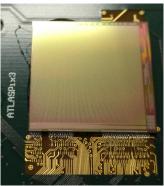
- ✤ Full size 2x2 cm chip from ATLAS developments
- Demonstrating module and mini-stave assembly
- \bullet Two wafers (one thinned to 150 μ m) dedicated to the initial effort:
 - practicing the DAQ system (design by KIT, production done by Chinese groups, now begin distributed)
 - test module assembly (Milano): flex circuits now being populated
 - integration of modules in the test system (UK)

* Further generations of the sensors are in development:

- ♦ FCEPCPix1 in AMS,
- possible porting to other foundries







ATLASpix3 Financial requests for 2021



***** Perform a further iteration in module assembly:

- current flex hybrid implementation followed the KISS (keep it simple and safe) principle;
- ★ a second generation would implement features for use in system tests and a more realistic environment:
 - reduce number of layers (possible by dropping options implemented in the 2020 version)
 - design for operation within a serial powering chain
- * Additional sensors will be needed for building mini-staves
 - same masks as ATLASPIX3, so non-recurring costs already paid in ATLASPIX3 original submission. Contributions from various FA, cost should be 2k€/wafer + taxes.

***** Funding requests:

| Categoria | Sez. | Capitolo | | [k€] |
|-----------|------|----------|---|------|
| 3 | MI | Consumi | Flex hybrid | 5 |
| 3 | MI | Consumi | Acquisto wafer ATLASPIX3 (2 wafer x 2.5 k€) | 5 |