



WP4 activities



UNIVERSITÀ DEGLI STUDI DI MILANO



Istituto Nazionale di Fisica Nucleare

Nicola Neri
on behalf of WP4

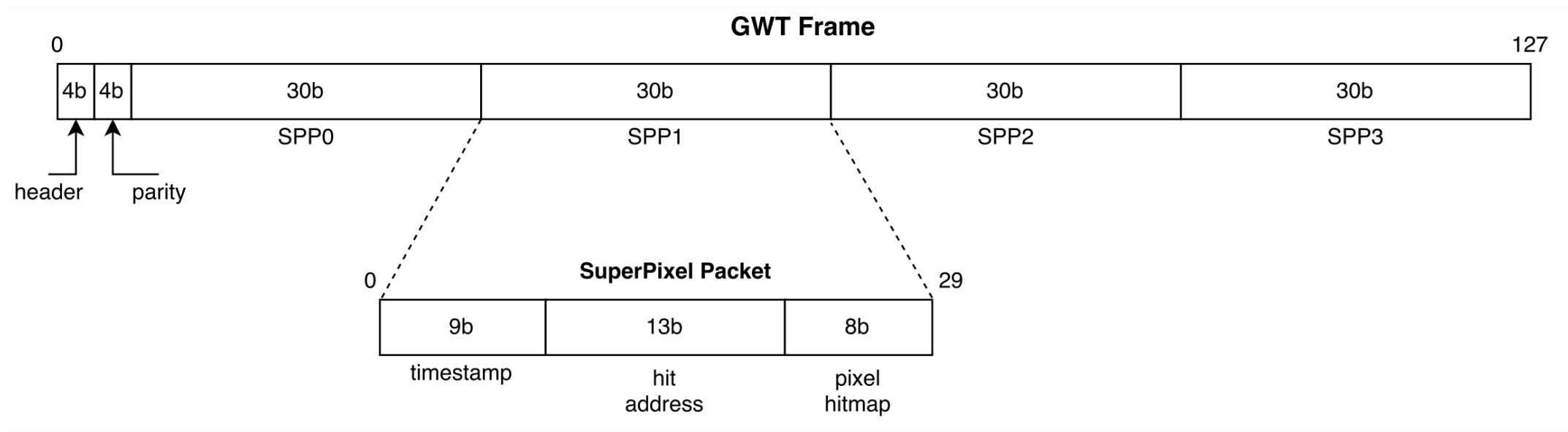
14 Settembre 2020

Activities

- ▶ Tracking on FPGA:
 - clustering, stub maker on FPGA 1
 - tracking on FPGA 2
- ▶ Simulations
 - optimisation of the architecture
 - performance of 4D tracking on FPGA
 - Integration with VELO
 - stub based tracking optimal geometry
 - costs

VELO data format

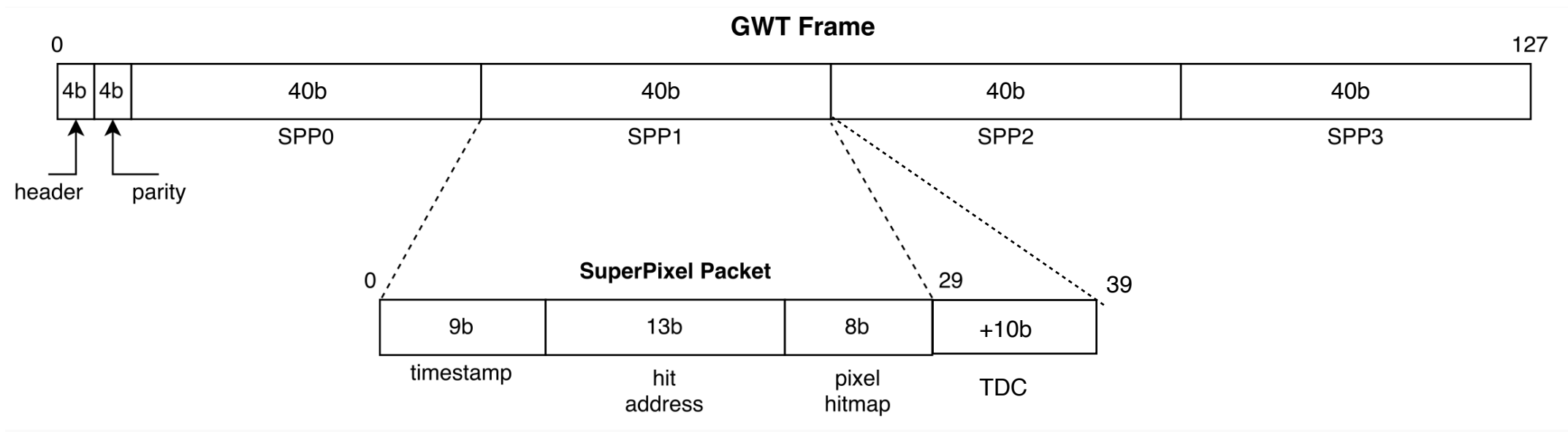
- ▶ Readout type: continuous, triggerless, binary
- ▶ Timing resolution: 25 ns
- ▶ Data format: 30bit. 9-bit timestamp defines maximum latency



- ▶ Pixel data organised in SuperPixels, groups of 2x4 pixels (30% reduction in data size)
- ▶ Data sent out of time —> Timestamp stored in SuperPixel data packer

Timespot data format

- ▶ Readout type: continuous, triggerless, binary
- ▶ Timing resolution: 30 ps
- ▶ Data format: ~40bit. 9-bit timestamp defines maximum latency + 10-bit TDC, defines hit time wrt reference time



- ▶ 10 bit to divide 1 ns, time of pp collision, into 1 ps intervals and determine the time of the hit with respect to the time of collision
- ▶ Assumption: ASIC has a 10 bit TDC and a reference clock for collisions is provided by LHC (to be verified)

Estimated costs for VELO tracking

- ▶ Working hypotheses:
 - clustering and stub construction can be done on DAQ FPGA
 - 100.000 engines are needed for track reconstruction with 1.000 engines per FPGA
 - cost of each FPGA 10.000 Euro
 - 30% of the cost is for switch ports, infrastructures and spares
- ▶ Total cost: about 1.300.000 Euro

By Stephen M. (Steve) Trimberger, Fellow IEEE

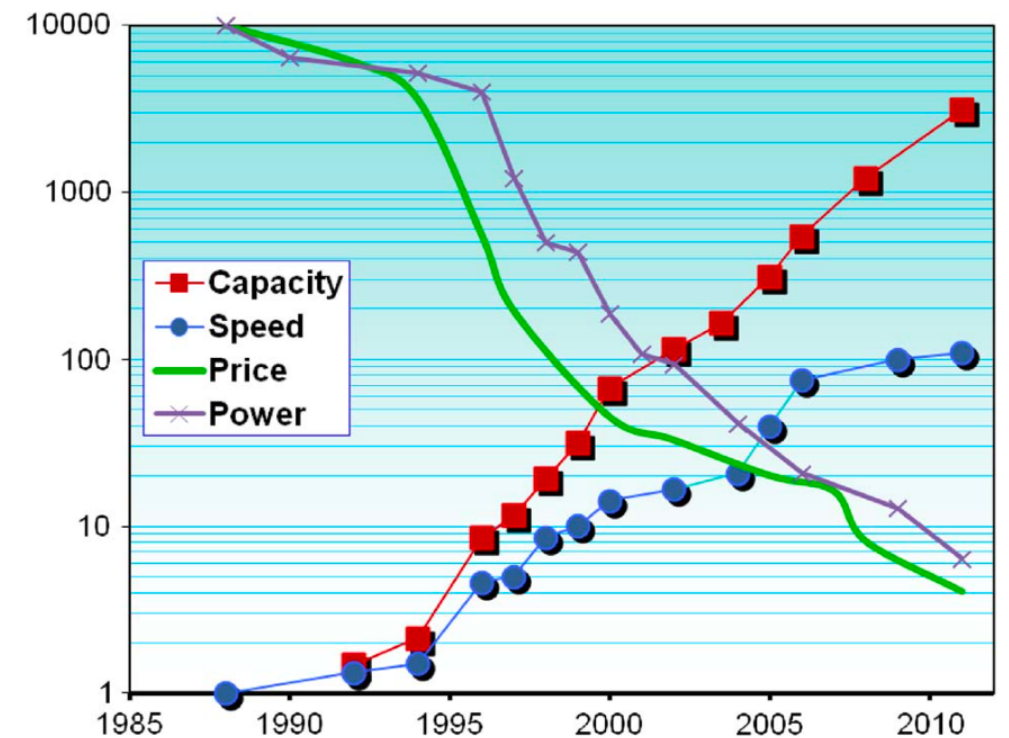
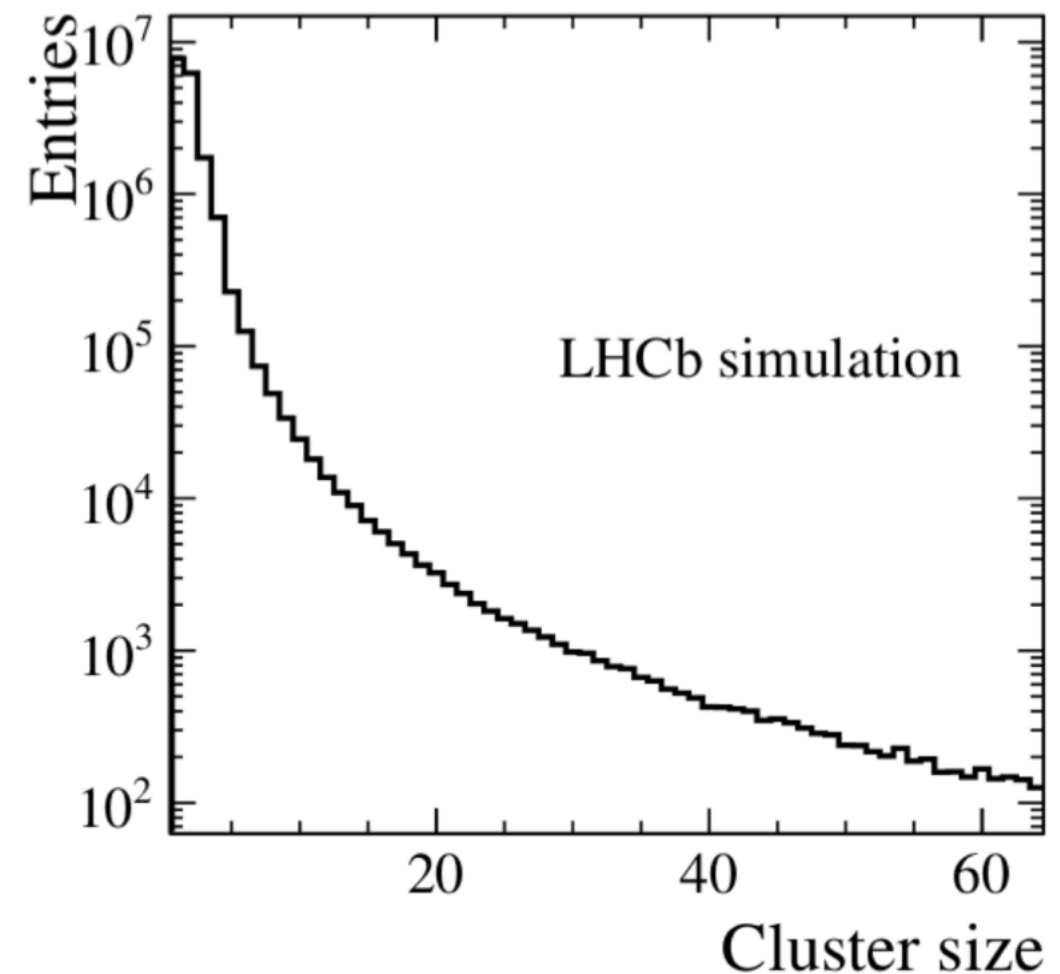


Fig. 1. Xilinx FPGA attributes relative to 1988. Capacity is logic cell count. Speed is same-function performance in programmable fabric. Price is per logic cell. Power is per logic cell. Price and power are scaled up by 10 000×. Data: Xilinx published data.

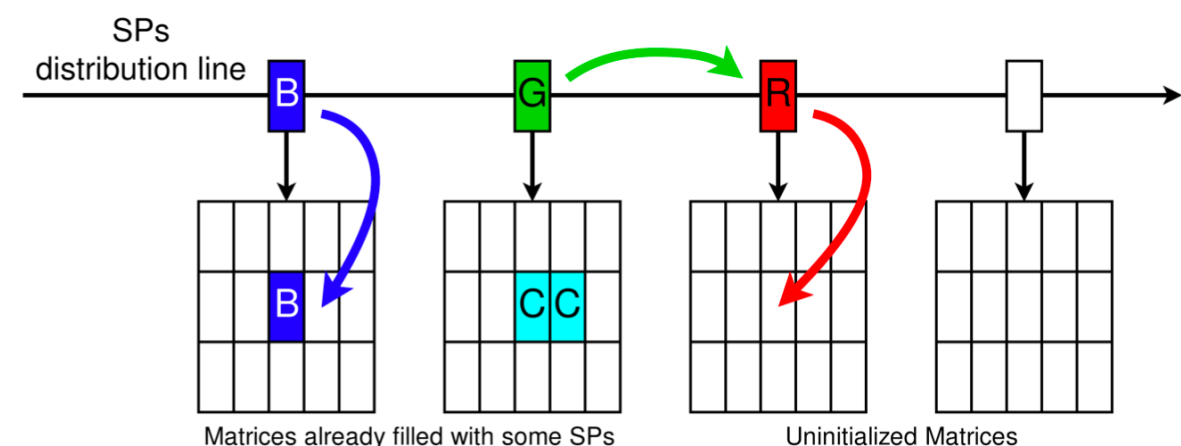
Cost expected to reduce of 1 order of magnitude in 10 years

Clustering

- ▶ Time info not needed for clustering (Serena, Angelo)
- ▶ Solution for 2D VELO clustering in FPGA has been already proposed
- ▶ 2/3 of clusters contained in one SP. Very fast to reconstruct with pre-calculated position stored in LUT
- ▶ Clusters with neighbour SP require a parallel cluster finder



F. Lazzari et al., *J.Phys.Conf.Ser.* 1525 (2020) 1, 012044



Stub maker

- ▶ Fundamental modules implemented and tested on FPGA (Marco)
- ▶ Grid of stub makers and test with simulated data in progress

