TimeSPOT WP4:
Stato delle attività a Milano

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Current status

- **Switch + Engines** implementation completed

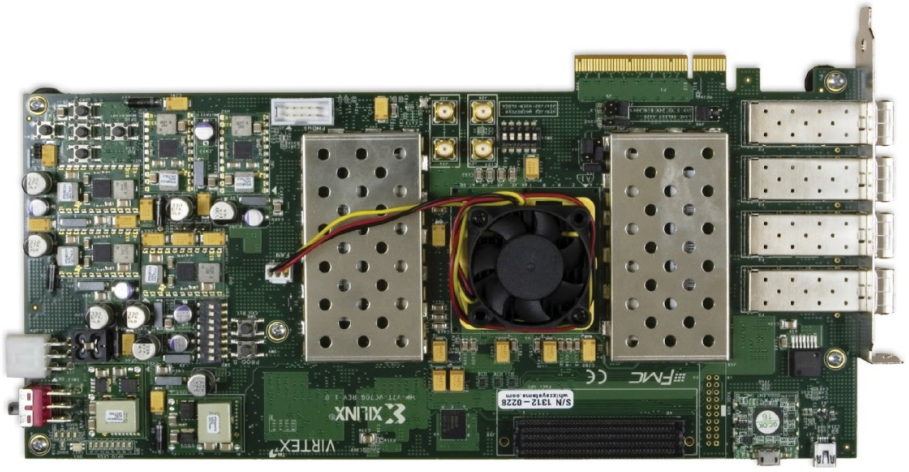
- **Stub Constructor** implementation ongoing:
  - Main components are already implemented and tested in hardware

- **Generation** of input data from simulation completed (based on an older software implementation)
  - Finalization of the algorithm porting to Python3 implementation ongoing

- **Communication** between VC709 and gFEX board via optical links to be checked/fixed

VC709 activity

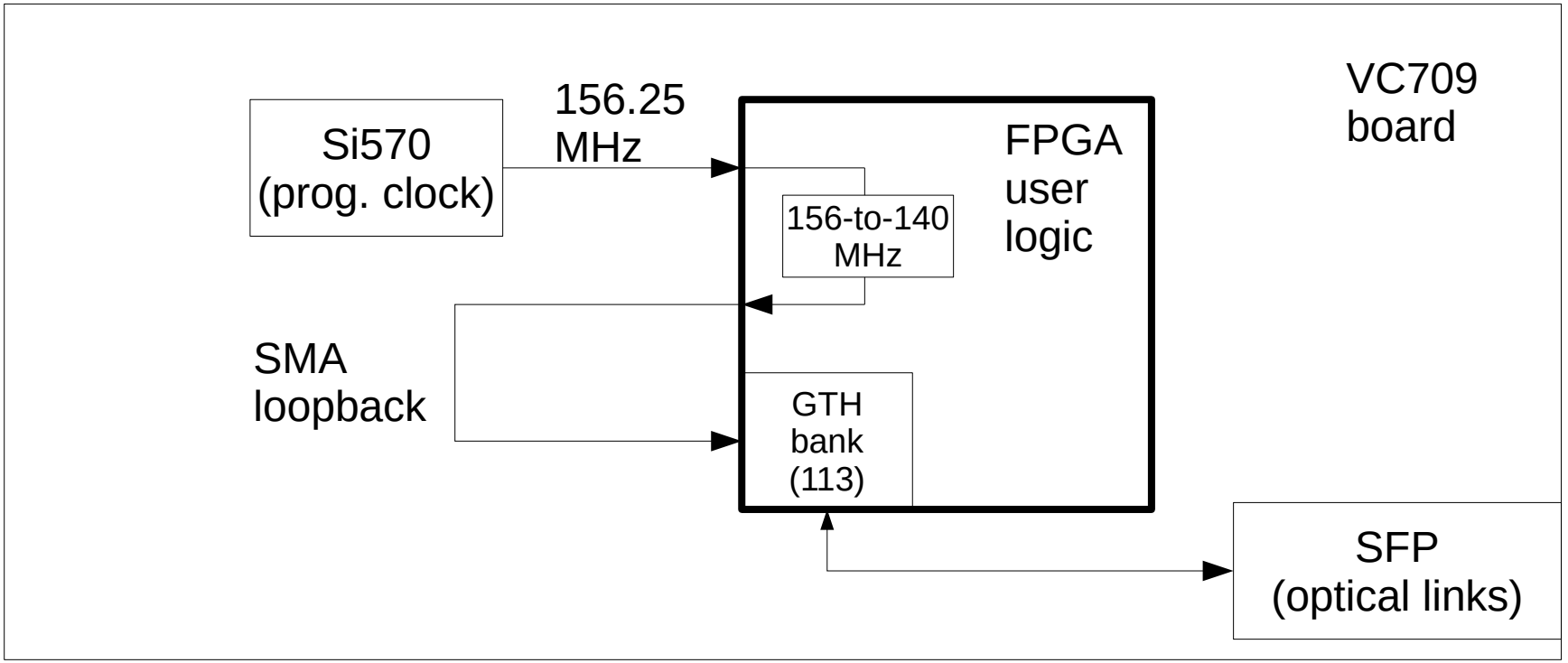
- VC709 firmware **tasks**:
  - Communication with PC via PCIe (Wupper) : **done**
  - Communication with gFEX : **ongoing**
  - Implementation of Stub Constructor : **ongoing**



- Activity resumed starting from M.Luchi's work (former master student)
  - Main focus of the activity was based on the **communication tasks**
  - Main information has been recollected and merged in a **unique firmware** including:
    - GTH, MIG (RAM), PCIe (Wupper)
    - slow control (I2C)
    - Stub Maker and xy-to-rphi converter tests

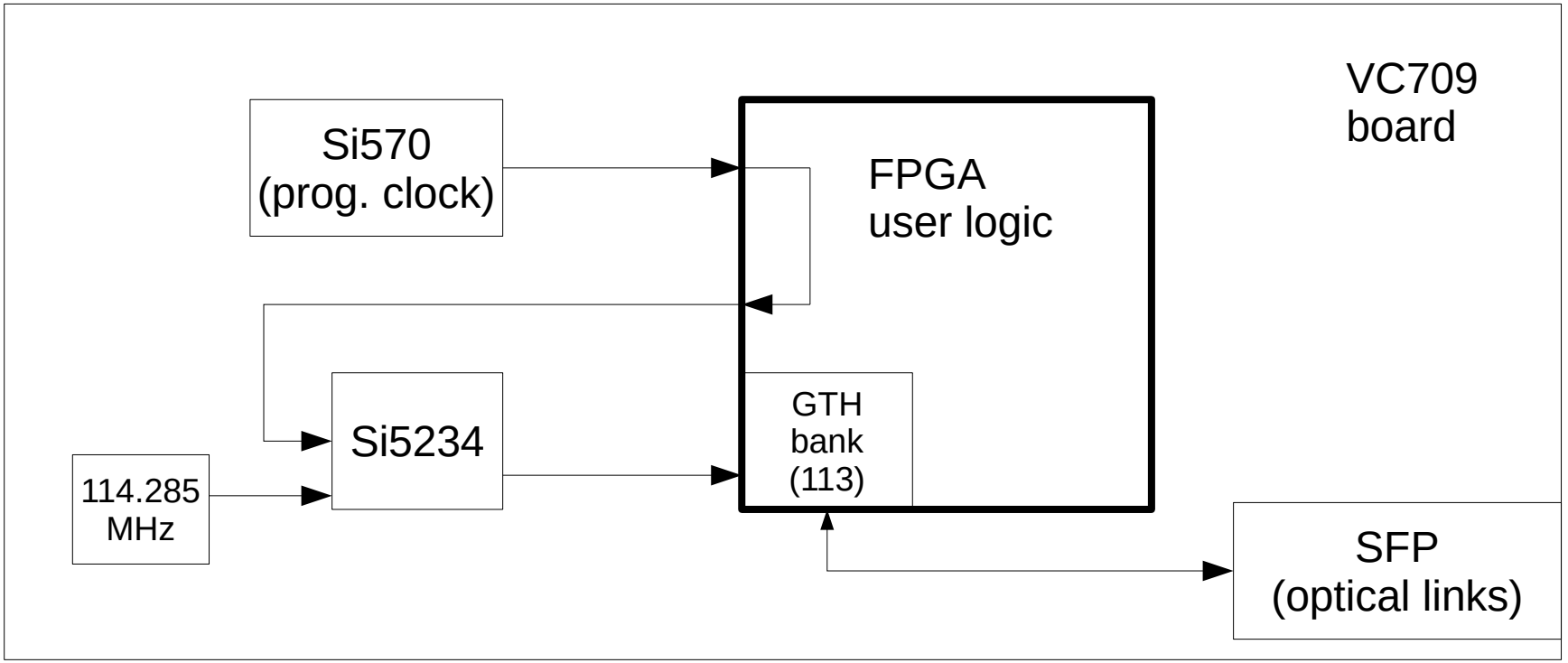
VC709 to gFEX communication

- VC709 optical links working in loopback (VC709 TX to VC709 RX) configuration.
- In the past an attempt of communication to/from the gFEX was made with no results.
- The main cause of the failure could be the different clock sources of the two boards
  - In practice the two boards TX and RX could not synchronize
- The old clocking scheme of the VC709 is reported below:



VC709 to gFEX communication

- The VC709 has one programmable clock generator (Si570) and one Si5324 jitter cleaner (with integrated crystal oscillator)
- Two approaches are under investigation at the moment
  - 1) clock generation on Si570 + Jitter cleaning on Si5324
  - 2) clock generation directly on Si5324 (using the 114.285 MHz crystal oscillator)
- At the moment I am working on verifying the correctness of the generated clocks in the two schemes, and communication tests willl be performed after



Near future plans

- **Optical links communication tests between VC709 and gFEX**
  - The communication via optical links is really necessary since the gFEX has no high speed communication to/from PC

- **Implementation of the full Stub Constructor on the VC709 board**
  - The major components have already been tested (i.e. Stub Maker, xy-to-rphi coordinate conversion modules, Switch for hits delivery)

- **Reproduce Switch+Engines results on gFEX**
  - Using data generated from improved simulation and with higher statistics
  - Using data from PC (via VC709); in the past a set of input data was stored in a BRAM

- **Connect Stub Constructor (VC709) to Switch and Engines (VC709) for a complete test**