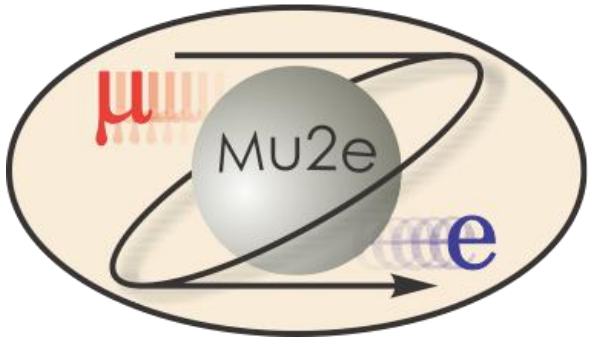
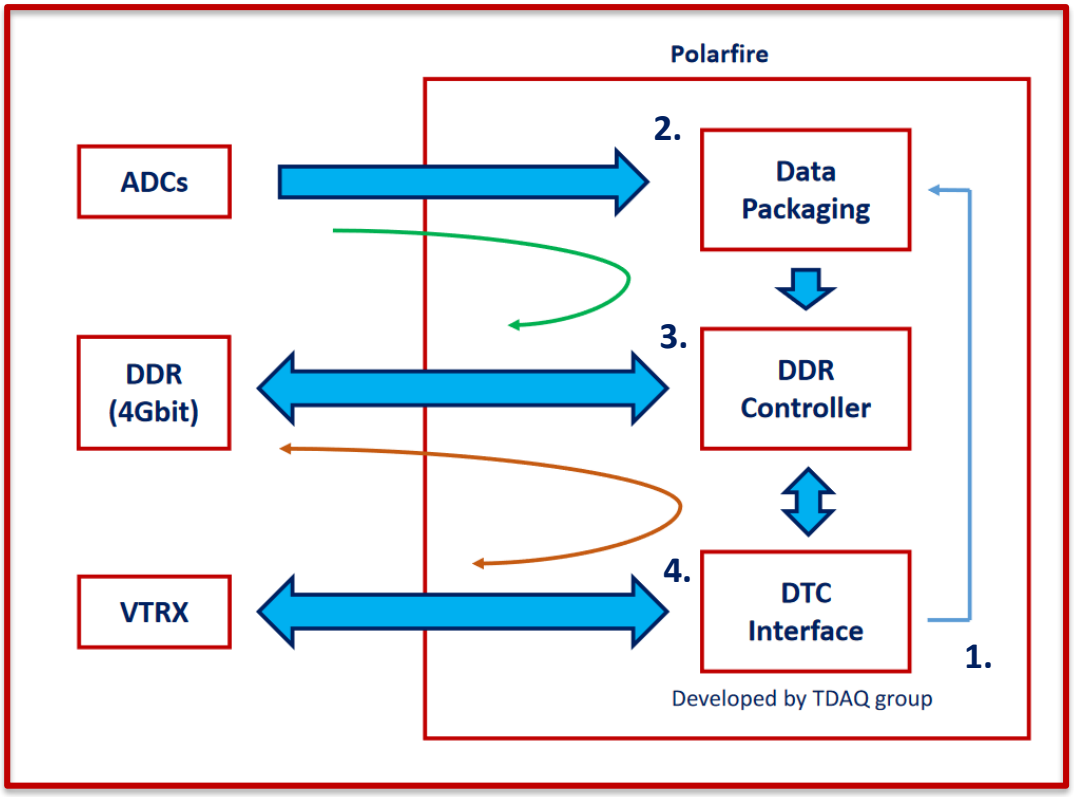


Status of DiRAC Firmware

Mu2e Italian Meeting
September 03, 2020

S. Di Falco, A. Gioiosa, L. Morescalchi, E. Pedreschi, F. Spinella

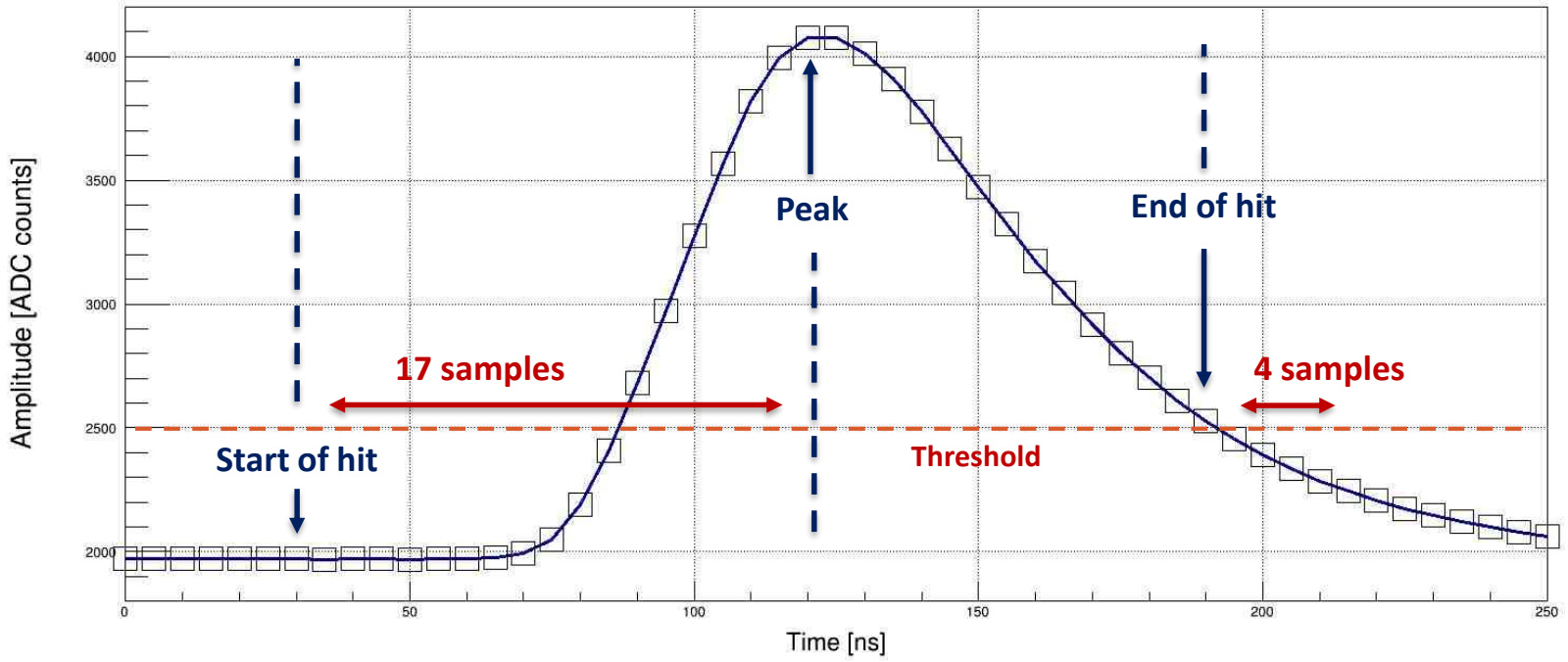
Main Firmware Block Diagram



1. TDAQ sends Heartbeat packet that contains EVENT TAG and EVENT WINDOWS
2. DiRAC builds the calo hit applying a zero suppression and pre-processing data
3. Data are stored in the DDR
4. TDAQ sends Data Request for a specific EVENT TAG, and DiRAC retrieve requested Data Packet from DDR and sends it out to DTC

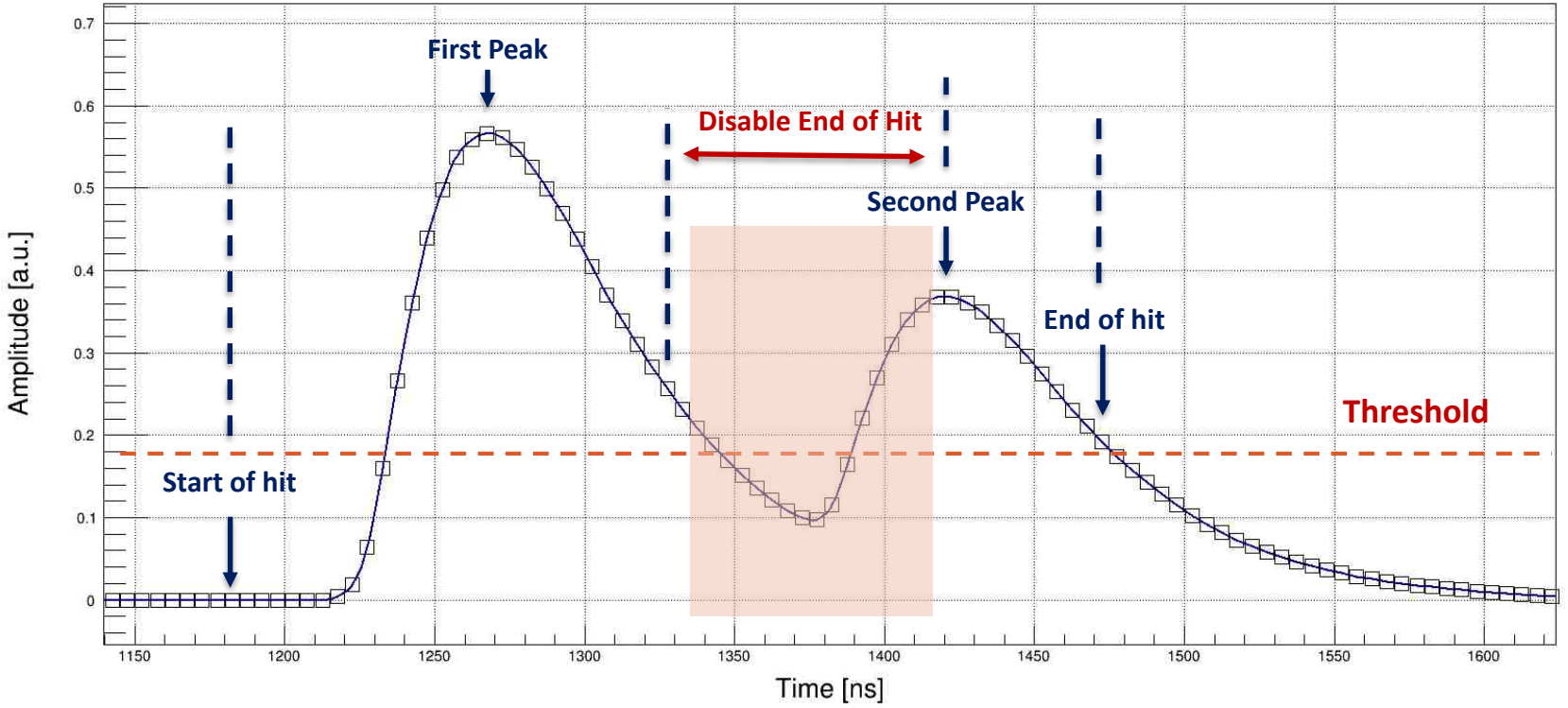
The slow control block is not shown..

Zero Suppression: Hit Definition



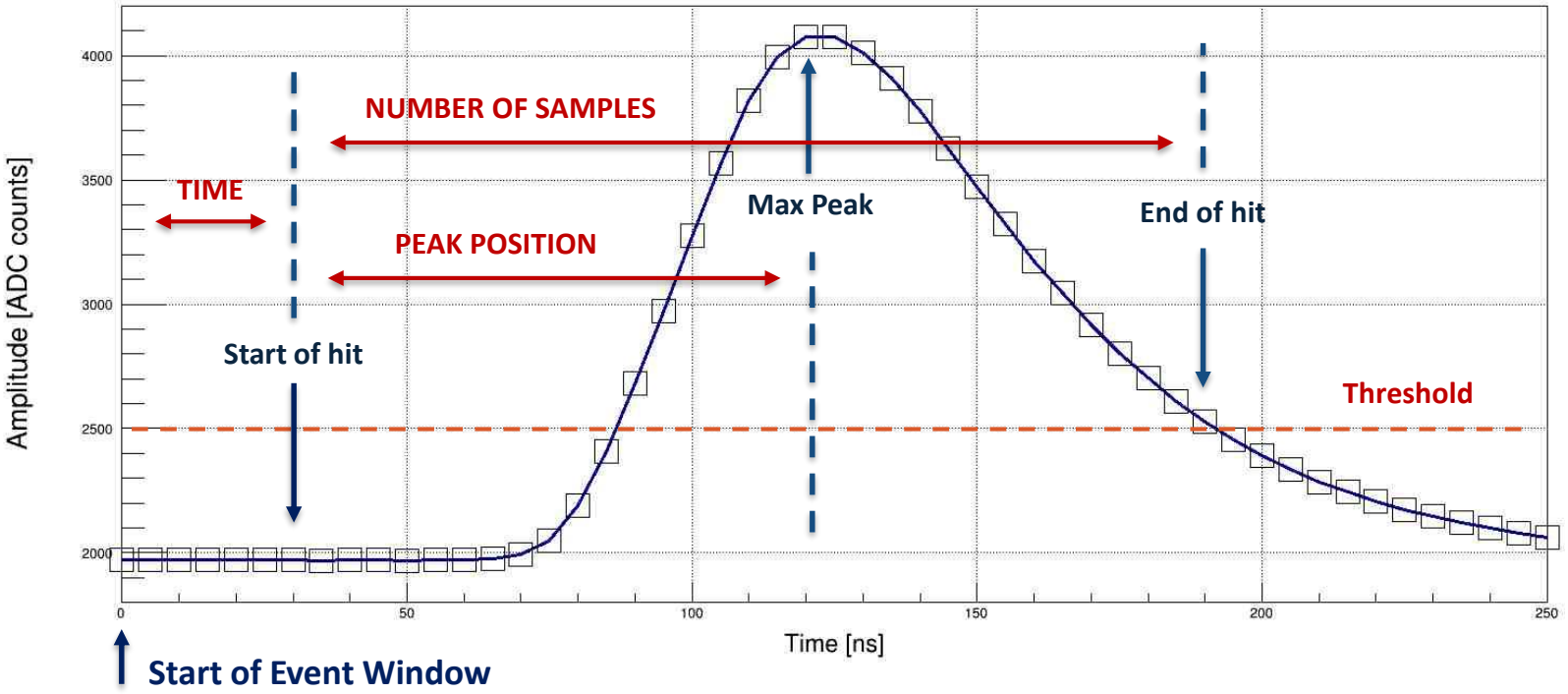
- An hit triggers when is found a peak over threshold and is composed of:
  - 17 samples before the peak, to be sure to record the rising edge and the baseline level
  - A variable number of samples until the waveform goes under threshold for 4 consecutive samples

How to Handle the Pileup?



- After the first peak over threshold, if other ones arrive within 17 samples from the moment the waveform goes under threshold, the two hits are merged
  - This allows to save more bandwidth than would be possible separating the hits

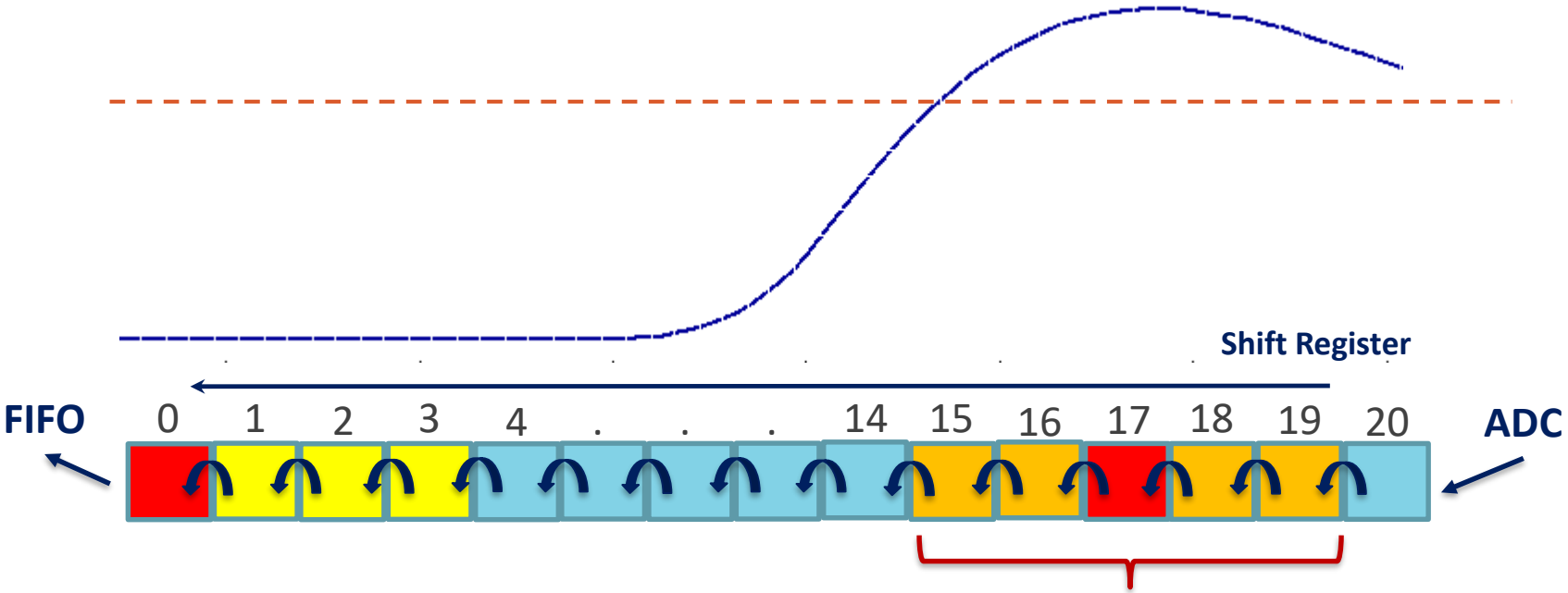
Zero Suppression: Pre-Proc



- Other than the value of the samples, we have to store in the hit also some additional info:
  - **HIT TIME**: the number of clock cycles from the start of the Event Window to the first sample of the hit
  - **NUMBER OF SAMPLES**: the number of clock cycle from the start to the end of an hit
  - **PEAK POSITION**: the position inside the hit of the absolute maximum of the waveform
  - **ERROR FLAG**: a flag that contains info on the quality of the hit.. It has to be specified yet

Zero Suppression: Implementation

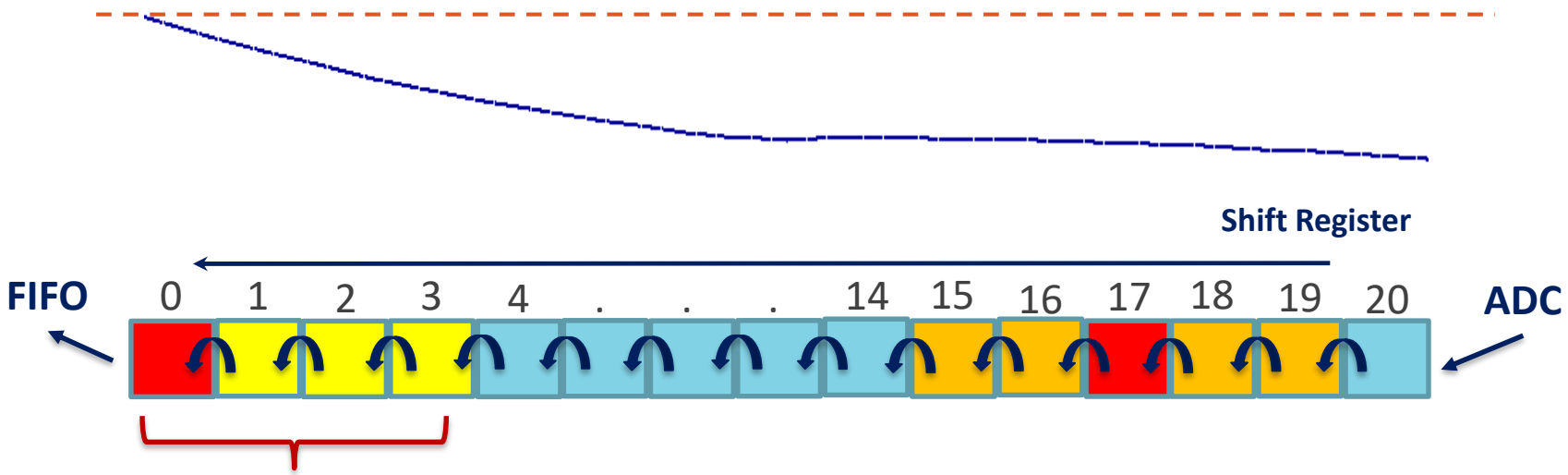
- The sampled waveforms pass through a shifter register, which can be seen as a picture of the samples that updates at every clock cycle
- A sample enters in position 20 and when in position 0 it can be either stored in a FIFO or lost



- If a maximum is detected in position 17, the hit starts and the samples are written in the FIFO from 0 until the hit ends

```
89    peak_flag <= '1' when
90    (data_pipe(17) >= data_pipe(18)) AND
91    (data_pipe(17) >= data_pipe(16)) AND
92    (data_pipe(17) > data_pipe(15)) AND
93    (data_pipe(17) > data_pipe(19)) else '0';
94
```

Zero Suppression: Implementation

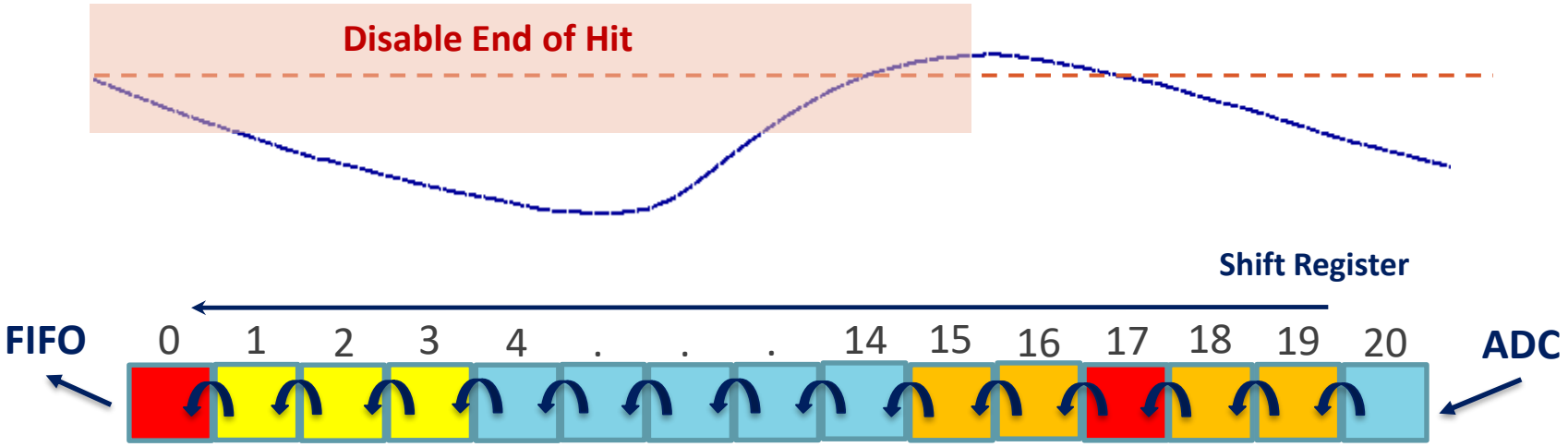



```
96    thr_low <= '1' when
97    (data_pipe(0) < THR_VALUE) AND
98    (data_pipe(1) < THR_VALUE) AND
99    (data_pipe(2) < THR_VALUE) AND
100   (data_pipe(3) < THR_VALUE) else '0';
101
```

- The hit ends if the registers from 0 to 3 are all under threshold and there are no peaks detected in the stream

- Time, Number of Samples, Position of the Peak and Error Flag are computed while the waveform pass thought the register and are available when the hit ends

Zero Suppression: Implementation

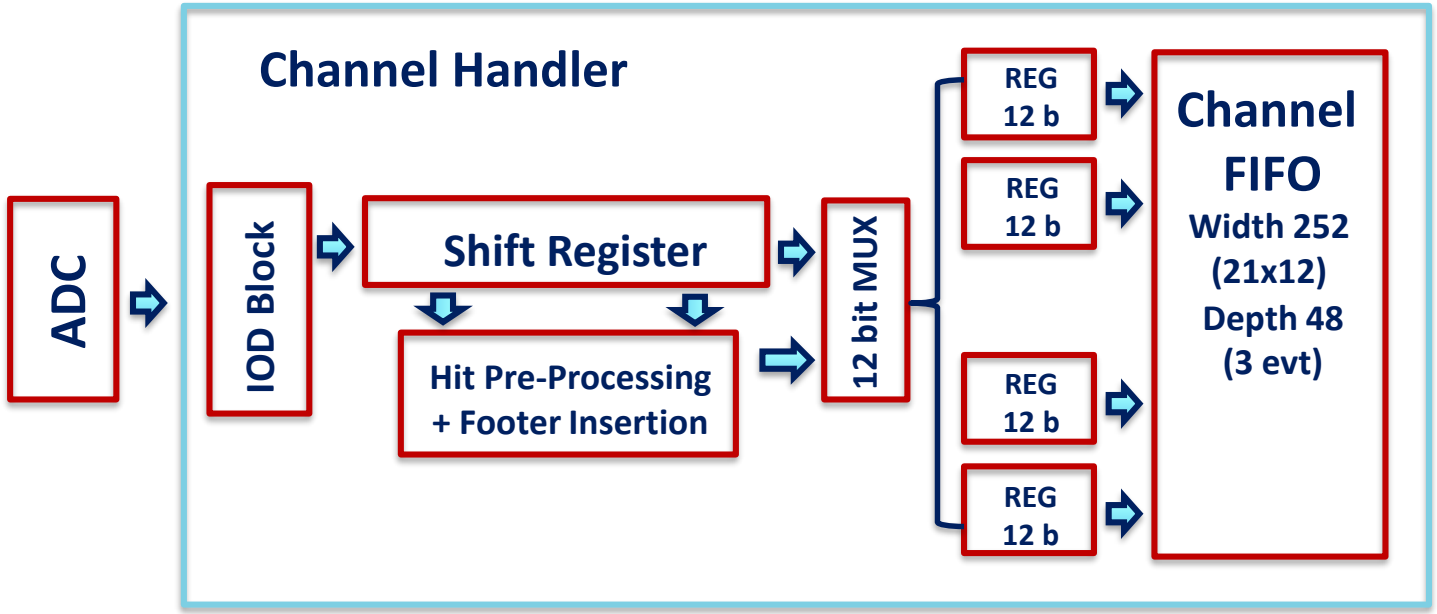


- If a peak is detected in position 17, the ‘under threshold’ condition is disabled until the peak arrives in position 0
- Afterwards, normal conditions apply

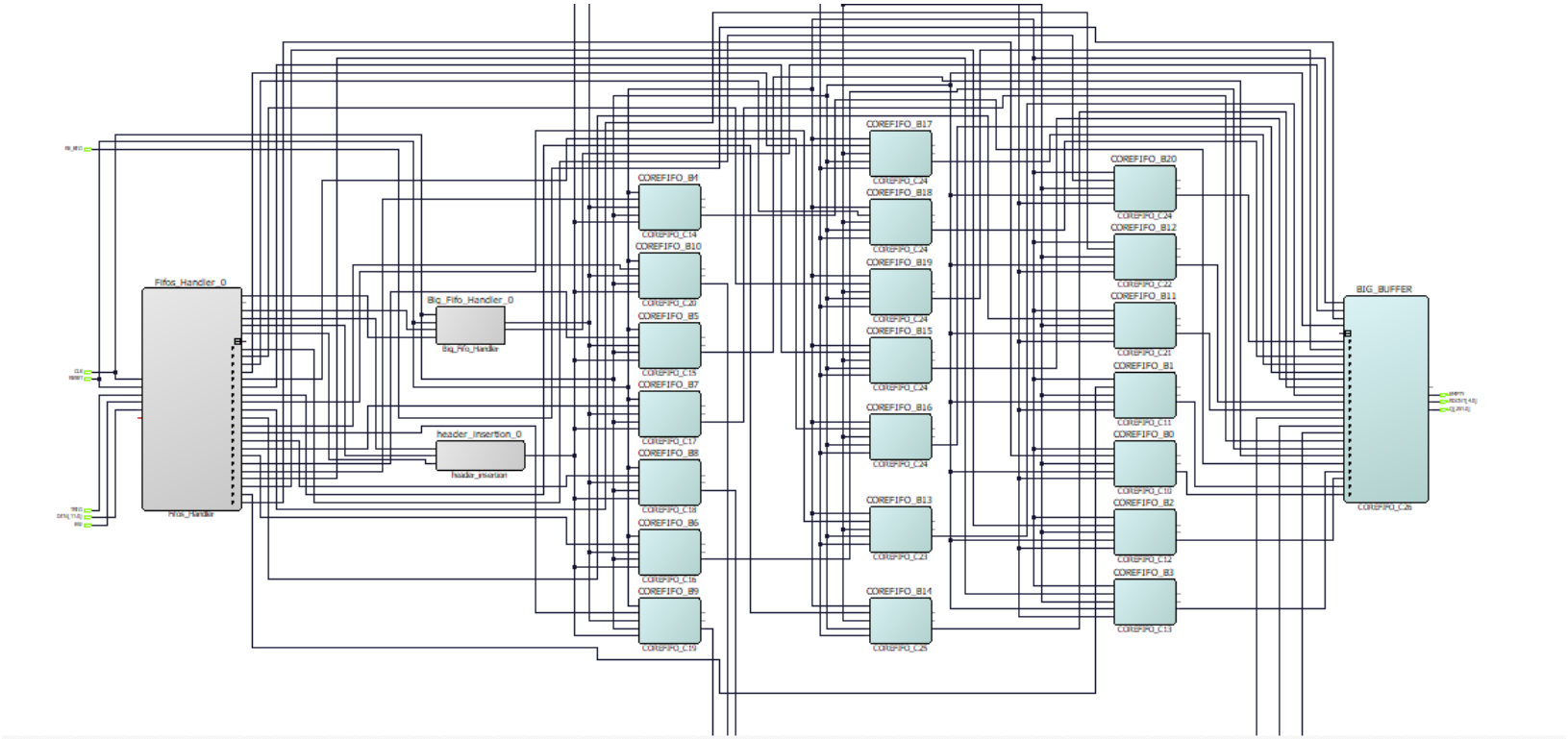
```
if (peak_flag = '1' and thr_flag = '1') then
  PIL_STATE <= BLIND_TH;
  pileup_counter := nBPEAKs;
else
  if (pileup_counter = 0) then
      pileup_counter := nBPEAKs;
      PIL_STATE <= WAIT_PEAK;
      continue_hit <= '0';
  else
      pileup_counter := pileup_counter - 1;
      PIL_STATE <= BLIND_TH;
  end if;
end if;
```

One Channel Pipeline

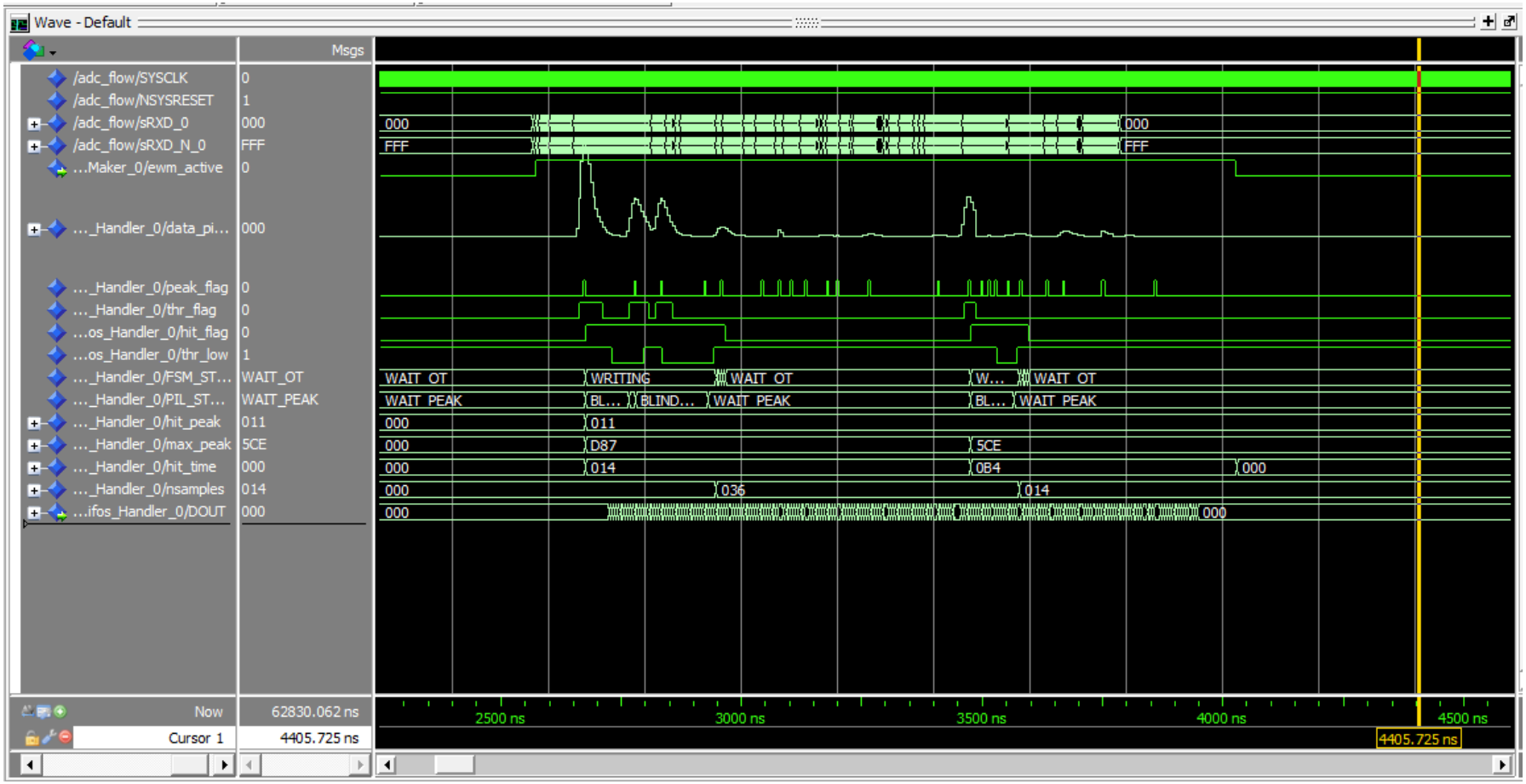
- To handle the data volume we decided to parallelize as much as possible the flux inside the FPGA
- The DDR memory is 32 bit wide with an operating frequency of 1333 MHz but it can be seen at the firmware level as a larger and slower memory : 256 bits with 166 MHz clock frequency -> 21 samples (12 bit wide) can be written in a single clock cycle



One Channel Firmware

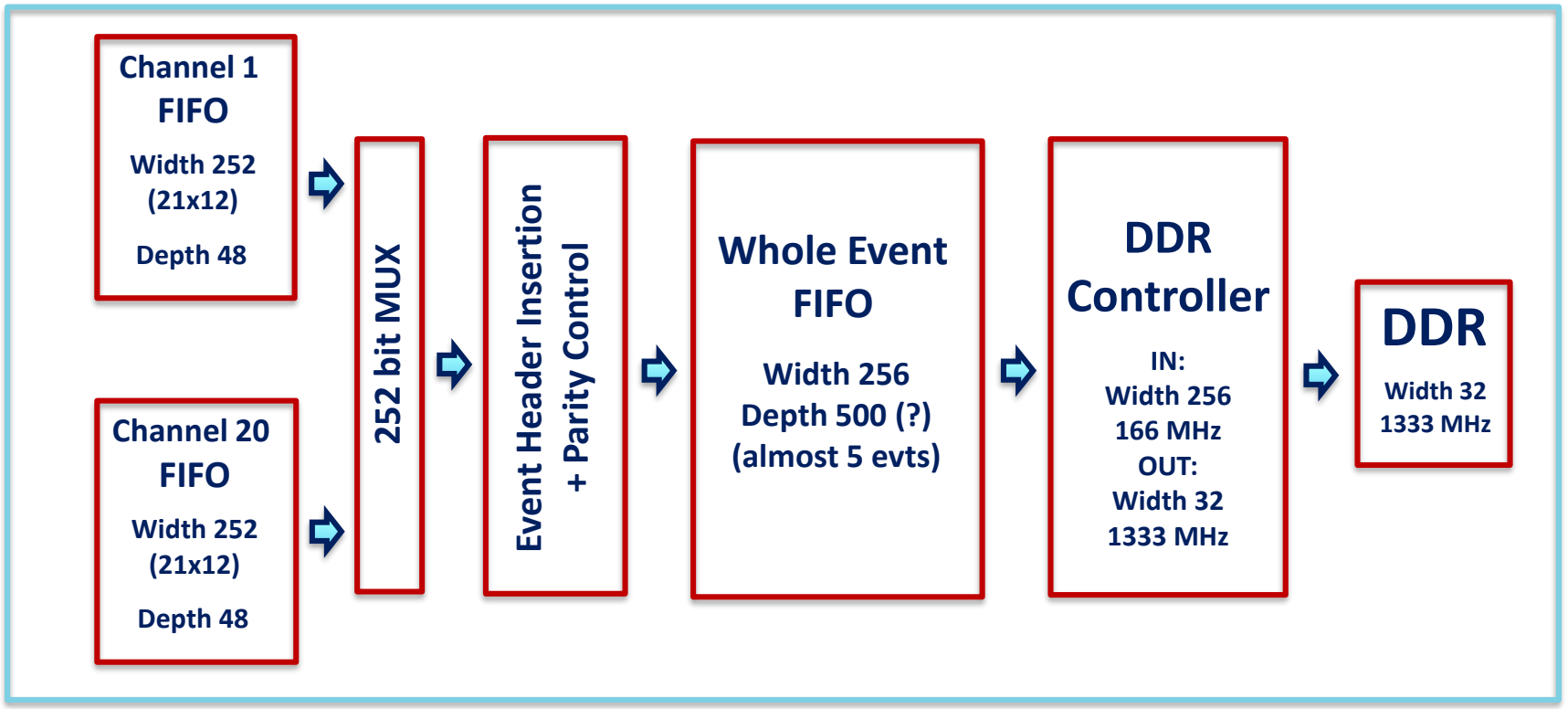


One Channel Simulation



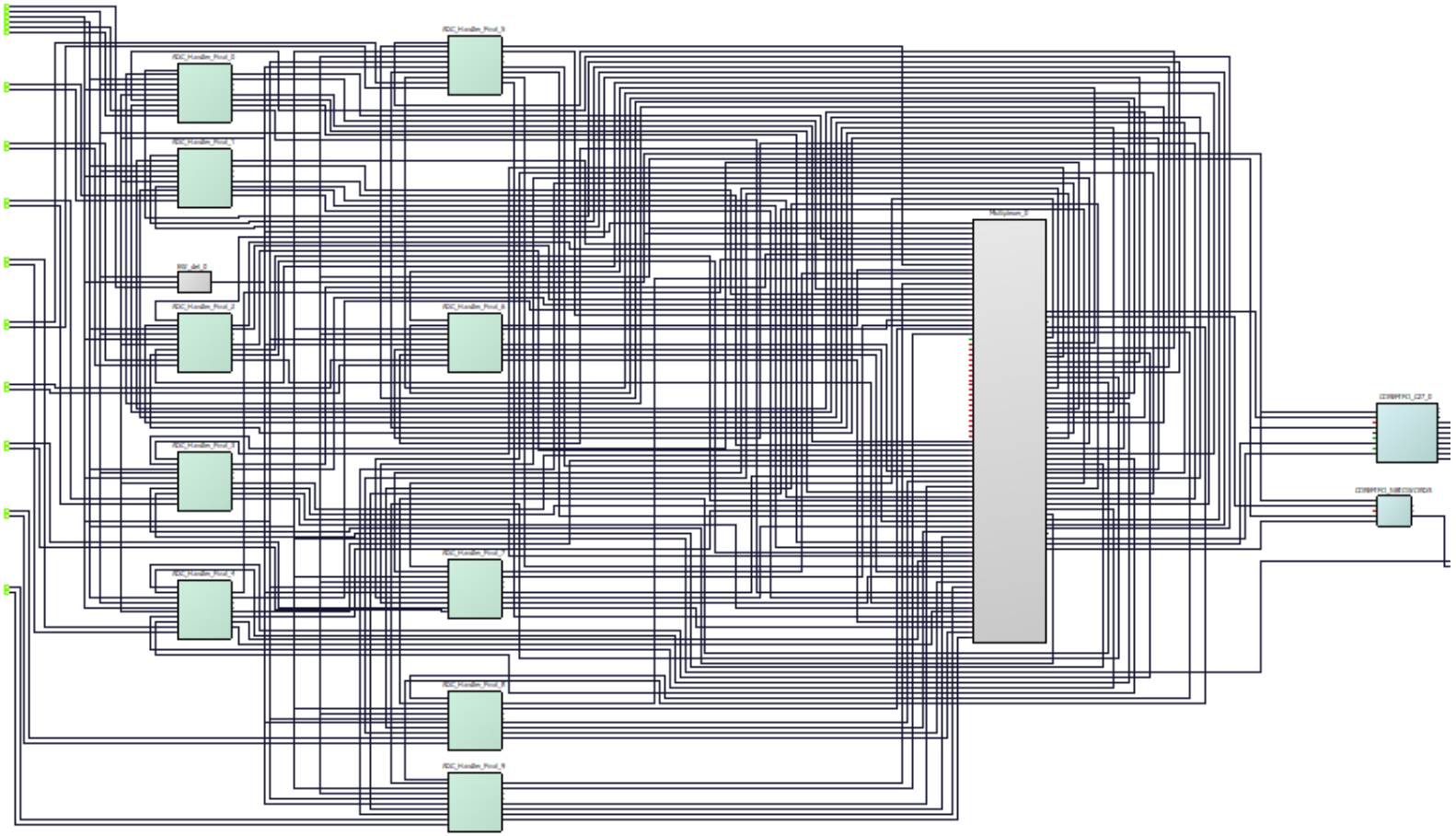
- This part is working as expected…

20 Channels Data Pipeline



- Data are conveyed into a 'whole event' FIFO where they are ready to be written in the DDR
- The depth of these FIFO has to be optimized with respect to a realistic simulation of the hit distribution and to the DDR performances (latency, read/write time, arbiter)

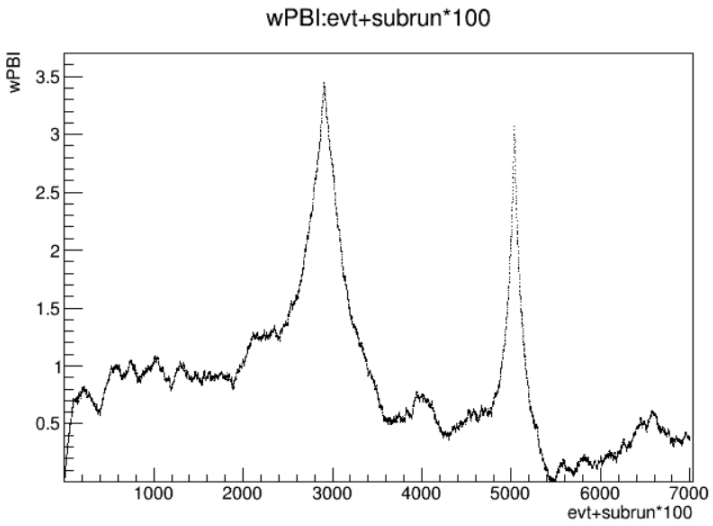
20 Channels Firmware



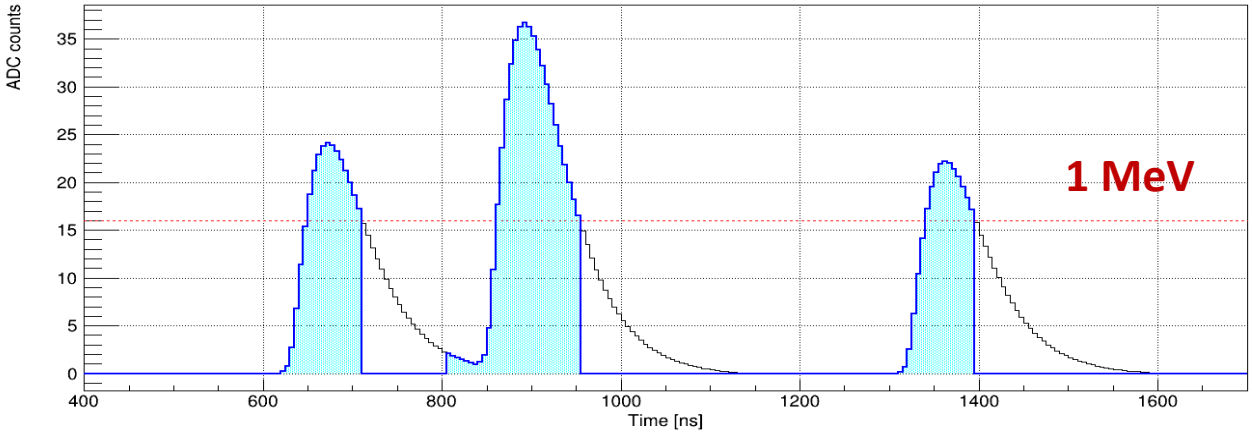
Post-Sinthesys Resources Usage

Module Name	Fabric 4LUT	Fabric DFF	Interface 4LUT	Interface DFF	Single-Ended I/O	Differential I/O Pairs	uSRAM 1K	LSRAM 18K	Chip
Top	35596	30756	21864	21864	5	133	1	607	21
Primitives	2	0	0	0	5	3	0	0	1
ADC_Block_0	858	1303	720	720	0	130	0	20	11
CLKBUF_DIFF_0	0	0	0	0	0	0	0	0	1
CLKBUF_DIFF_1	0	0	0	0	0	0	0	0	1
CORERESET_PF_C0_0	1	2	0	0	0	0	0	0	0
Data_Handler_Final...	34735	29451	21144	21144	0	0	1	587	4
Primitives	3	0	0	0	0	0	0	0	0
ADC_Handler_F...	2963	2832	2088	2088	0	0	0	58	0
ADC_Handler_F...	2961	2830	2088	2088	0	0	0	58	0
ADC_Handler_F...	2961	2830	2088	2088	0	0	0	58	0
ADC_Handler_F...	2961	2830	2088	2088	0	0	0	58	0
ADC_Handler_F...	2960	2830	2088	2088	0	0	0	58	0
ADC_Handler_F...	2961	2830	2088	2088	0	0	0	58	0
ADC_Handler_F...	2962	2830	2088	2088	0	0	0	58	0
ADC_Handler_F...	2960	2830	2088	2088	0	0	0	58	0
ADC_Handler_F...	2961	2830	2088	2088	0	0	0	58	0
ADC_Handler_F...	2961	2830	2088	2088	0	0	0	58	0
COREFIFO_C27_0	188	290	252	252	0	0	0	7	0
COREFIFO_NBI...	21	23	12	12	0	0	1	0	0
EW_del_0	0	25	0	0	0	0	0	0	0
Inganno_0	23	0	0	0	0	0	0	0	0
Inganno_1	21	0	0	0	0	0	0	0	0
Inganno_2	21	0	0	0	0	0	0	0	0
Inganno_3	21	0	0	0	0	0	0	0	0
Inganno_4	21	0	0	0	0	0	0	0	0
Inganno_5	21	0	0	0	0	0	0	0	0
Inganno_6	21	0	0	0	0	0	0	0	0
Inganno_7	21	0	0	0	0	0	0	0	0
Multi8_0	8	0	0	0	0	0	0	0	0
Multiplexer_0	4734	811	0	0	0	0	0	0	4

Stress Test Simulation: Dataset



- S. Werkema produced about 43.5 ms of beam intensity fluctuation and Kutschke simulated around 12 ms (7000 evts) of them
- The information regarding the calorimeter have been extracted and the waveforms have been constructed with the new signal shape
- An event list with about 7k evts has been prepared using the board with more occupancy



Stress Test Simulation: Testbench

- To test this firmware implementation we setup a testbench using a realistic digital simulation that includes the expected hit distribution for each channel and the luminosity fluctuation

FPGA Firmware VHDL

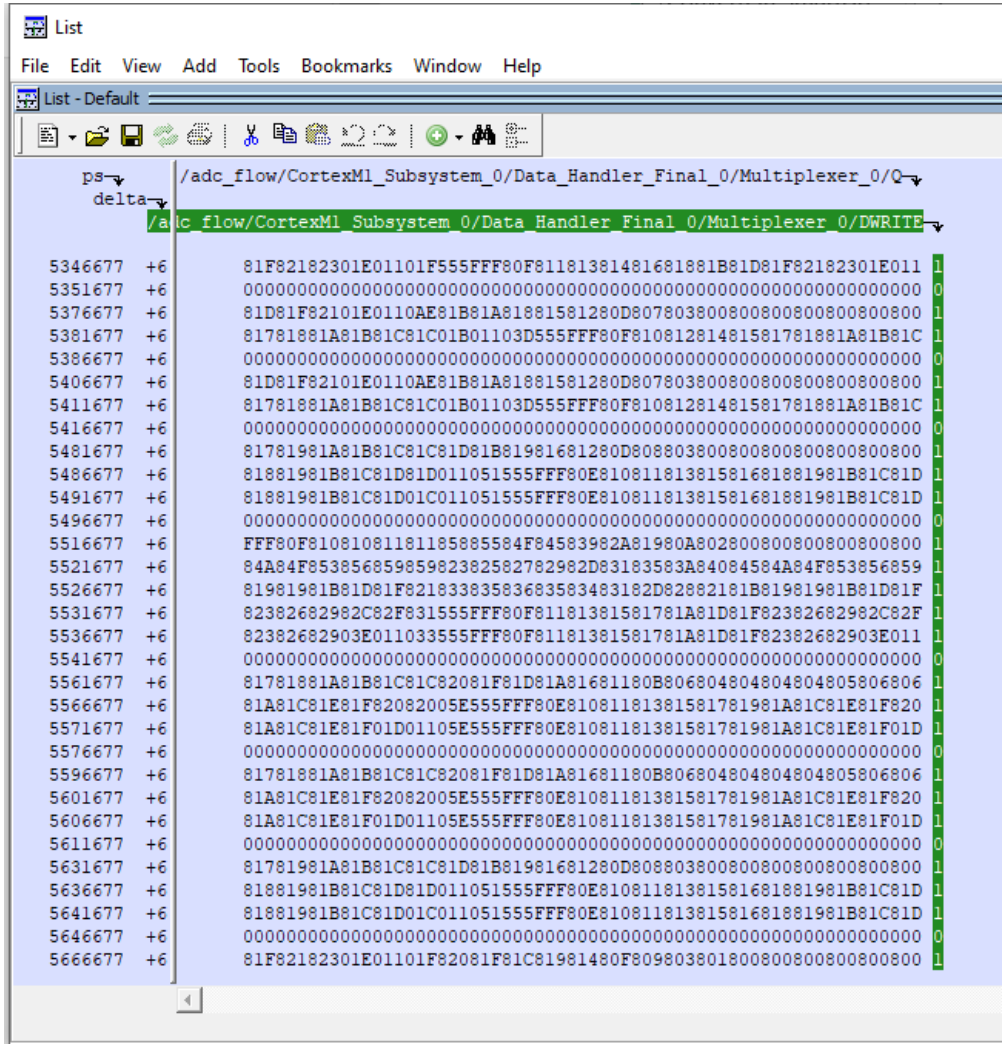
Modelsim Hardware Simulation

- **VHDL for external DDR modules is missing!**

Stress Test Simulation: Results

- Have been used 100 events in the worst region around the peak of the luminosity

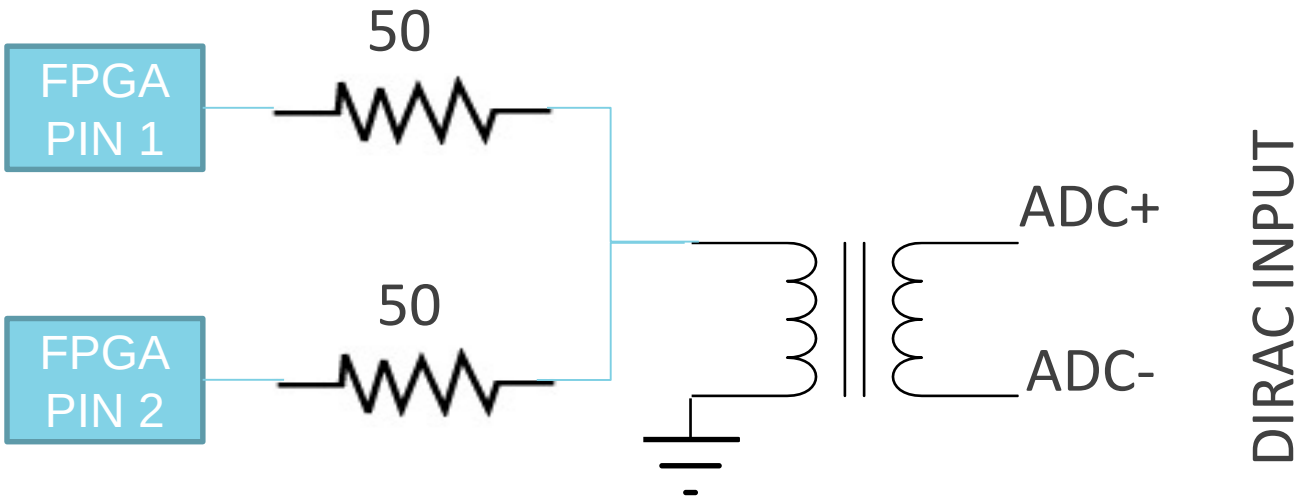
FIFO Content Check



- The FIFO has been filled without any bottleneck..
- To check the content we need a dedicated C++ simulation that reproduces the 256 bits words starting from the same text files
  - Script under development
- It remains to be seen if we are able to empty the FIFO and write into the external DDR at the right rate
  - The DDR clock is 166 MHz and not 200 MHz
  - Tracker group reported a big latency in the read/write operation
  - The VHDL model for the DDR is not available
- We are keeping the possibility open to pass from DDR3 to DDR4

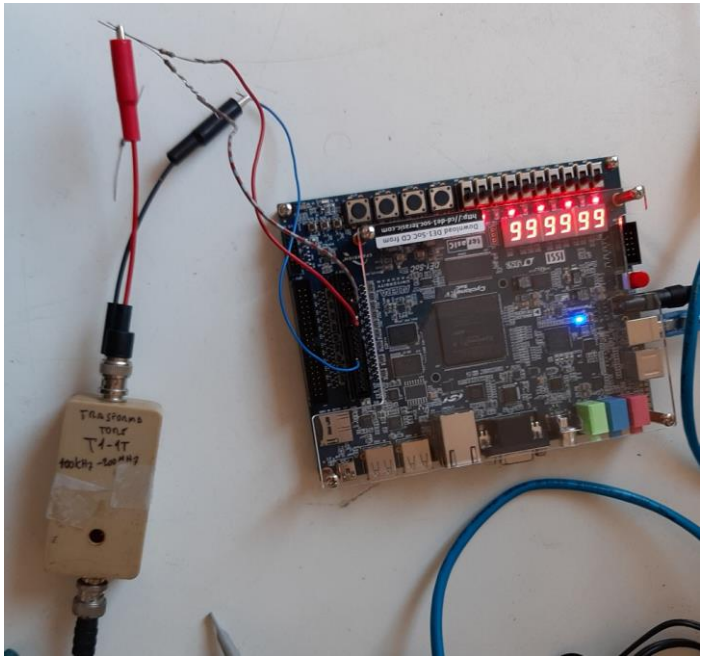
Hardware Stress Test

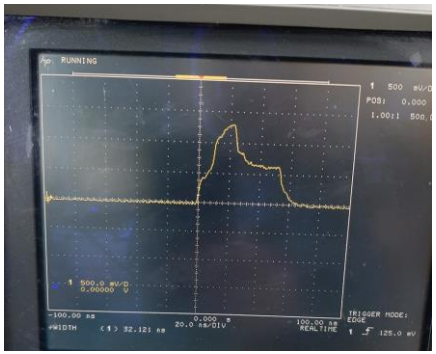
- To validate data bandwitdh in the DIRAC we don't need real waveforms.
- Square waves connected to the ADC inputs (V > THR) are enough and are easy to generate through digital outputs of an FPGA demo board.
- The algorithm uses the first peak as start for taking data so we plan to use 2 levels square waves to emulate real signals.

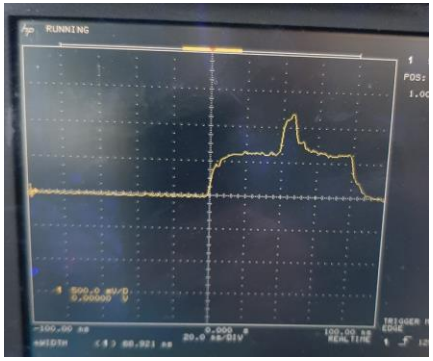


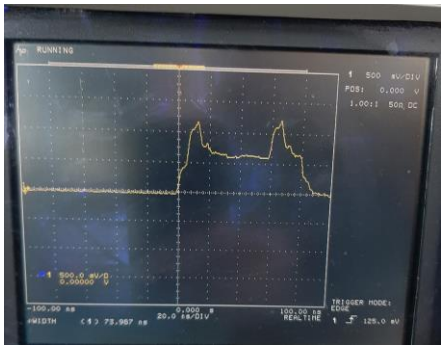
Hardware Stress Test

- Antonio has written a macro to convert the root file to a text file to fill a memory inside the pattern generator FPGA (includes 128 event windows) pattern generator FPGA

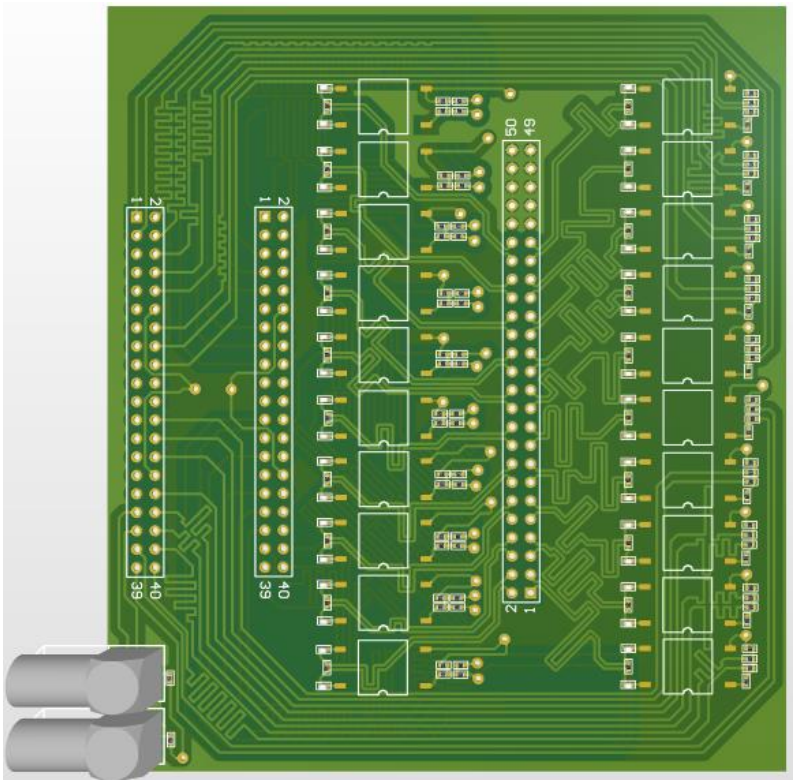


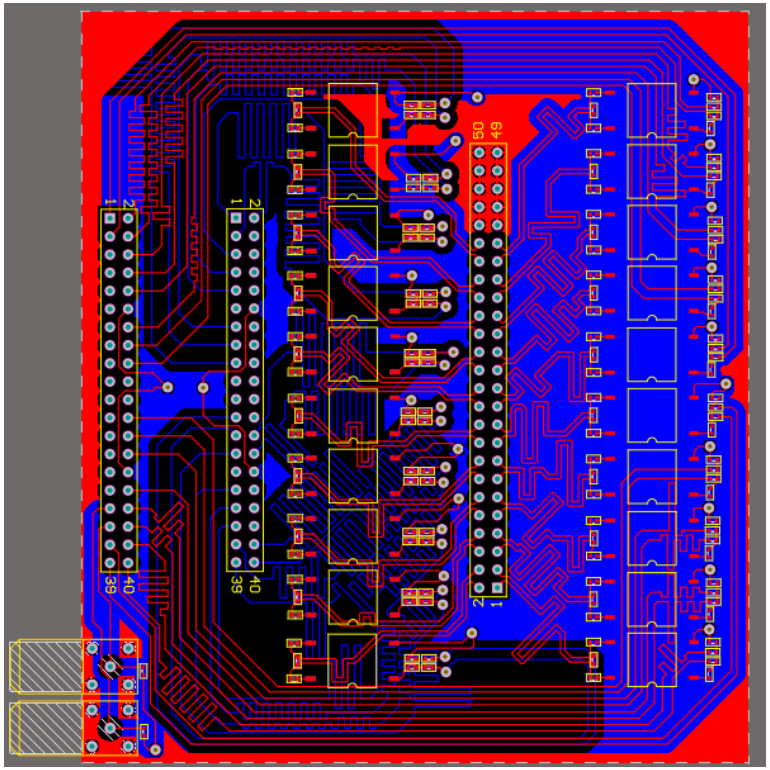






Hardware Stress Test





- Interface to DIRAC, include transformers to convert single ended digital signals to differential

Summary

- We completed a first version of the firmware that includes the interface with the DTC, the interface with the RAM and the final packaging of data
- The data flow inside the FPGA has been studied and a first version of this part of the firmware has been written and simulated using a realistic digital simulation that includes the expected hit distribution for each channel and the luminosity fluctuation
  - So far the FPGA seems to substain the data flux, but the VHDL model of external DDR is missing
- Same data stream can be used to stress test the real hardware using as waveform generator an FPGA demo board
  - All the materials for the test have been purchased