DIRAC and TRAD System status

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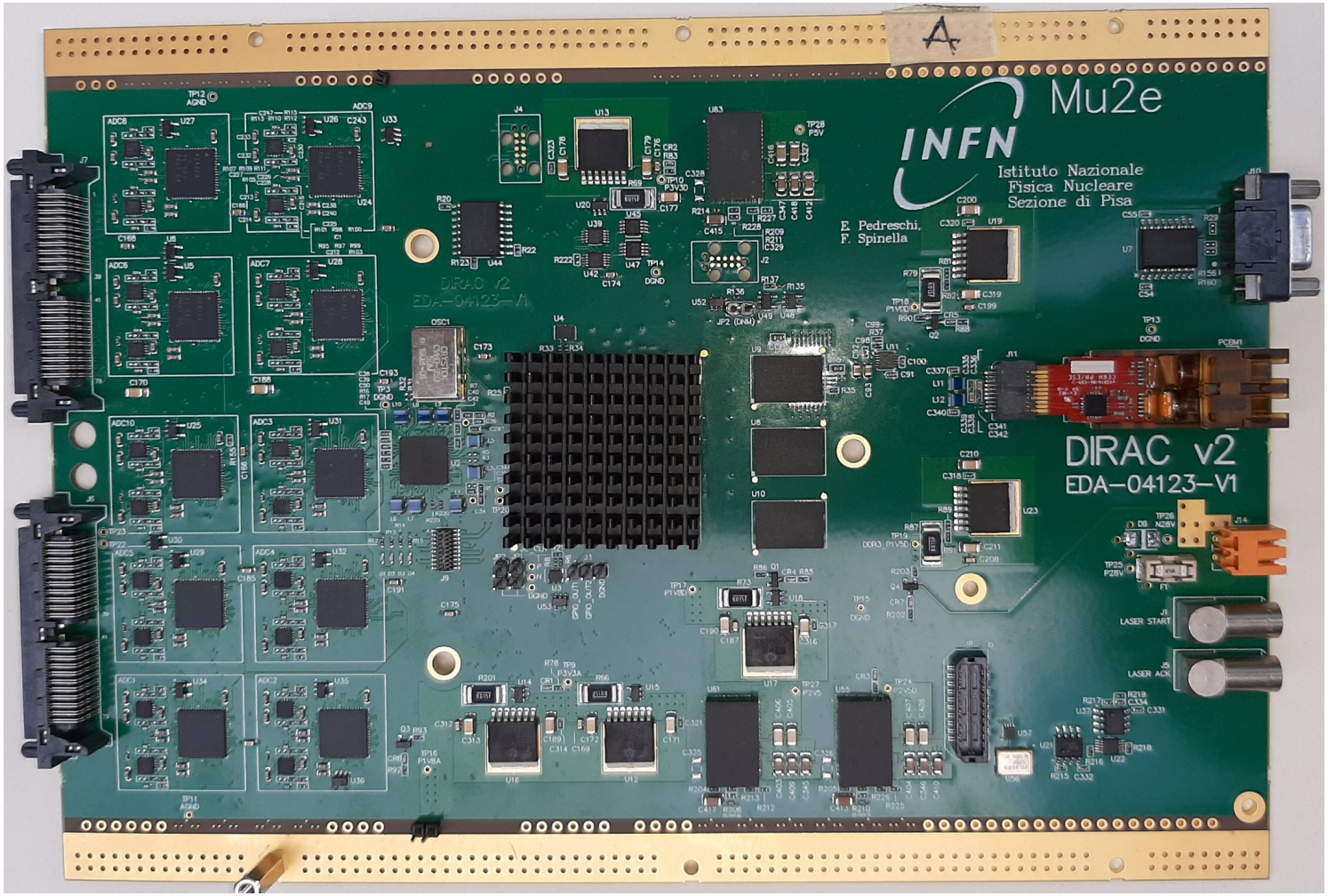
Mu2e Italia CM

03-September-2020

Outline

- DIRAC V2
- TRAD System
- Plans

DIRAC V2 (1)



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DIRAC V2 (2)

- Rispetto alla DIRAC V1:

  - ❑ Polarfire FPGA (più rad-hard, 2 volte più grande, più veloce)
  - ❑ VTRX (ricevitore ottico)
  - ❑ Supporta DDR3 fino a 2 Gbyte (attualmente 2 schede con DDR3 da 0.5 Gbyte e 2 schede da 1 Gbyte)
  - ❑ Sistema di monitoring migliore (V, I e T)
  - ❑ CAN bus
  - ❑ Nuovi DCDC converter (più rad-hard)
  - ❑ Albero di clock più efficiente
  - ❑ Stessa interfaccia analogica (ADCs, amplificatori, …)

DIRAC V2 test

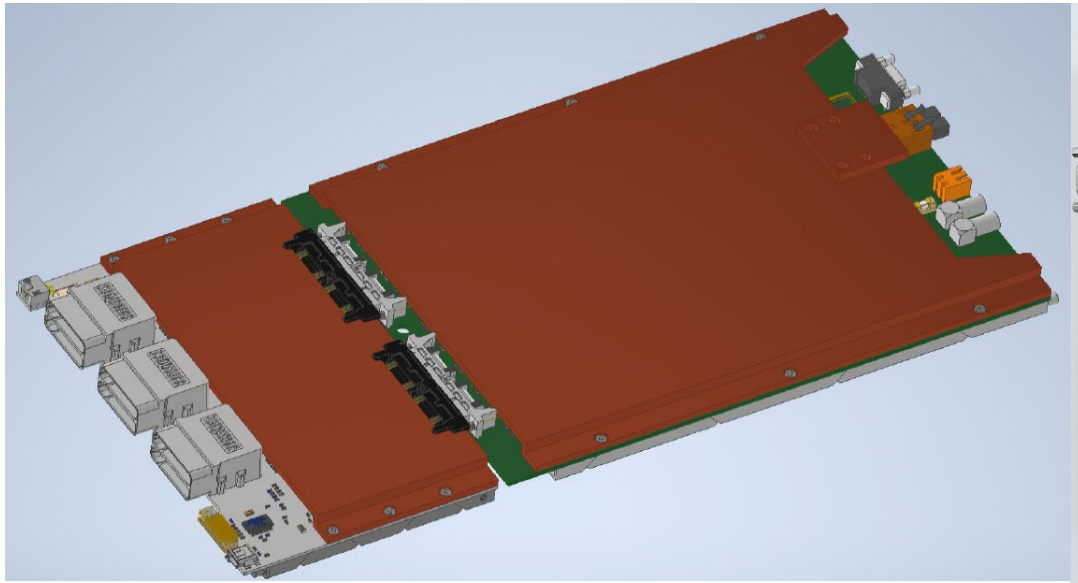
- Test funzionali :
  - ❑ Schema di power
  - ❑ ADC (20 canali)
  - ❑ Albero di clock + Jitter cleaner (SPI + ARM Cortex M1 synth.)
  - ❑ DDR test
  - ❑ Readout della fibra + clock recovery attraverso la fibra + OTSdaq
  - ❑ ADC di monitoring, Interface to laser system
  - ❑ CAN bus test (work in progress…)

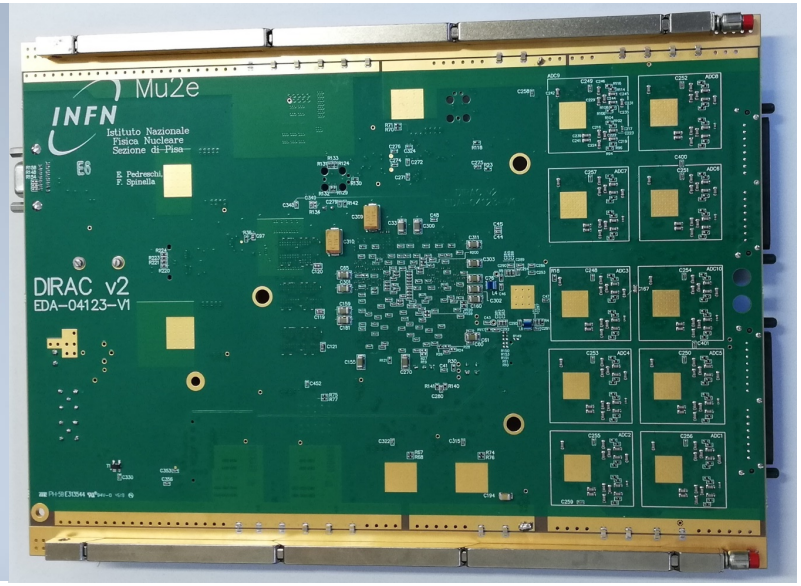
- Test mancanti (a causa della Pandemia di COVID 19):

  - ❑ Test dei 20 canali sul Modulo0
  - ❑ Lettura tramite fibra dei dati provenienti da dati simulati realistici alla massima velocità
  - ❑ Test finali TID,SEU,B (a livello di componenti fatti nel 2019)

Thermal interface: cardlocks and copper plate

- I Cardlock si adattano bene alla scheda
- Piastra in rame per la dissipazione termica per Mezzanine board e DIRAC V2 progettata, prototipo in arrivo





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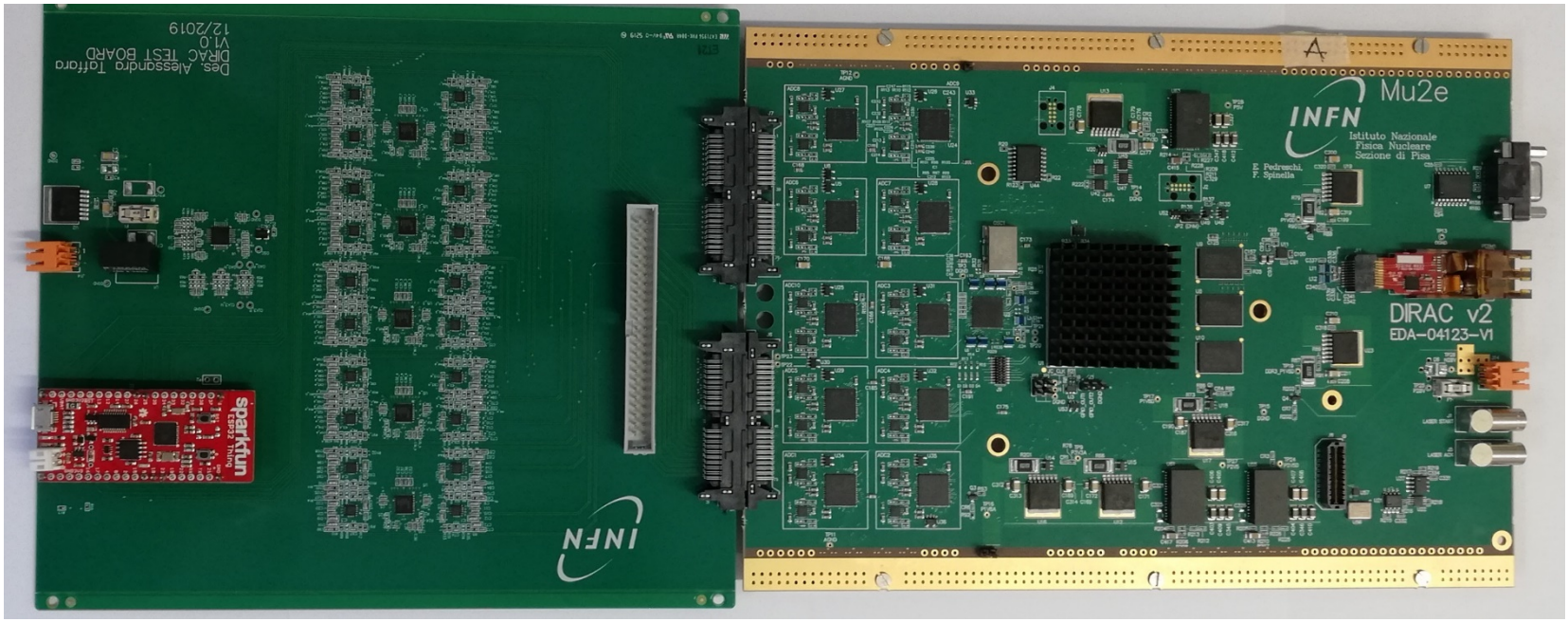
DIRAC V2 TEST Board

- TEST Board emula la Mezzanina and FEE (20 canali)
- Impulsa la DIRAC V2 ai test di radiazione and nei test di validazione delle schede di produzione.
- Utile per valutare eventuali crosstalk fra i canali
- Impulsi programmabili a piacere (20 channels AWG) attraverso una ESP32 CPU



DIRAC V3

- Piccolo errore sullo stampato: è necessario spostare di 2 mm il VTRx
- Daremo il via al masterista del CERN solo dopo aver effettuato i test di qualifica mancanti (l'errore è del CERN)

Produzione

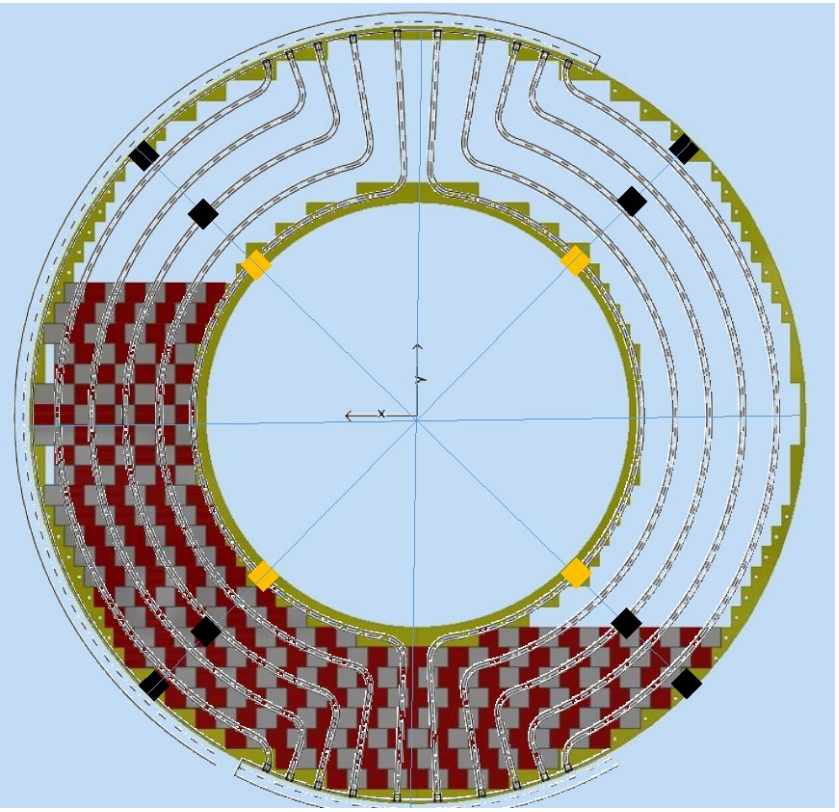
- L’assegnazione delle gare si è conclusa a luglio
- Abbiamo autorizzato l’acquisto del 90% dei componenti
- I rimanenti saranno acquistati al termine di tutti i test e a quel punto daremo il via alla pre-produzione delle schede (10 pezzi)
- in questo momento a Pisa ne abbiamo 4 funzionanti

Sistema TRAD (1)

- I sensori T-Rad sensori per il sistemaTRAD sono:
  - Termometro Digitale (Maxim Integrated DS18S20Z) ➔ Temperatura (T);
  - SiPM (ON Semiconductor MICROFC−60035−SMT) ➔ Fluenza di neutroni (n);
  - Radfet (Tyndal TY1003) ➔ Dose (rad);
- Dal momento che su tutte le DIRAC ci saranno i sensori di T e I (T anche su FEE):
  - La copertura dei sensori T-RAD dovrà essere garantita solo sull superficie frontale (Front Face) del calorimetero
  - Si può pensare di posizionare qualche sensore T-Rad sensors anche sul piatto frontale del FEE (FEE PLATE) ➔ **é necessario**?
- 2 schede TRAD per disco ➔ ogni scheda leggerà non più di 6 (or 9) sensori

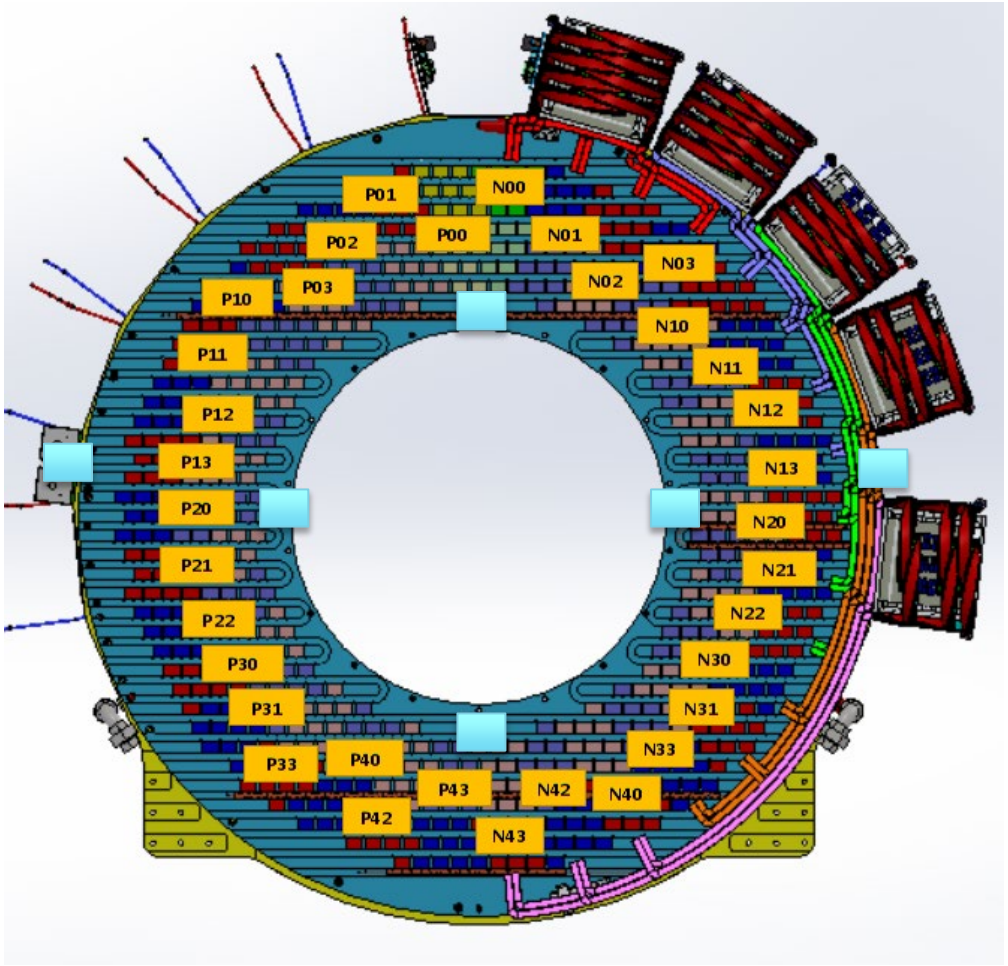
Sistema TRAD (2)

FRONT-FACE



12 rad, 12 n, 12 T OK

FEE-PLATE



(6 rad, 6 n, 6 T) servono?

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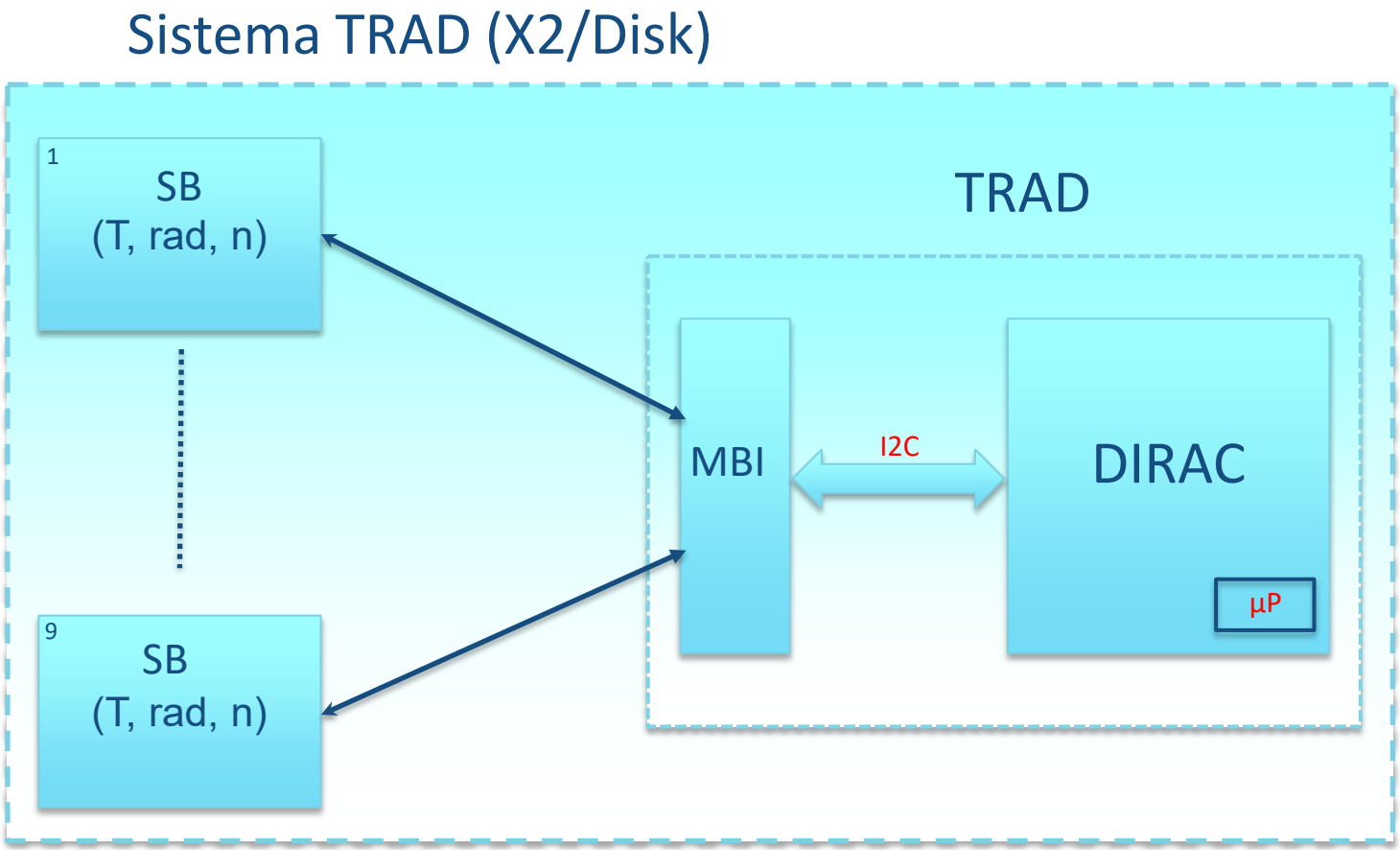
TRAD System schematic block

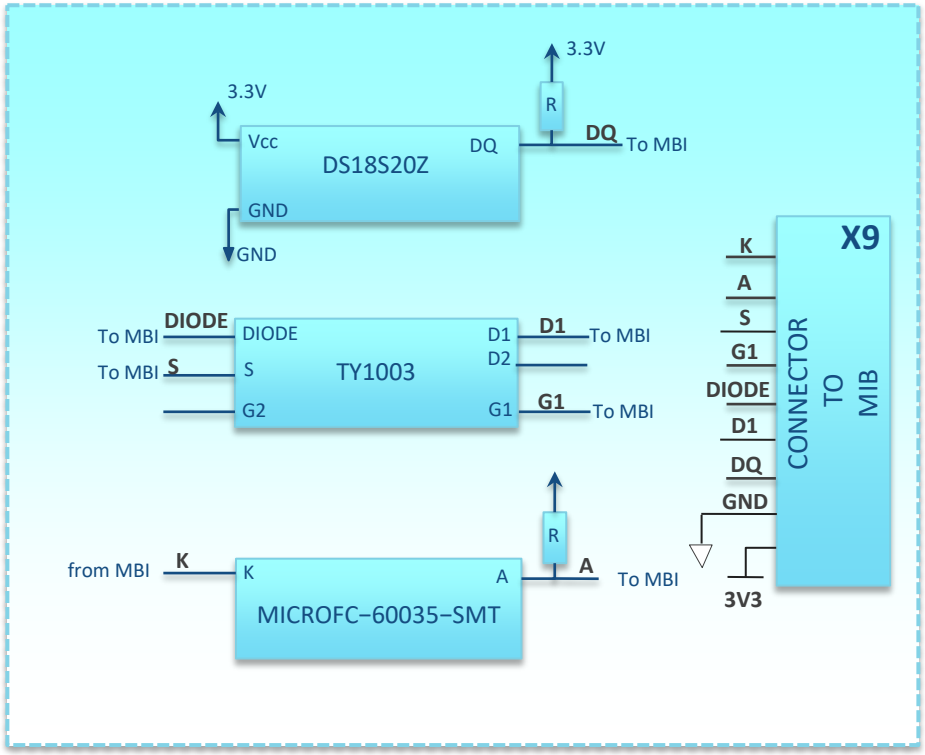


*SB → Sensor Board

**MBI → Mezzanine Board Interface

Sensors Board schematic block

Sensors Board



T-Rad sensors:

- Digital Thermometer (Maxim Integrated DS18S20Z) ➔ Temperature (T);
- Radfet (Tyndal TY1003) ➔ Dose (rad);
- SiPM (ON Semiconductor MICROFC−60035−SMT) ➔ Neutron fluence (n);

Temperature Sensor

DS18S20 **High-Precision 1-Wire Digital Thermometer**

General Description

The DS18S20 digital thermometer provides 9-bit Celsius temperature measurements and has an alarm function with nonvolatile user-programmable upper and lower trigger points. The DS18S20 communicates over a 1-Wire bus that by definition requires only one data line (and ground) for communication with a central microprocessor. In addition, the DS18S20 can derive power directly from the data line ("parasite power"), eliminating the need for an external power supply.

Each DS18S20 has a unique 64-bit serial code, which allows multiple DS18S20s to function on the same 1-Wire bus. Thus, it is simple to use one microprocessor to control many DS18S20s distributed over a large area. Applications that can benefit from this feature include HVAC environmental controls, temperature monitoring systems inside buildings, equipment, or machinery, and process monitoring and control systems.

Applications

- Thermostatic Controls
- Industrial Systems
- Consumer Products
- Thermometers
- Thermally Sensitive Systems

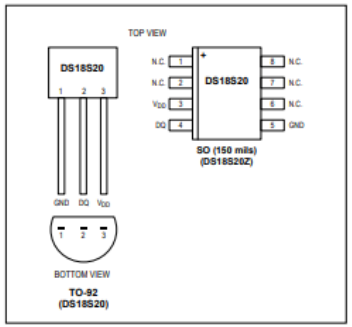
Ordering Information appears at end of data sheet.

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

Benefits and Features

- Unique 1-Wire® Interface Requires Only One Port Pin for Communication
- Maximize System Accuracy in Broad Range of Thermal Management Applications
  - Measures Temperatures from -55°C to +125°C (-67°F to +257°F)
  - ±0.5°C Accuracy from -10°C to +85°C
  - 9-Bit Resolution
  - No External Components Required
- Parasite Power Mode Requires Only 2 Pins for Operation (DQ and GND)
- Simplifies Distributed Temperature-Sensing Applications with Multidrop Capability
  - Each Device Has a Unique 64-Bit Serial Code Stored in On-Board ROM
- Flexible User-Definable Nonvolatile (NV) Alarm Settings with Alarm Search Command Identifies Devices with Temperatures Outside Programmed Limits
- Available in 8-Pin SO (150 mils) and 3-Pin TO-92 Packages

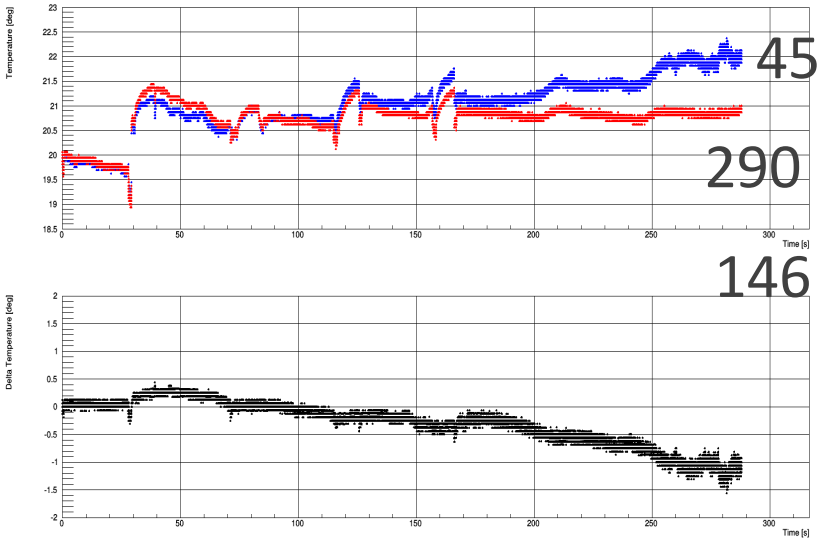
Pin Configurations



maxim integrated

19-5474; Rev 3; 4/15

- The DS18S20 comunica attraverso il bus 1-wire
- Il Termometro Digitale testato nel 2018 @ Enea:
  - Dose rate 1.85 krad/h unshielded (red)
  - Dose rate 0.3 krad/h shielded (blu)



45 Krad

290 Krad

146 ore

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Dose Sensor

Varadis

DATASHEET: VT01

TECHNICAL DATA
VT01
400nm RADFET
in 6L SOT-23 Plastic package

VT01 Description and Pin-Out

The VT01 is Varadis 400nm RADFET chip packaged in a plastic SOT-23 six lead package.

The part consists of two identical RADFETs, R1 and R2, and a diode (see Figure 1 and Table 1). The RADFETs' gate oxide thickness is 400nm and W/L is 300µm/50µm. The RADFETs have individual gate and drain terminals, while the source and bulk are common and connected together; this is also the diode bulk contact.

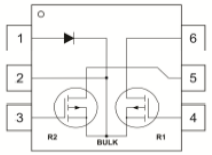


Figure 1: VT01 pin-out drawing.

Table 1: VT01 pin-out description.

Pin Number	Description
1	Diode anode
2	Source/bulk (common)
3	Gate of R2
4	Gate of R1
5	Drain of R2
6	Drain of R1

Calibration Data

The calibration curve for the RADFET shows evolution of ΔV (the change in RC threshold voltage with reference to its pre-irradiation value) with dose. Note that a specific calibration curve, obtained using the Co-60 source, is associated with each RADFET production batch. The calibration curve, together with analytical equation and fitting coefficients, will be provided with the supplied parts. For illustration, typical calibration curve is shown in Figure 4.

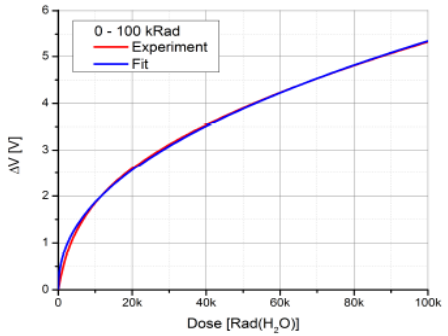
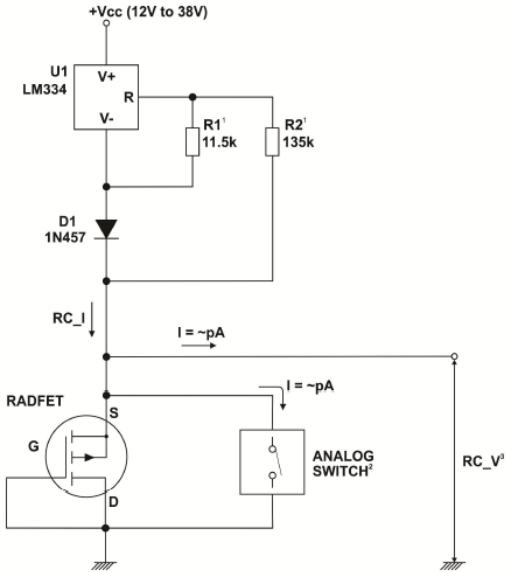


Figure 4: Typical calibration curve indicating change in RC_V during irradiation. Irradiation at room temperature with Co-60 gamma source, dose rate ~50 Gy/h (5 krad/h).. Voltage measurements performed at room temperature using 0.2% duty cycle with all terminals grounded between measurements

3 rev 1.4 (June 2020)

- Tyndal TY1003 (ora Varadis VT01)
- Varadis è uno sin-off di Tyndall National
- Testato dalla compagnia fino a 100krad @ temperature ambiente
- Dal datasheet di Varadis lo schema del circuito di sensing del RADFET è:



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Neutron Sensor

C-Series SiPM Sensors

Silicon Photomultipliers (SiPM), Low-Noise, Blue-Sensitive

The C−Series low-light sensors from ON Semiconductor feature an industry-leading low dark-count rate combined with a high PDE. For ultrafast timing applications, C-Series sensors have a fast output that can have a rise time of 300 ps and a pulse width of 600 ps. The C−Series is available in different sensor sizes (1 mm, 3 mm and 6 mm) and packaged in a 4-side tileable surface mount (SMT) package that is compatible with industry standard, lead-free, reflow soldering processes.

The C−Series Silicon Photomultipliers (SiPM) form a range of high gain, single-photon sensitive, UV-to-visible light sensors. They have performance characteristics similar to a conventional PMT, while benefiting from the practical advantages of solid-state technology: low operating voltage, excellent temperature stability, robustness, compactness, output uniformity, and low cost. For advice on the usage of these sensors please refer to the Biasing and Readout Application Note.

ON Semiconductor®

www.onsemi.com

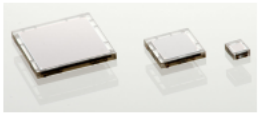


Figure 1. C−Series Sensors

ORDERING INFORMATION

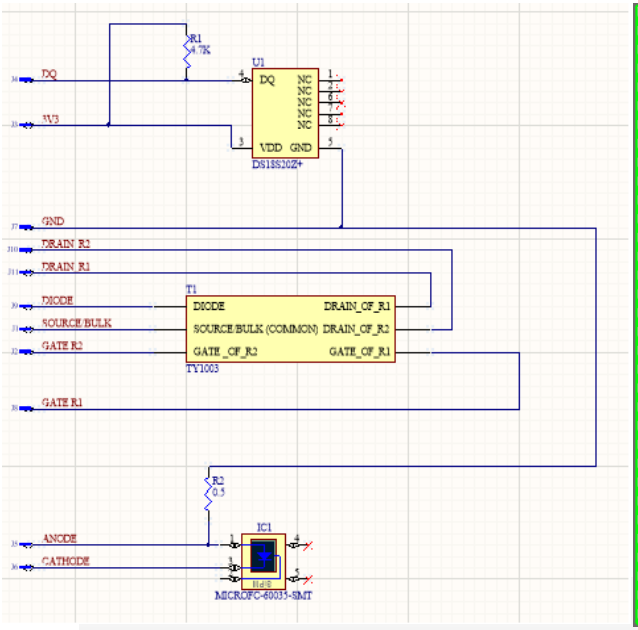
See detailed ordering and shipping information on page 15 of this data sheet.

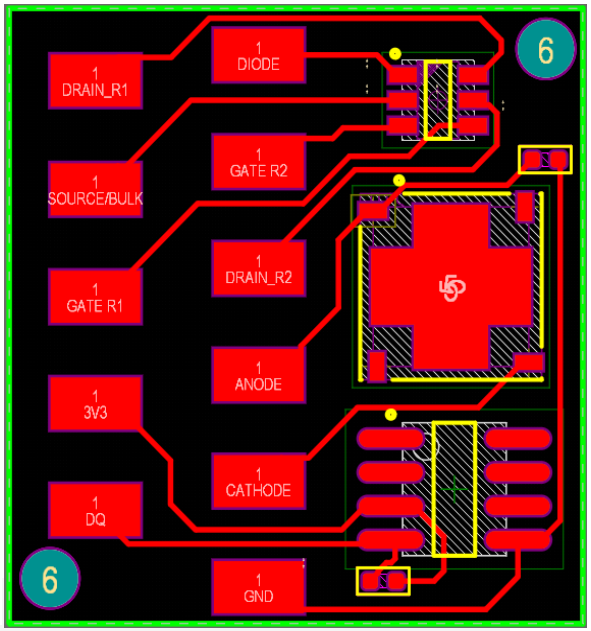
Table 1. PERFORMANCE PARAMETERS

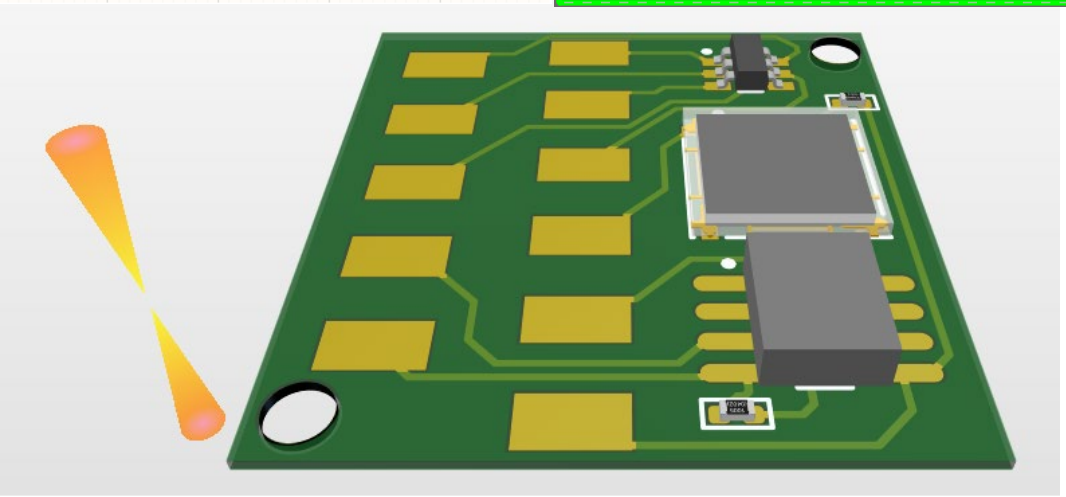
Sensor Size	Microcell Size	Parameter (Note 1)	Overvoltage	Min.	Typ.	Max.	Units
1 mm	10μ, 20μ, 35μ	Breakdown Voltage (Vbr) (Note 3)		24.2		24.7	V
3 mm	20μ, 35μ, 50μ						
6 mm	35μ						
1 mm	10μ, 20μ, 35μ	Recommended overvoltage Range (Voltage above Vbr) (Note 2)		1.0		5.0	V
3 mm	20μ, 35μ, 50μ						
6 mm	35μ						
1 mm	10μ, 20μ, 35μ	Spectral Range (Note 4)		300		950	nm
3 mm	20μ, 35μ, 50μ						
6 mm	35μ						
1 mm	10μ, 20μ, 35μ	Peak Wavelength (λp)			420		nm
3 mm	20μ, 35μ, 50μ						
6 mm	35μ						

- Idark è funzione della fluenza di neutroni e della temperatura
- C-Series SiPM Vbias is ~ 25V (Mu2e SiPM 170V) → si usa 28V dalla DIRAC
- Saranno testate @ FNG to:
  - Valutare il trend della Idark con I neutroni
  - calibrare in funzione della fluenza di neutroni e della temperatura
- I sensori saranno allocate in posizioni differenti del detector → temperature diverse

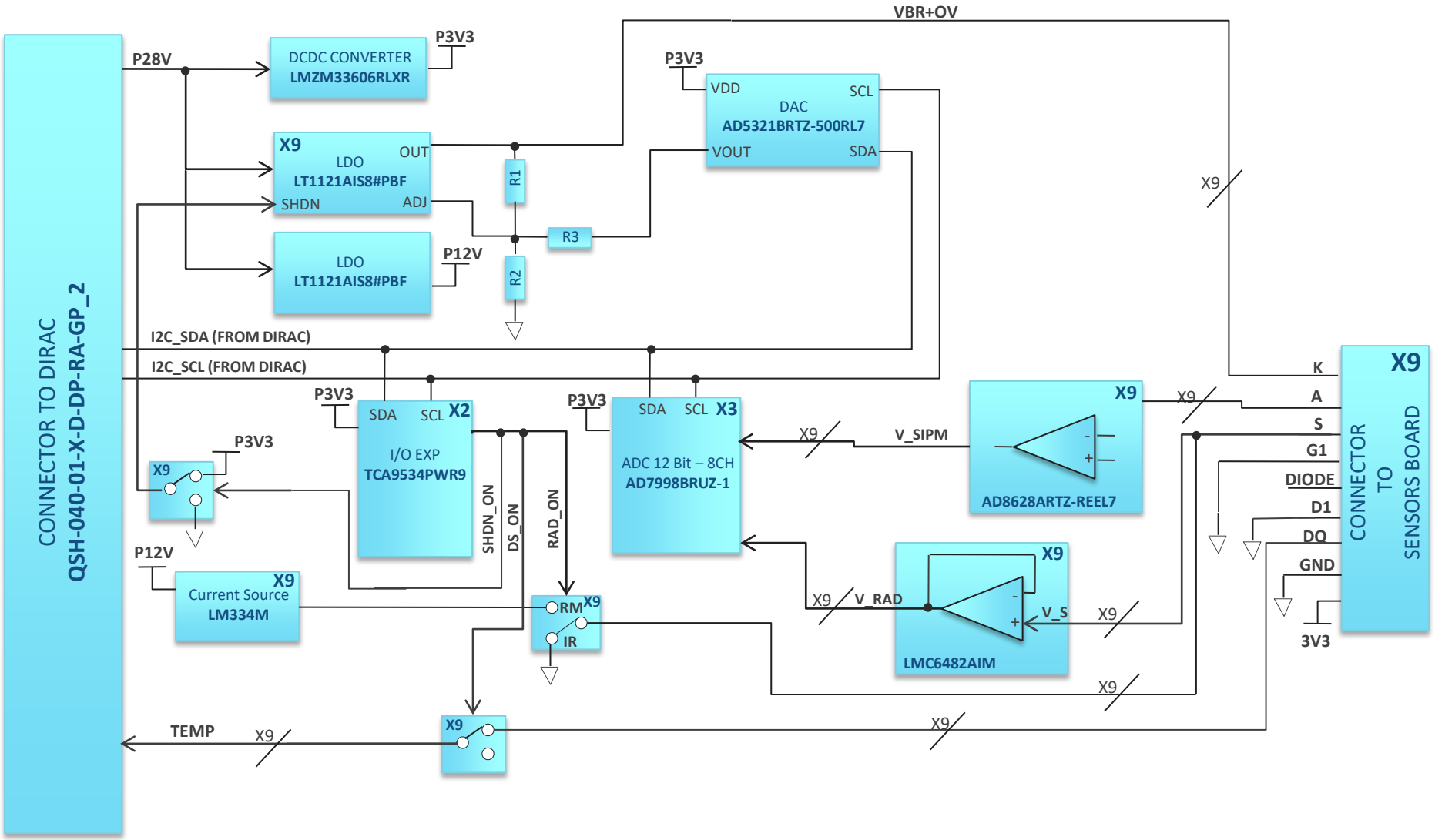
Sensor Board Altium project



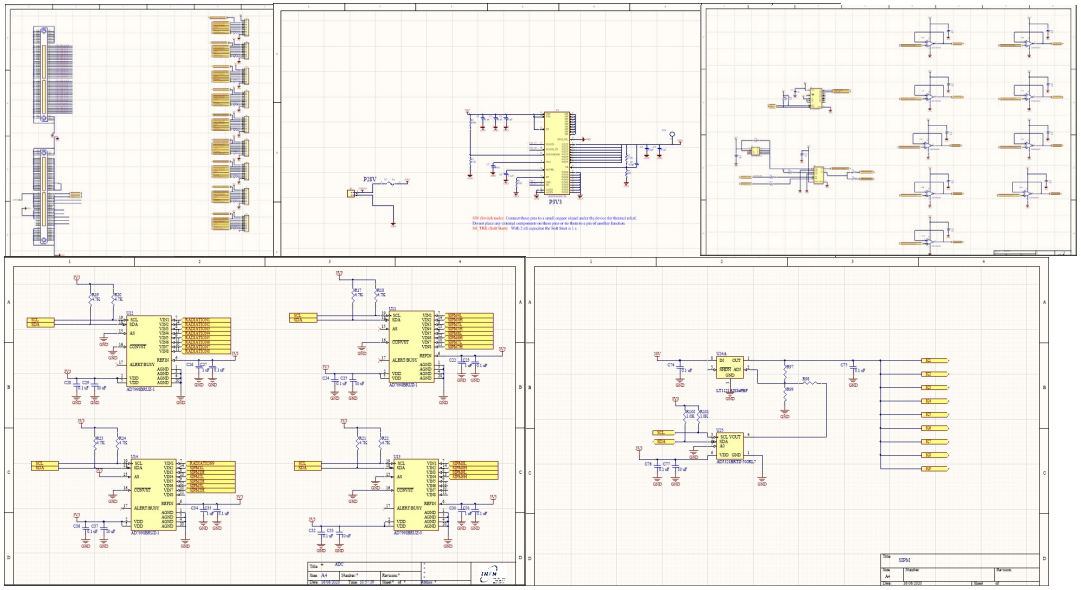




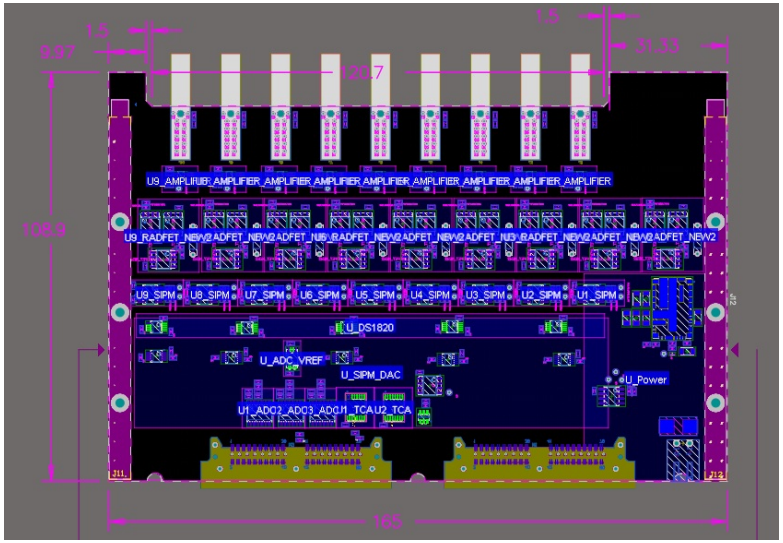
Mezzanine Board Interface schematic block

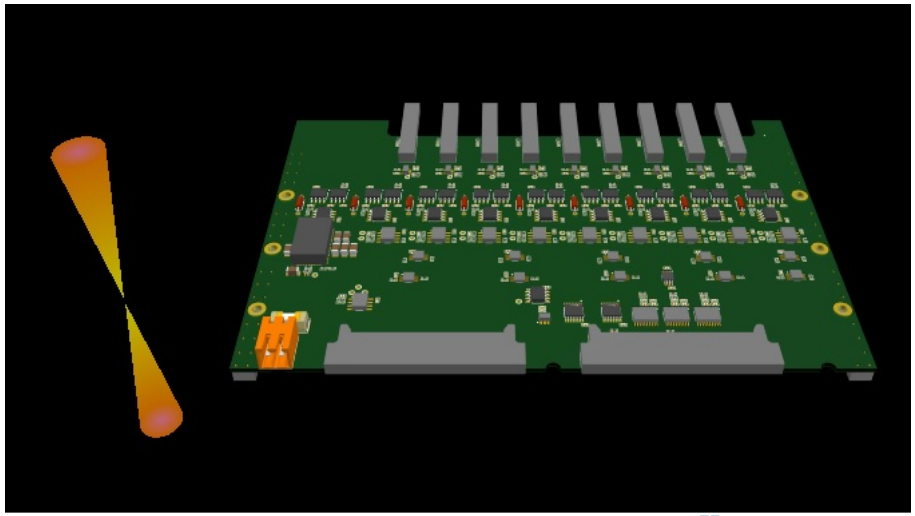


Mezzanine Interface Board



- Schemi completi
- Routing quasi completo
- Stesso fattore di forma della mezzanina del FE
- Connettori verso SB 2 opzioni:
  - ❑ Harting (fig.) → 36 canali
  - ❑ 6µD → 24 canali

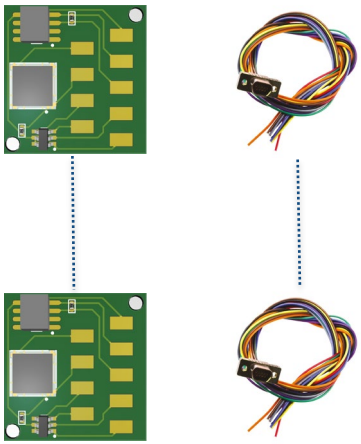




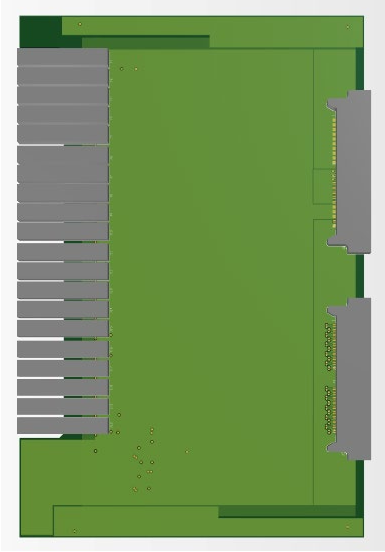
Plans

- Sensor board pcb sarà ordinato in questi giorni
- Tutti I component della SB (except radfet) già ordinati e in stock a Pisa
- TY1003 saranno ordinati a giorni
- Gli schemi della MIB sono stati completati, lo sbroglio è quasi completato (Pisa)
- Stiamo pianificando i test dei SiPM e la calibration @FNG Facility
- I test dei SiPm saranno effettuati direttamente utilizzando la catena SB, MIB e DIRAC

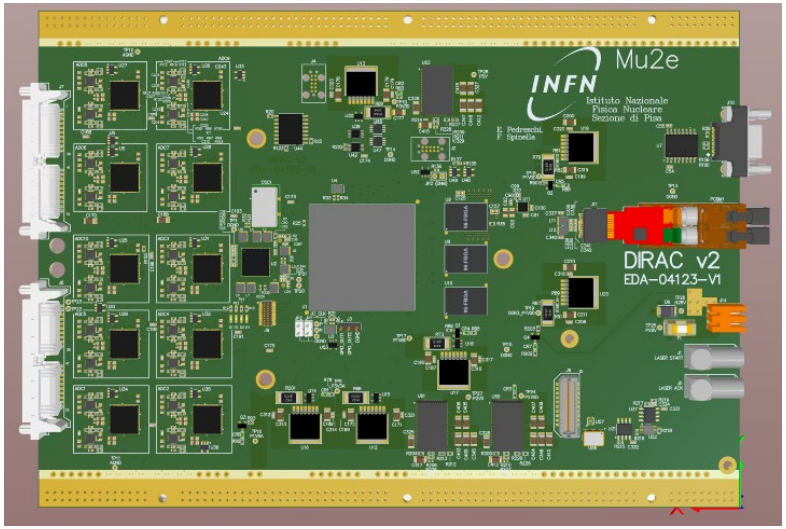
SBs



MIB



DIRAC



Thank you for the attention!