A Readout System for the HEPD-02 Tracker

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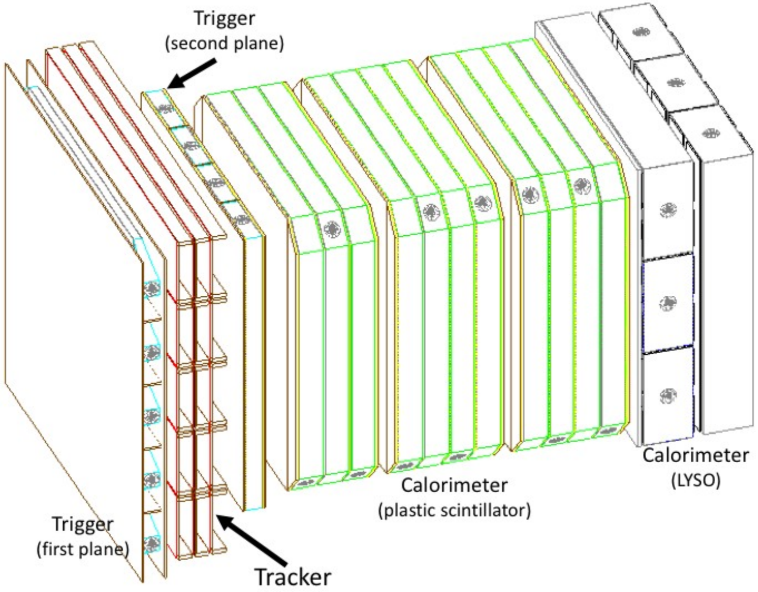
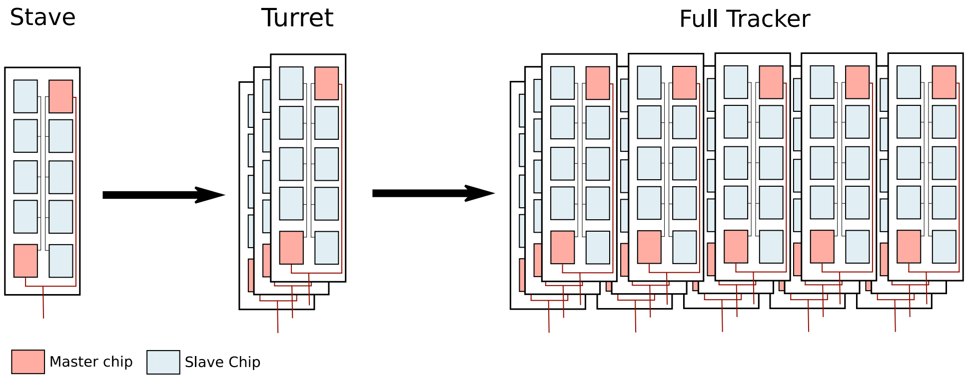
HEPD-02

High Energy Particle Detector (HEPD) to measure fluxes of particles trapped in the magnetosphere in the 3-150 MeV range for electrons and 30-300 MeV for protons.



- 3-planes detector tracker based on the ALPIDE pixel sensor.



- Two layers of crossed trigger bars, aligned with the tracker turrets.
- 11-tiles plastic scintillator + two layers of LYSO scintillators.
- Shrouded in Containment/Veto detectors.

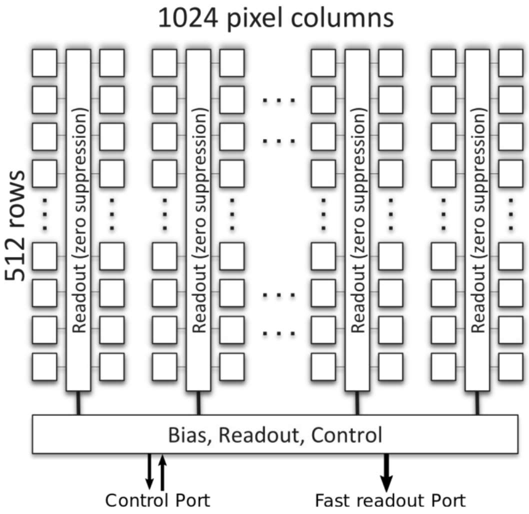
Challenges

The use of a pixel tracker over micro-strip detectors offer advantages but also some new challenges:

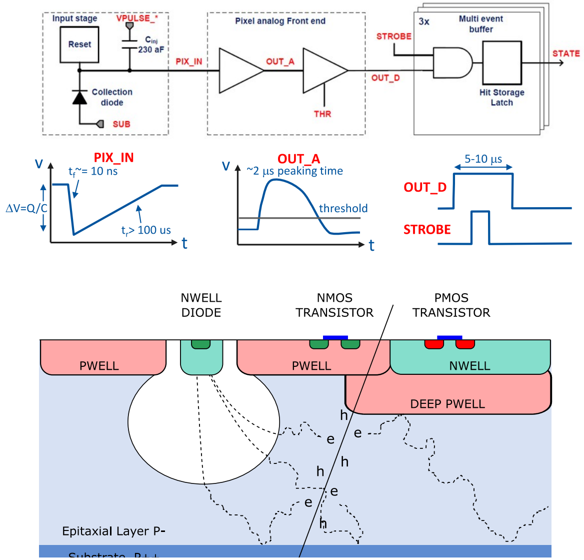
- Physics: Higher angular resolution.
- Sparse readout scheme: keep data rate to a value acceptable for a space mission.
- Power budget: Digital pixel sensors have higher power requirements, requiring some tuning to fit in the power budget of the mission.

ALPIDE sensor

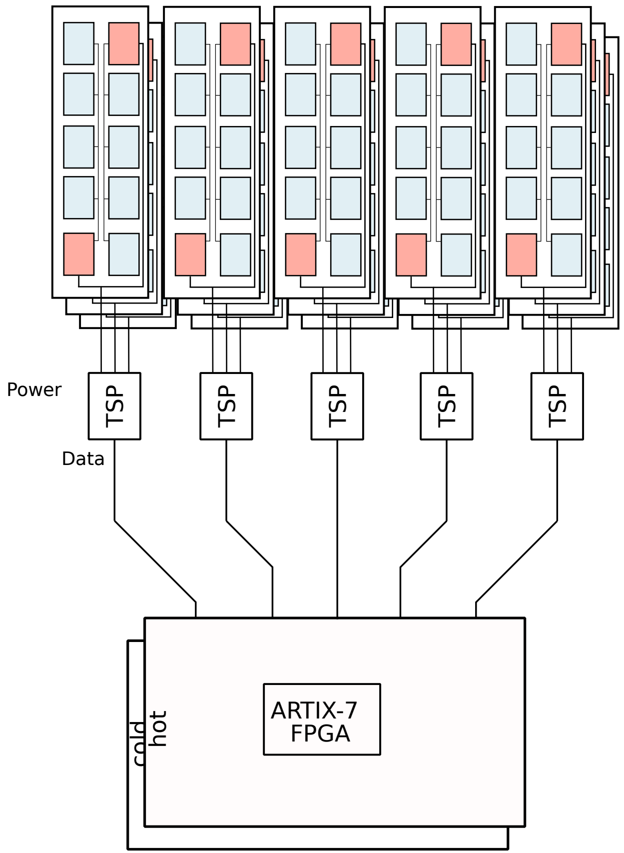
15 × 30 mm² CMOS Monolithic Active Pixel Matrix sensor composed by a 1024x512 pixel matrix with in-pixel digital readout.



- Each pixel generates a binary output (hit/no-hit) after a trigger command.
- Readout executed on groups of two columns, with zero suppression and efficient cluster coding.
- Fast readout port (up to ~1 Gbps) + slow readout side-channel from the control port (~1 Mbps).



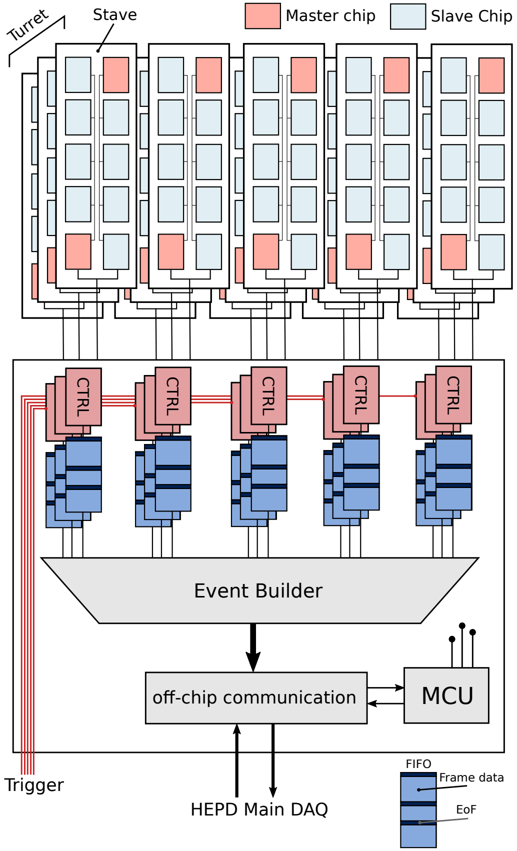
Tracker DAQ



Readout of the tracker is managed by a single board (TDAQ) with a low power FPGA.

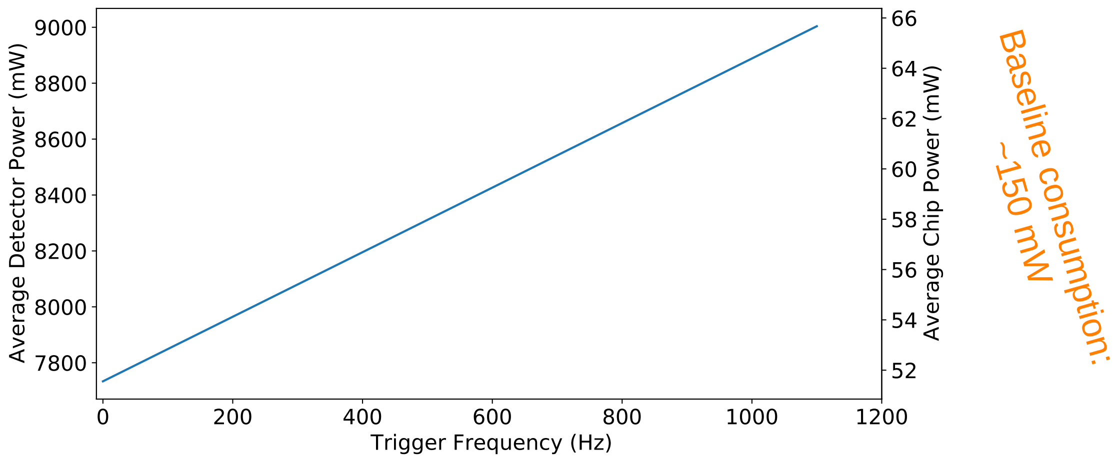
- Very small event rate/size expected so only slow readout port is used, avoiding the prohibitive power consumption of high speed serializers.
- Data lines are separated from power by a Tracker Splitting Board.
- Each turret has 3 data channels plus clock signals to the chips.
- TDAQ board communicates with main HEPD DAQ board via a ~100 Mbps spacewire link.

Power Consumption Reduction

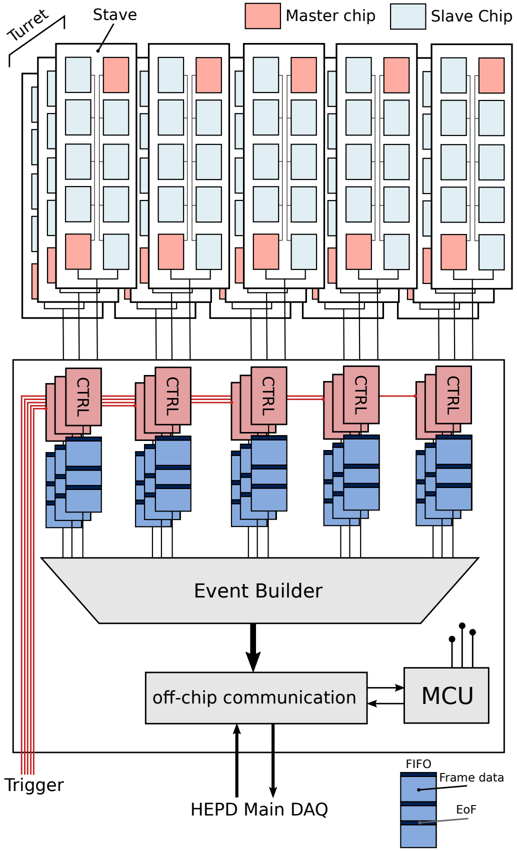


The readout of the tracker is performed in parallel on each stave and employs clock gating to save power.

- 15 readout cores ("CTRL") propagate the trigger to the staves (triggered tower + 2 adjacent) and implement a readout finite state machine.
- Clock signal is provided to a turret only when a trigger is received and then disabled after readout.



Event Packaging



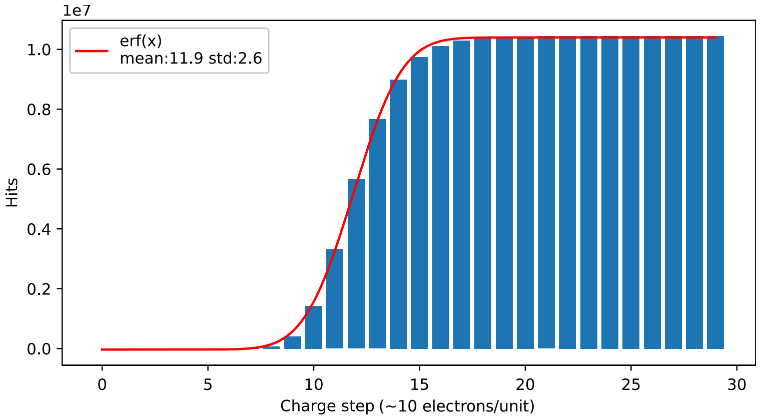
All data collected after a trigger is packaged in a single “event package”.

- Another stage of zero suppression gives a further large reduction of raw data rate.
- Event package is tagged and time-stamped for synchronization with other sensors in HEPD-02.
- Cyclic Redundancy Check to detect transmission errors in data payload.

Calibration Procedures

On board soft-CPU implemented in the FPGA will perform in-flight calibration and telemetry procedures:

- Threshold scan: injecting charge in pixel to measure pixel sensitivity.
- Masking of noisy pixels (detrimental to detector dead time and on data rate).
- Gather diagnostic data such as staves temperature.



Conclusions

- Physical tracker design and production procedure already defined (also see talk “*Assemblaggio e caratterizzazione del tracciatore a pixel monolitici di silicio per HEPD-02*” by L. De Cilladi).
    - Turret prototype produced and passed space qualification testing.

- Prototype of the readout system near completion and already tested on a turret prototype.
    - Readout and clock gating procedure implemented and validated.
    - Calibration procedure defined and in process of validation.
    - Further work on power consumption characterization and optimization in progress.