

# CYGNO DAQ meeting

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# CYGNO DAQ meeting

- Digitizer module for SiPM:
  - Components selected: ADC (quad, 500 MSPS), FPGA (Arria 10 with processor), uC (PIC Ethernet and USB ports)
  - Schematics drawing already started (PIC section)
- Selection of technologies for camera readout
  - Comparison of different commercial Frame Grabbers

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## 14-Bit, 500 MSPS, JESD204B, Quad Analog-to-Digital Converter

Data Sheet

**AD9694**

### FEATURES

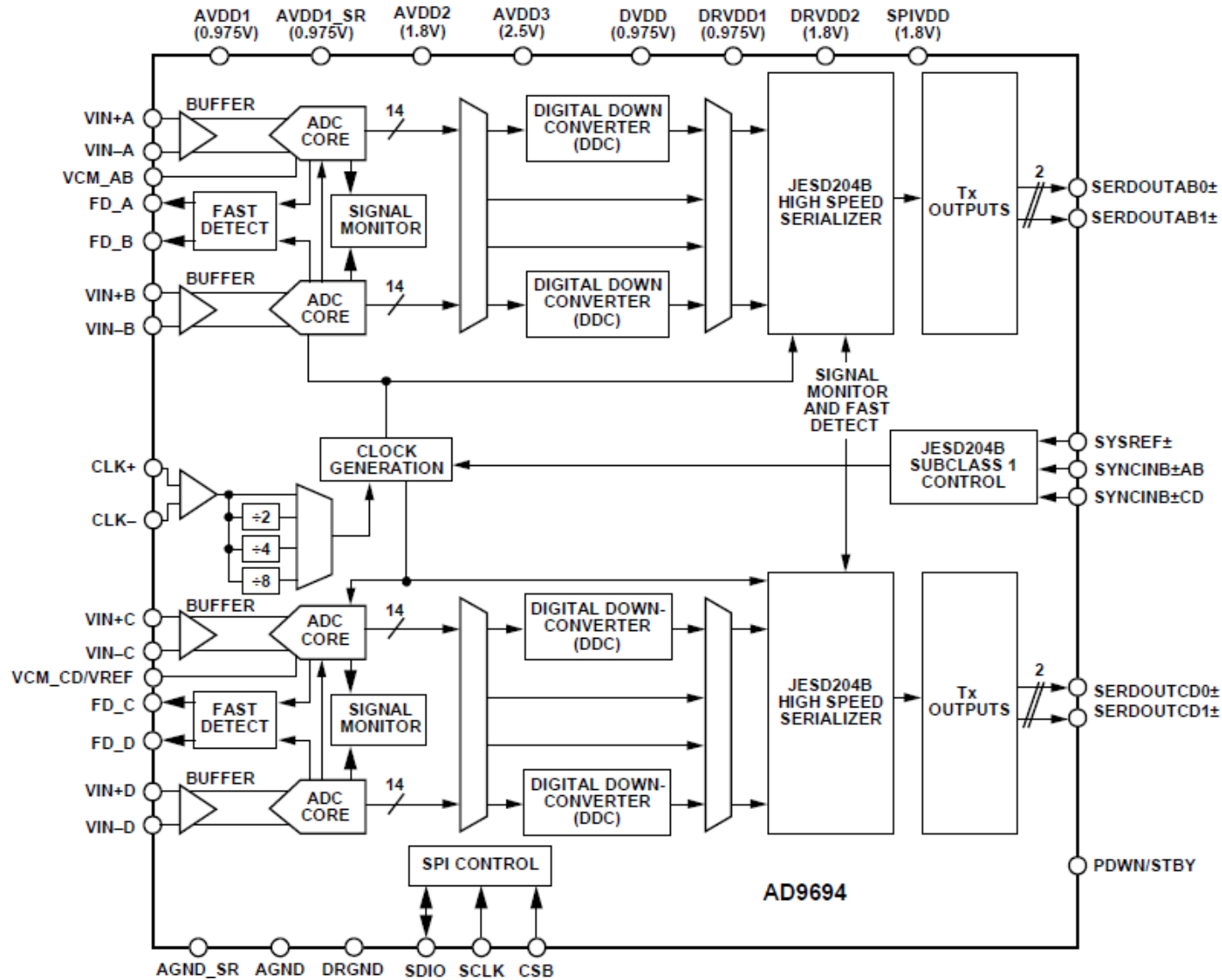
- JESD204B (Subclass 1) coded serial digital outputs
  - Lane rates up to 15 Gbps
- 1.66 W total power at 500 MSPS
  - 415 mW per ADC channel
- SFDR = 82 dBFS at 305 MHz (1.80 V p-p input range)
- SNR = 66.8 dBFS at 305 MHz (1.80 V p-p input range)
- Noise density = -151.5 dBFS/Hz (1.80 V p-p input range)
- 0.975 V, 1.8 V, and 2.5 V dc supply operation
- No missing codes
- Internal ADC voltage reference
- Analog input buffer
- On-chip dithering to improve small signal linearity
- Flexible differential input range
  - 1.44 V p-p to 2.16 V p-p (1.80 V p-p nominal)
- 1.4 GHz analog input full power bandwidth

- Amplitude detect bits for efficient AGC implementation
- 4 integrated wideband digital processors
  - 48-bit NCO, up to 4 cascaded half-band filters
- Differential clock input
- Integer clock divide by 1, 2, 4, or 8
- On-chip temperature diode
- Flexible JESD204B lane configurations

### APPLICATIONS

- Communications
  - Diversity multiband, multimode digital receivers
    - 3G/4G, W-CDMA, GSM, LTE, LTE-A
  - General-purpose software radios
  - Ultrawideband satellite receivers
- Instrumentation
- Radars
- Signals intelligence (SIGINT)

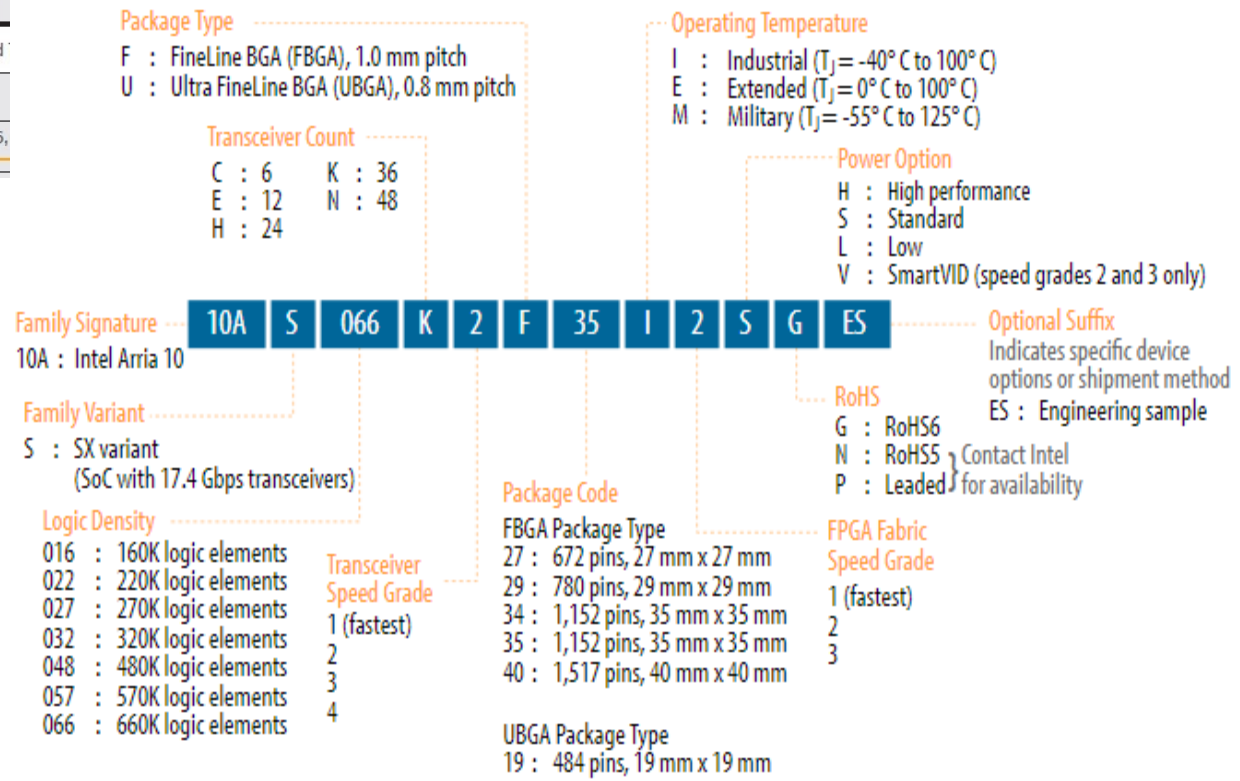
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PRODUCT LINE		GX 160 SX 160	GX 220 SX 220	GX 270 SX 270	GX 320 SX 320	GX 480 SX 480	GX 570 SX 570	GX 660 SX 660	GX 900	GX 1150	GT 900	GT 1150
Resources	LEs (K)	160	220	270	320	480	570	660	900	1,150	900	1,150
	System logic elements (K)	210	288	354	419	629	747	865	1,180	1,506	1,180	1,506
	Adaptive logic modules (ALMs)	61,510	83,730	101,620	118,730	181,790	217,080	250,540	339,620	427,200	339,620	427,200
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160	1,358,480	1,708,800	1,358,480	1,708,800
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133	2,423	2,713	2,423	2,713
	M20K memory (Mb)	9	11	15	17	28	35	42	47	53	47	53
	MLAB memory (Mb)	1.0	1.8	2.4	2.8	4.3	5.0	5.7	9.2	12.7	9.2	12.7
	Hardened single-precision floating-point multipliers/adders	156/156	191/191	830/830	985/985	1,368/1,368	1,523/1,523	1,688/1,688	1,518/1,518	1,518/1,518	1,518/1,518	1,518/1,518
	18 x 19 multipliers	312	382	1,660	1,970	2,736	3,046	3,376	3,036	3,036	3,036	3,036
	Peak fixed-point performance (GMACS) <sup>1</sup>	343	420	1,826	2,167	3,010	3,351	3,714	3,340	3,340	3,340	3,340
Peak floating-point performance (GFLOPS)	140	172	747	887	1,231	1,371	1,519	1,366	1,366	1,366	1,366	
Clocks, Maximum I/O Pins, and Architectural Features	Global clock networks	32	32	32	32	32	32	32	32	32	32	32
	Regional clocks	8	8	8	8	8	8	16	16	16	16	16
	Hard processor system (available in SX devices only)	Dual-core Arm® Cortex®-A9 MPCore® processor. See the following page for details.										
	Maximum LVDS channels (1.6 G)	120	120	168	168	222	324	270	384	384	312	312
	Maximum user I/O pins	288	288	384	384	492	696	696	768	768	624	624
	Transceiver count (17.4 Gbps)	12	12	24								
	Transceiver count (25.78 Gbps)	-	-	-								
	PCIe® hardened IP blocks (Gen3 x8) <sup>2</sup>	1	1	2								
Maximum 3 V I/O pins	48	48	48									
Package Options <sup>3</sup> and I/O Pins <sup>4</sup> : General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs <sup>5</sup> , and												
U19	U484 pin (19 mm)	192, 48, 72, 6	192, 48, 72, 6	-								
F27	F672 pin (27 mm)	240, 48, 96, 12	240, 48, 96, 12	240, 48, 96,								

Figure 3. Sample Ordering Code and Available Options for Intel® Arria® 10 SX Devices

**Only version SX has integrated processor (HPS):**  
 Example (less expensive device):  
 10AS016E4F27E3SG = US\$469 (mouser.com 09/07/20)  
 SX 160, 160k Les, 12 transceivers, FBGA package, 673 pins,  
 With Transceiver Speed Grade 4, a rate up to 11,3 Gbps,  
 enough for interfacing the AD9694 ADC (10 Gbps).



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## PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

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**32-bit MCUs (up to 2 MB Live-Update Flash and 512 KB SRAM) with FPU,  
Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog**

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### Operating Conditions

- 2.1V to 3.6V, -40°C to +85°C, DC to 252 MHz
- 2.1V to 3.6V, -40°C to +125°C, DC to 180 MHz

### Core: 252 MHz (up to 415 DMIPS) M-Class

- 16 KB I-Cache, 4 KB D-Cache
- FPU for 32-bit and 64-bit floating point math
- MMU for optimum embedded OS execution
- microMIPS™ mode for up to 35% smaller code size
- DSP-enhanced core:
  - Four 64-bit accumulators
  - Single-cycle MAC, saturating, and fractional math
  - IEEE 754-compliant
- Code-efficient (C and Assembly) architecture

### Clock Management

- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timers (WDT) and Deadman Timer (DMT)
- Fast wake-up and start-up

### Power Management

### Advanced Analog Features

- 12-bit ADC module:
  - 18 Msps with up to six Sample and Hold (S&H) circuits (five dedicated and one shared)
  - Up to 48 analog inputs
  - Can operate during Sleep and Idle modes
  - Multiple trigger sources
  - Six Digital Comparators and six Digital Filters
- Two comparators with 32 programmable voltage references
- Temperature sensor with  $\pm 2^\circ\text{C}$  accuracy

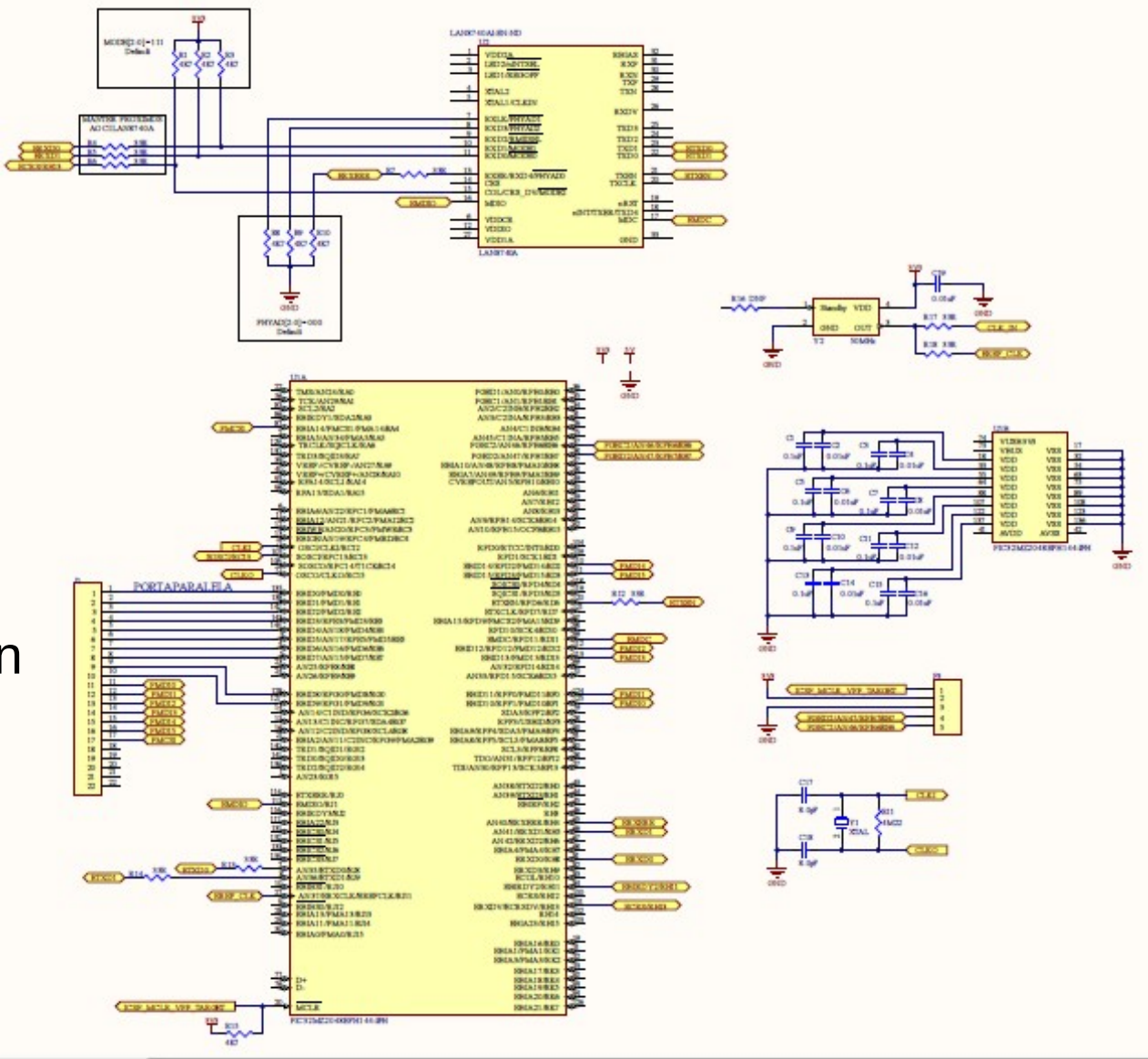
### Communication Interfaces

- Two CAN modules (with dedicated DMA channels):
  - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (25 Mbps):
  - Supports up to LIN 2.1 and IrDA® protocols
- Six 4-wire SPI modules (up to 50 MHz)
- SQI configurable as an additional SPI module (50 MHz)
- Five I<sup>2</sup>C modules (up to 1 Mbaud) with SMBus support
- Parallel Master Port (PMP)
- Peripheral Pin Select (PPS) to enable function remap

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Microcontroller schematics already under development

- Useful features:
- Ethernet port
  - USB port
  - FPGA registers configuration



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COMPARATIVO - FRAME GRABBER'S

Fabricante	Modelo	Nº de canais	Processamento Compatível	Procedência	Custo aproximado	Custo por canal	Link do FG	Datasheet
Sensoray	Model 817	16	Aguardando informação	Importado	Aguardando cotação	Aguardando cotação	<a href="http://www.sensoray.com/products/817.htm">http://www.sensoray.com/products/817.htm</a>	<a href="http://www.sensoray.com/download">http://www.sensoray.com/download</a>
Sensoray	Model 812	8	Aguardando informação	Importado	US\$227,00	US\$28,38	<a href="http://www.sensoray.com/products/812.htm">http://www.sensoray.com/products/812.htm</a>	<a href="http://www.sensoray.com/download">http://www.sensoray.com/download</a>
Active Silicon	Firebird 4XCXP12-3PE8	4	Sim (FPGA)/GPU Direct	Importado	Aguardando cotação	Aguardando cotação	<a href="https://www.activesilicon.com/products/firebird-4xcxp12-3pe8">https://www.activesilicon.com/products/firebird-</a>	<a href="https://www.activesilicon.com/wp">https://www.activesilicon.com/wp</a>
Kaya Instruments	KY-FGK-801	8	Sim (FPGA)	Importado	US\$1.650,00	US\$206,25	<a href="https://kayainstruments.com/komodo-8-channel">https://kayainstruments.com/komodo-8-channel</a>	<a href="https://storage.kayainstruments.c">https://storage.kayainstruments.c</a>
Euresys	Coaxlink Octo	8	Sim (GPU)	Importado	US\$2.599,00	US\$324,88	<a href="https://www.euresys.com/en/Products/Frame-Grabbers/Coaxlink-Octo">https://www.euresys.com/en/Products/Frame-Gr</a>	<a href="http://downloads.euresys.com/Do">http://downloads.euresys.com/Do</a>