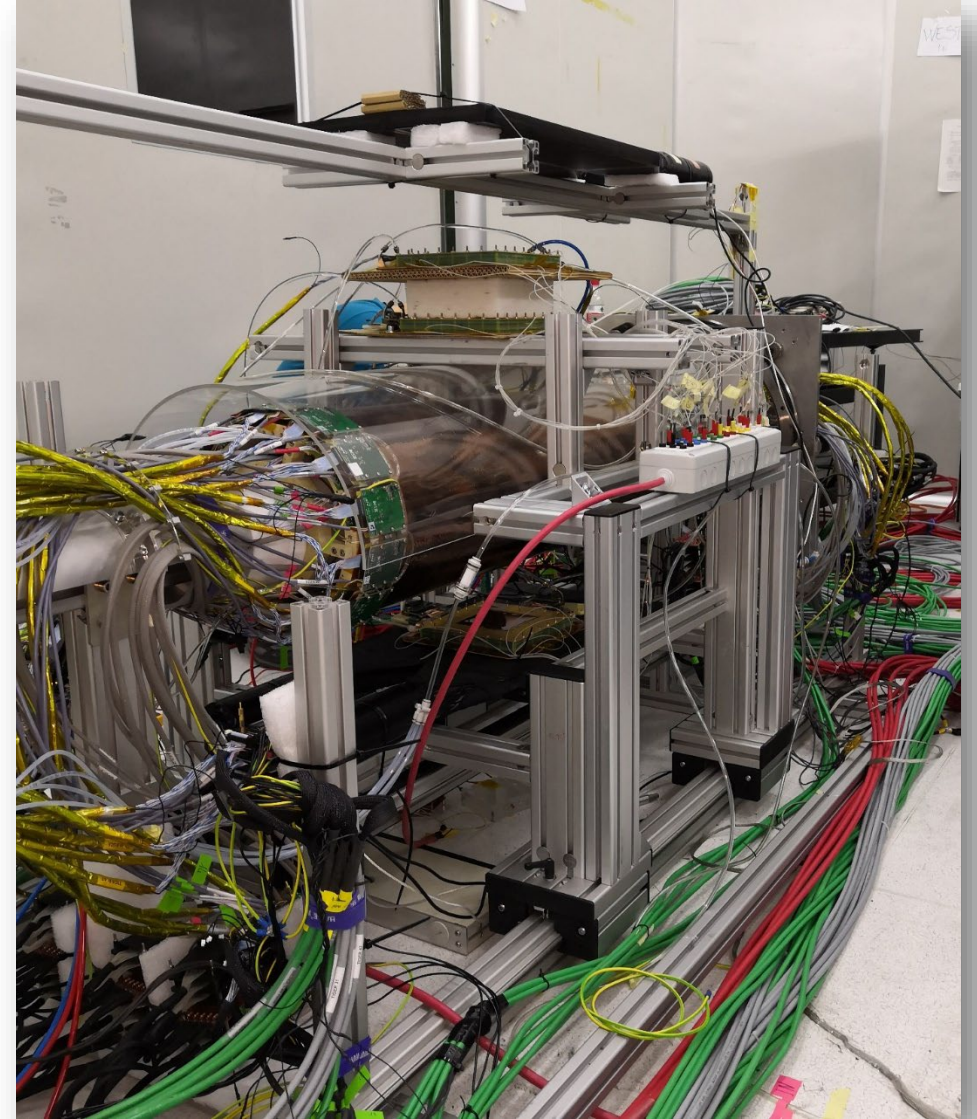


Integration: status and plans

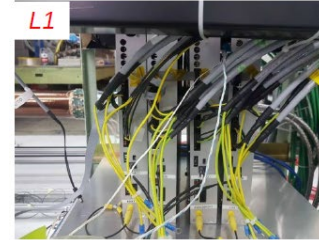
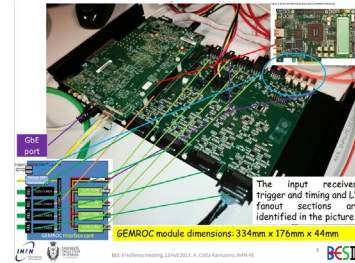
Michela Greco-INFN TORINO& UNITO



Off detector electronics>update and plans

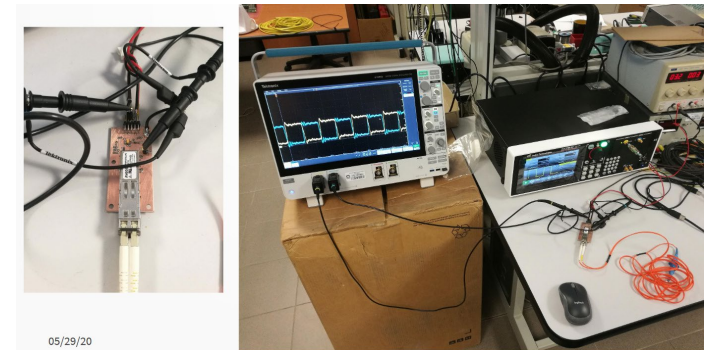
spare GEMROC_IFC cards

- ✓ Arrived and successfully tested
- ✓ Clk buffer modules mounted



FCS Fanout Board

- ✓ Order for Layout and board production placed in Dec 2019
- ✓ prototyping and testing of XCVR modules in progress
- ✓ final schematic for modular construction in progress

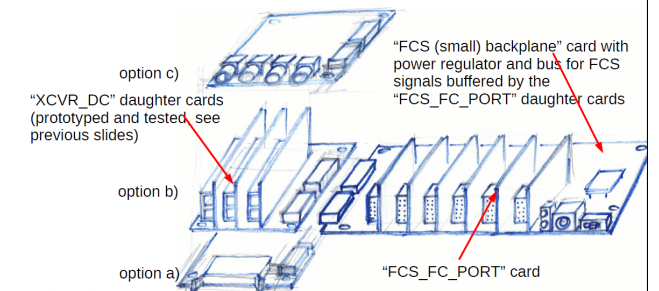


FCLS Fanout Boards

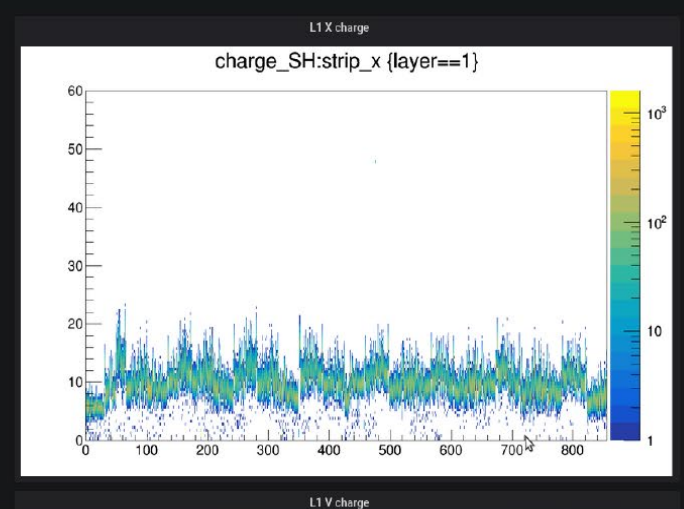
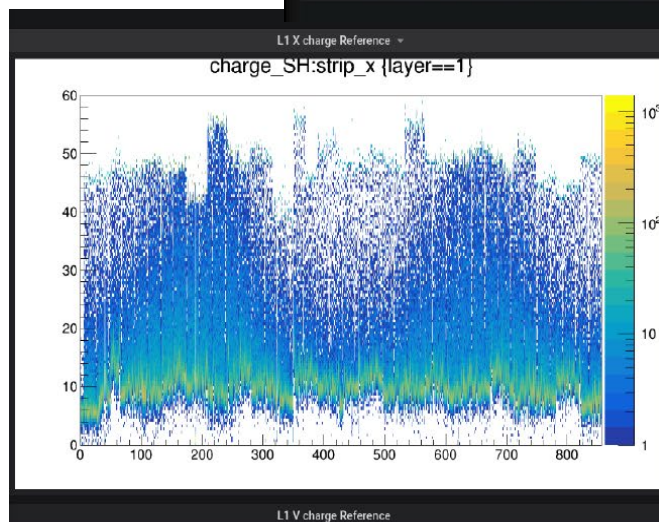
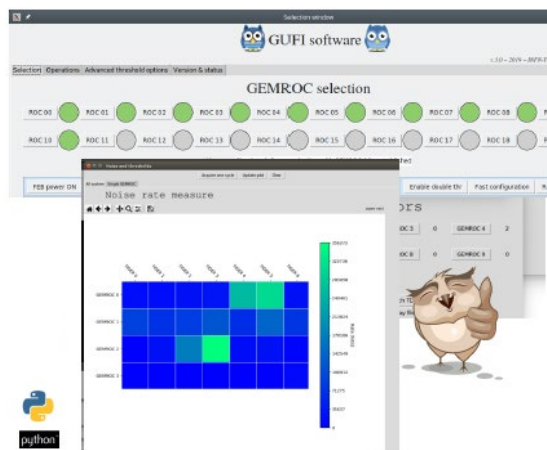
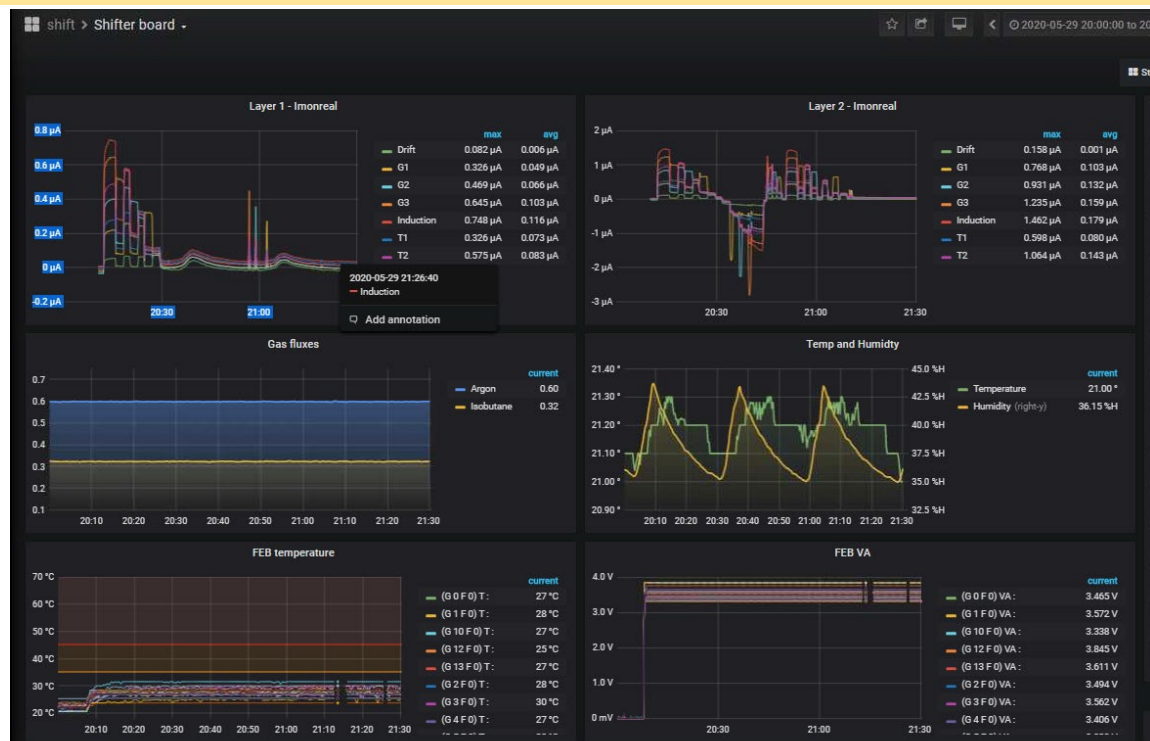
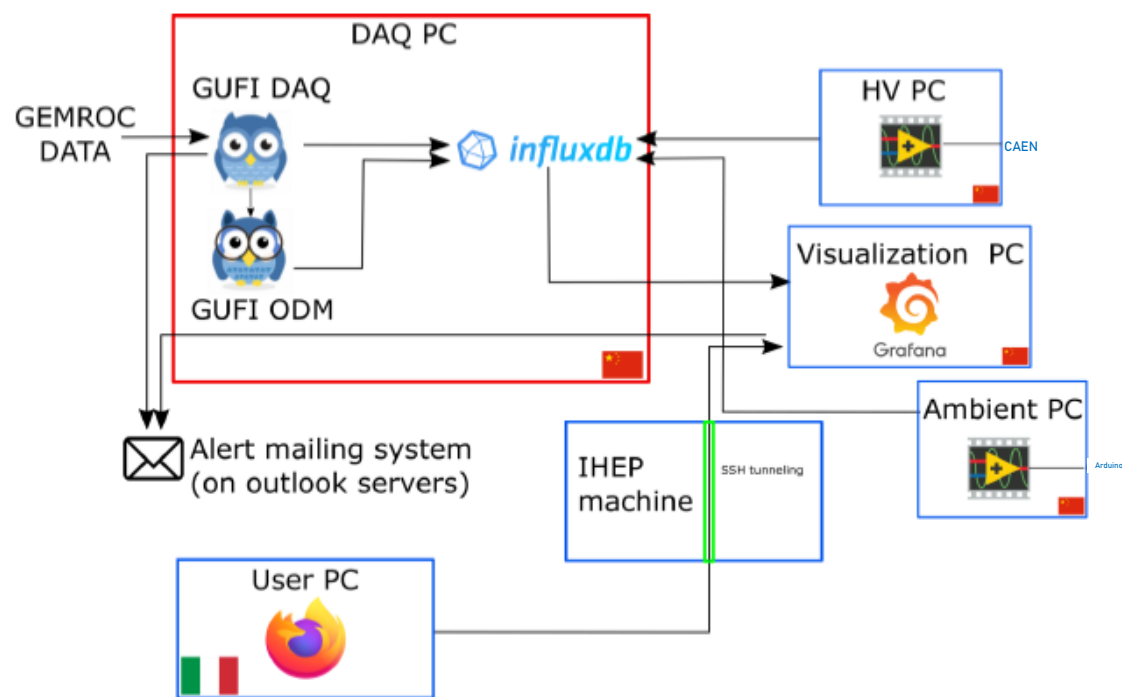
- ✓ Schematic diagram and Local Fanout board layout v1.0
 - ✓ New version 2.0, modular, in progress
- (cheaper to build; modules can be used to build the System Fanout as well)

A.Cotta Ramusino INFN-FE

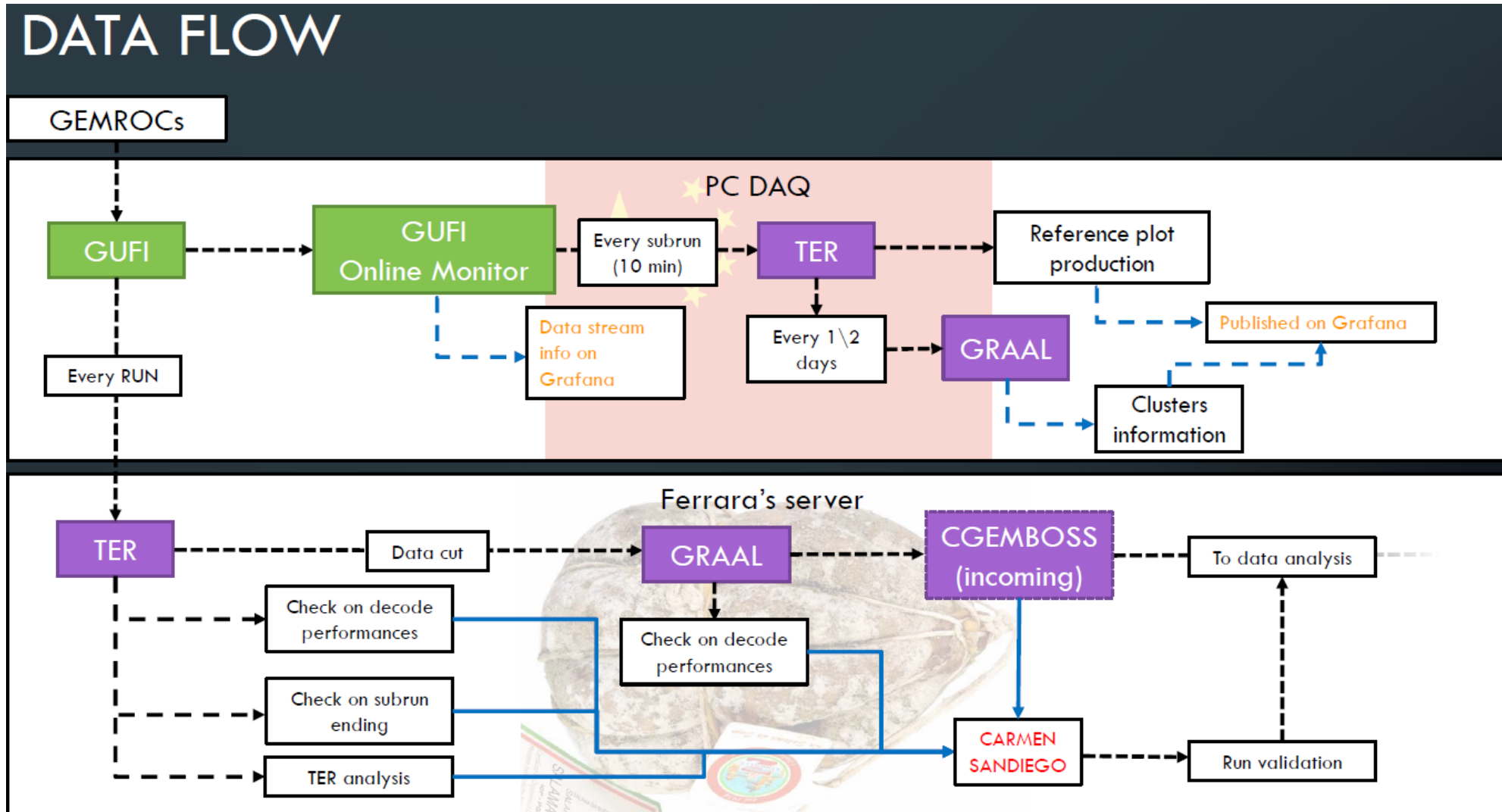
- The **MODULAR** FCLF will have:
- option a) 1 LVDS receiver port for the FCS signals from the BES-III Fast Control System Fanout (FCF)
 - option b) optical duplex ports for FCS signals (DC to 50MHz) ("XCVR_DC" daughter cards)
 - option c) LEMO ports for LVCMOS single ended FCS signals (for stand alone test setup)
 - 6 output ports ("FCS_FC_PORT") for point to point connection to the GEMROC



Integration Status> DAQ+online monitoring



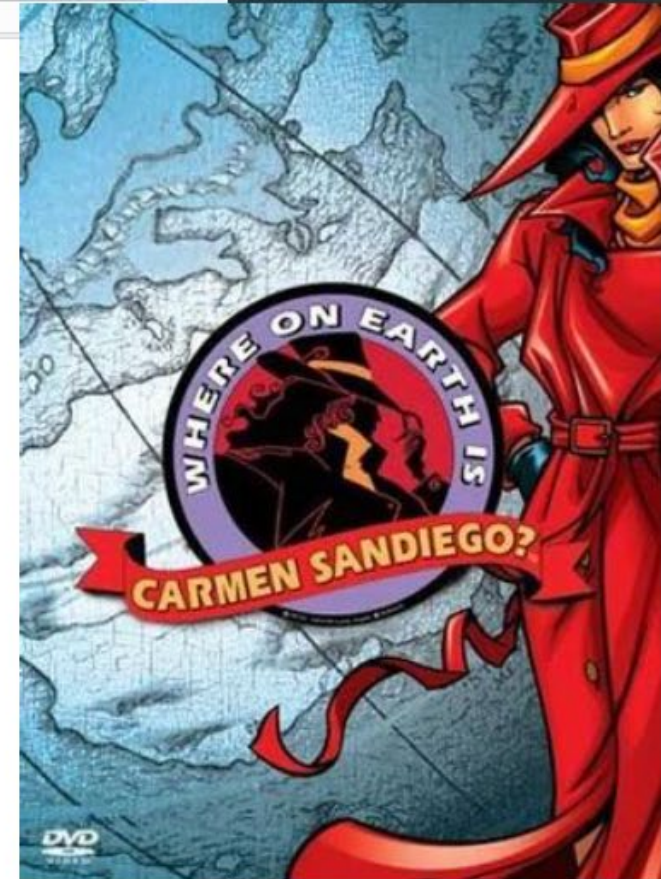
Integration Status> offline monitoring



Integration Status> offline monitoring

Index of /u/rfarinelli/.carmensandiego

Name	Last modified	Size	Description
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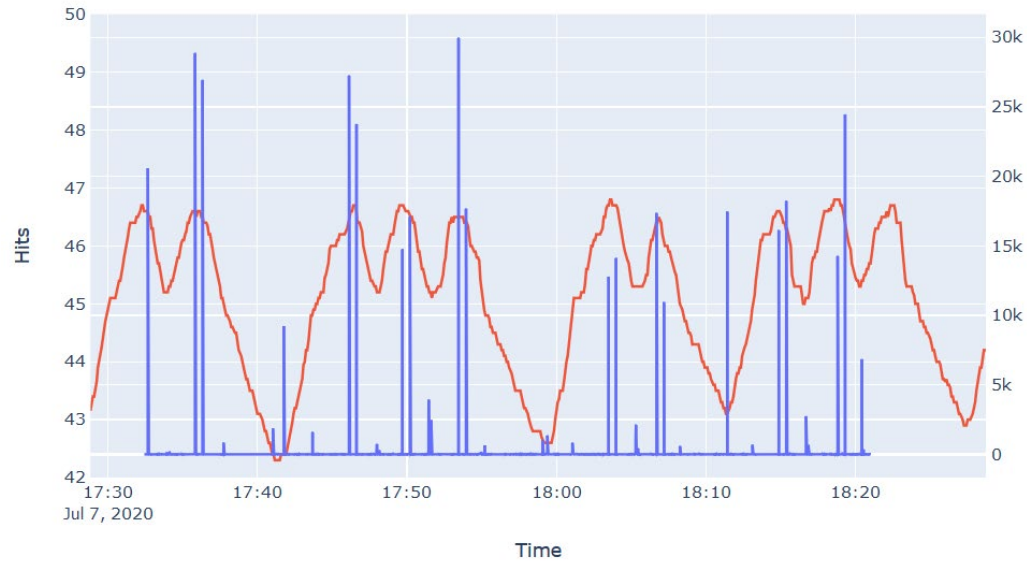


On going investigations>

Gas quality

Ambient EMI

Clean room cycles

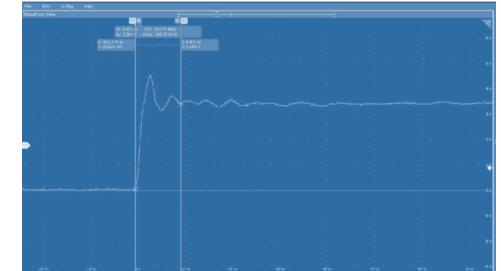
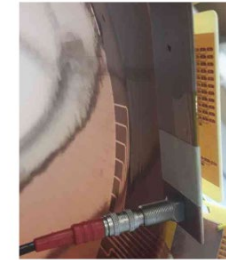
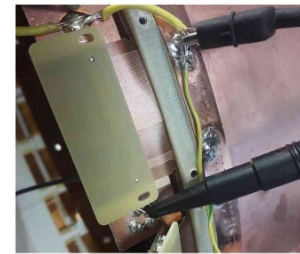


Trigger system

External
Internal

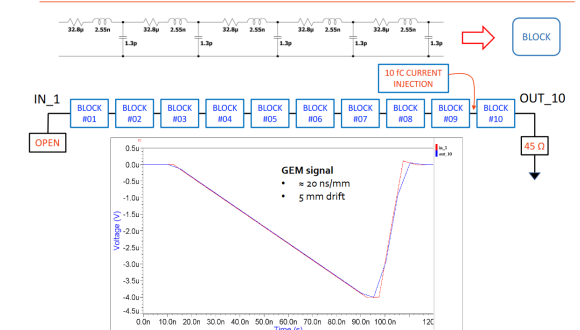
Signal propagation speed

Measurements



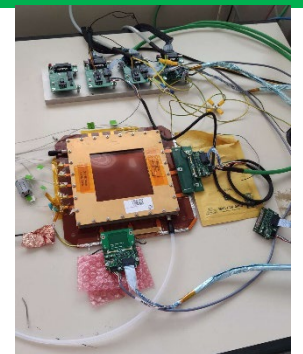
Simulation: V Microstrip Model

Strip simulation

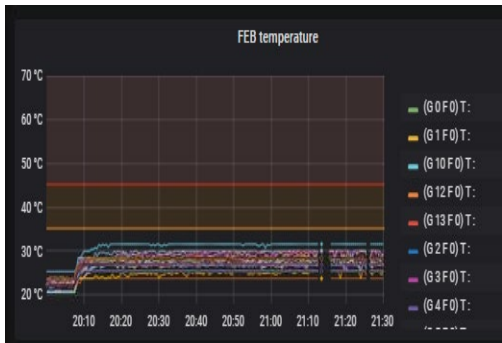
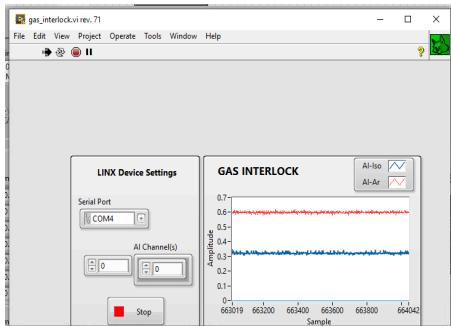
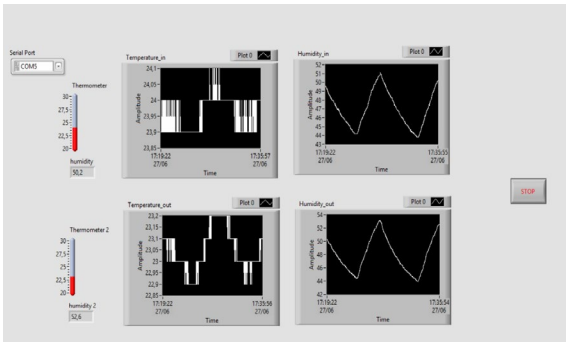
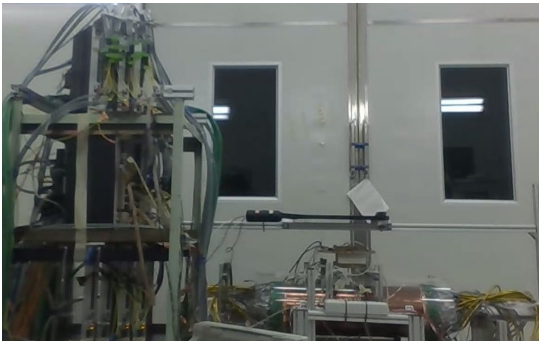


Noise studies.

1 planar chamber with 2 TIGER
+1 TIGER



Integration Plans > short term



HARDWARE INTERLOCK SYSTEM		
system	status	action
gas	failure	inhibit HV
cooling	failure	inhibit HV/LV
power	failure	inhibit HV/LV
slow control	failure	inhibit HV/LV
interlock	failure	inhibit HV/LV

PLC
+ARDUINO



Improving SW interlock System

Integration Plans > 2021

GENNAIO-MARZO	Maintenance L1+L2 Accensione L3
MARZO-APRILE	Rimozione struttura temporanea di sostegno Miglioramento setup per run cosmici
APRILE-GIUGNO GIUGNO-AGOSTO	Setup L1+L2+L3 in operazione Commissioning
AGOSTO-DICEMBRE	Run cosmici test BESIII-SC/DAQ per CGEM-IT



Milestones> 2020

30-04-0020

CGEM ELETTRONICA:
integrazione elettronica CGEM con DAQ di BESIII

Attività ritardata fortemente da covid19

Completamento: 30%

Si era posposta questa attività alla review di febbraio, ma a gennaio è subentrato il lockdown.

Sono stati fatti test di base ma per aumentare la complessità servirebbe integrare altre feb/gemroc (ad esempio oL1) quindi necessità di interagire in loco.

Fermi anche i test con i Data Concentrator che erano stati riportati ad Uppsala per migliorie hw/fw.

30-06-0020

CGEM ELETTRONICA:
montaggio sistema finale di cooling

Attività ritardata fortemente da covid19

Completamento: 50%

Numero dissipatori finali L1: 16/16; L2: 4/28 e L3: 20/36.