FaLaPHEL

Fast Links and RadHard Front End with Integrated Photonics and Electronics for Physics

Call aperta

Area di ricerca: Elettronica

Resp. Naz: F. Palla
Resp. Loc.: L. Gaioni

INFN Pavia, CDS, 14 luglio 2020

FaLaPHEL in a nutshell

- **Goal of the project**

  - Improve the state of the art of high speed data links and mixed-signal readout circuits for future high rate pixel detector applications, and study the integration of these data links and of analog/digital front-end blocks in a prototype readout circuit.

  - The project targets the tracker of the FCC-hh experiments with the opportunity to replace the inner pixel systems of the HL-LHC experiments in about 2032

- **INFN Units:** Padova, Pavia, Pisa

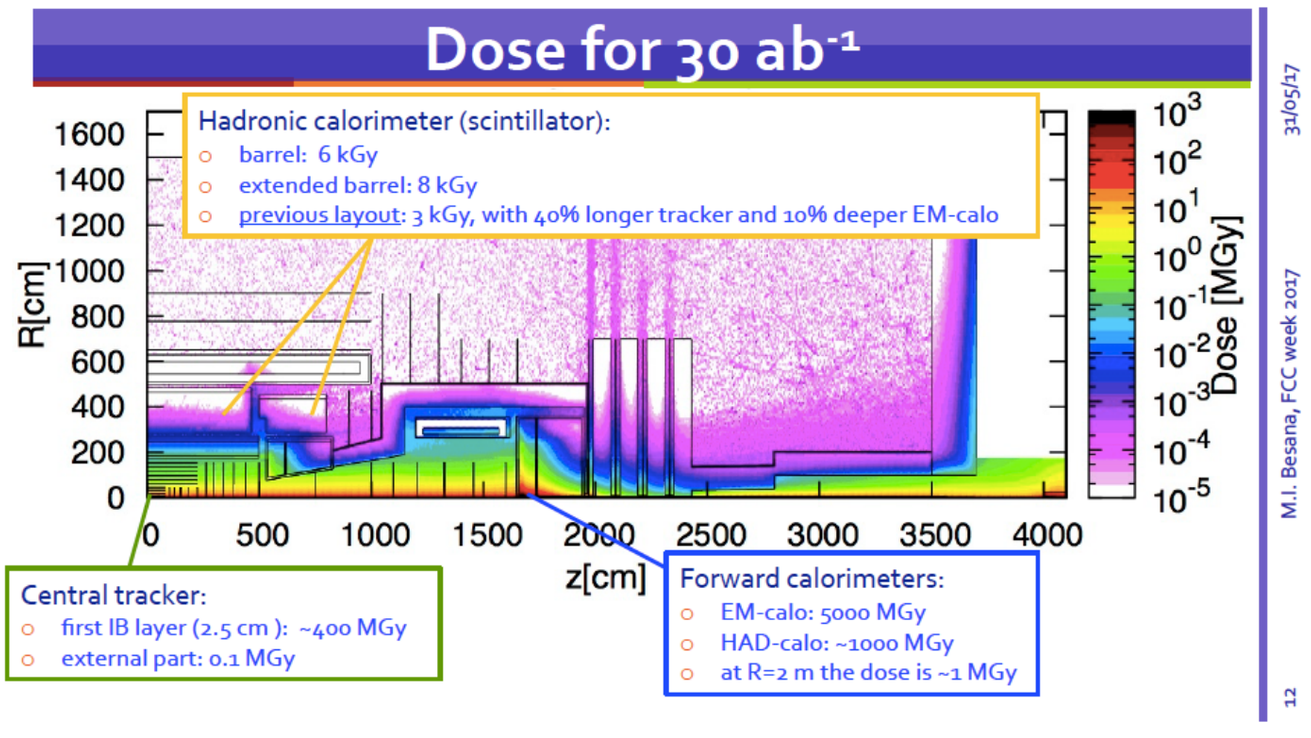
- **External Units:** Scuola Superiore S. Anna di Pisa, Dip. Ingegneria Informazione UniPisa, Dip. Fisica UniMilano

- **Duration**: 3 years

Next generation HEP detectors

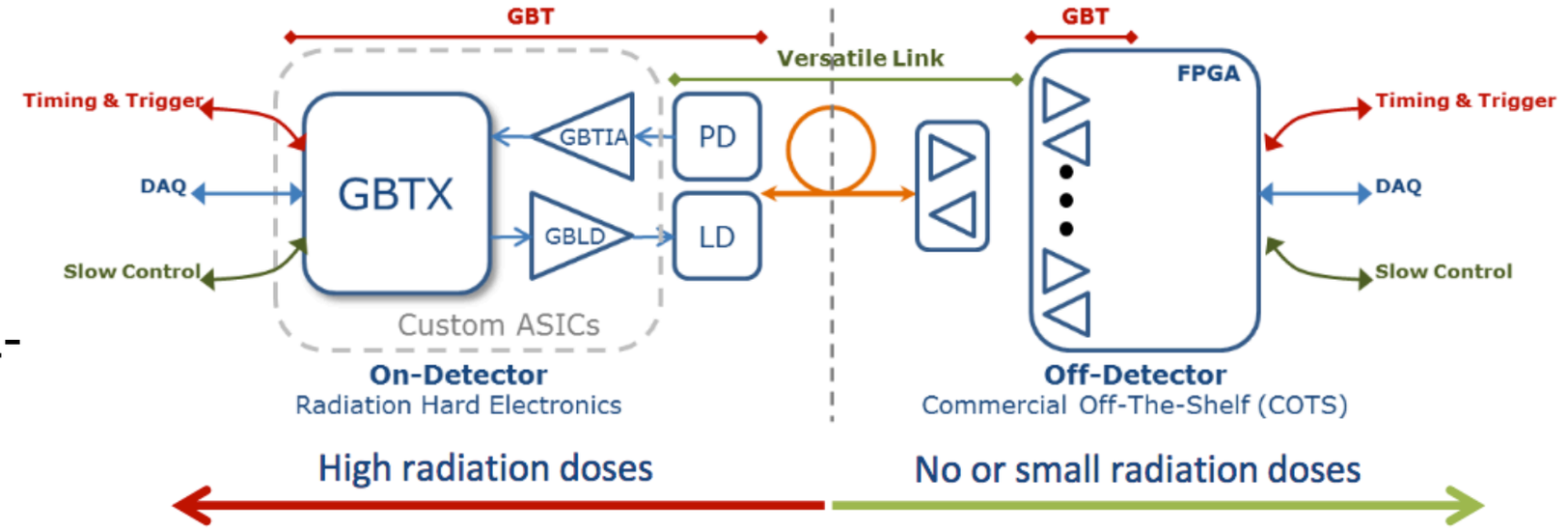
- **High-Luminosity LHC**
  - Increase of radiation levels
    - up to 6 MGy TID
    - up to $5x10^{16}$ n_{eq}/cm^2
  - Large data rates
    - Aggregate of 60 Tb/s

- **FCC-hh**
  - 0.5- 50 x 10^{16} n_{eq}/cm^2
  - 0.1 to 400 MGy
  - Huge data rates
    - ~6000 Tb/s outer tracker (untriggered)
    - 150 Tb/s (triggered @ 1 MHz)
    - pixel module 10 Gb/s/cm^2 (triggered @ 1 MHz)



State of the Art

- **LpGBT and Versatile Link** +
  - Based on 65 nm technology and VCSEL
  - Total dose 2 MGy
  - Total fluence 10^{15} n/cm^2
    - cannot be used at HL-LHC below ~20 cm radius
      - implies RD53 chips needs e-links to LpGBT (~1 meter away)



P. Moreira, The LpGBT ProjectStatus and Overview

- **Silicon Photonics** demonstrated to be sufficiently rad-hard (>10^{16} n/cm^2 and tested up to 300 Mrad)

- **PHOS4BRAIN (CSN5)** project showed 65 nm driver to to be rad-hard up to 8 MGy and reach ~5 Gb/s, limited by packaging (Aluminum wire bonds)

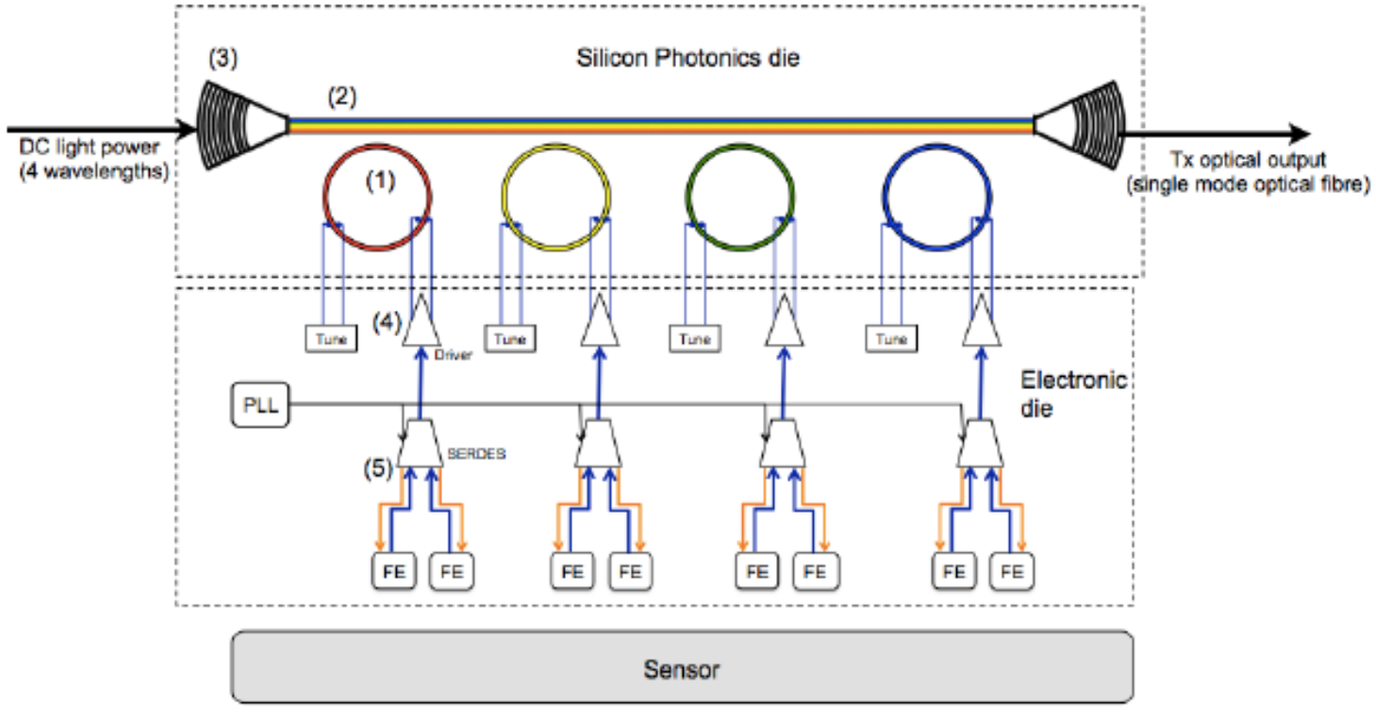
Goals of FaLaPHEL

- **Hybrid (3D or 2.5D) integration** of Silicon Photonics modulators with high speed radiation hard (**≥10 MGy**) electronics in 28 nm
- **Aggregated 100 Gb/s links** using wavelength division multiplexing (4 wavelength on a single optical fibre) and Integrated Front-End electronics

Table 1: Technology benchmarks and envisioned performance improvement with FALAPHEL

	State of the art – VCSEL+	**This project (FALAPHEL)**
Data rate	10 Gb/s	≥100 Gb/s
Radiation TID	200 Mrad (2 MGy)	≥1 Grad (10 MGy)
Total Fluence	10^{15}n/cm^2	>5 x 10^{16}n/cm^2

- Design and fabrication of a **demonstrator**



Challenges - I

- **ASIC: CMOS 28 nm wrt 65 nm**
  - Allows to reach higher modulation speed at similar power consumption
  - Similar or better radiation tolerance
  - Parasitic effects may have more significant impact
    - requires optimisation and study of bonding pads and interconnects (**Synergy with AIDAInnova**)

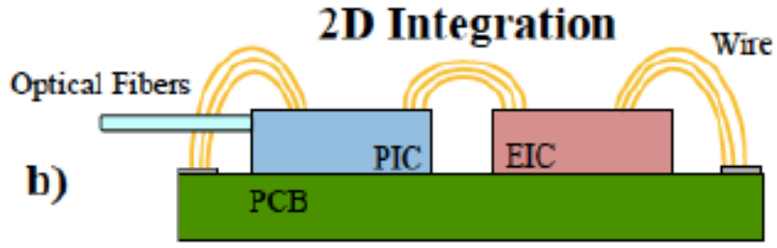
- **28nm Front-End**
  - Expected very low thresholds at lower power (to be verified experimentally)

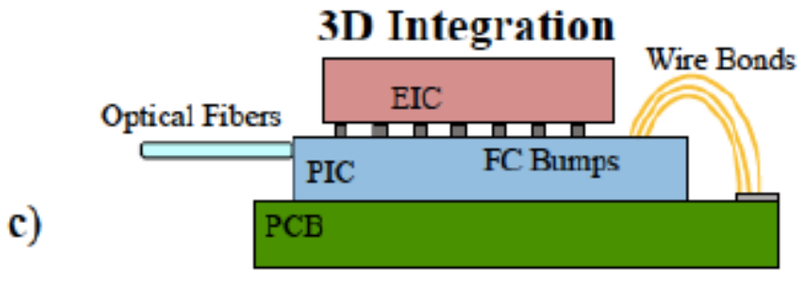
- **Photonics**: Ring vs Mach-Zehnder Modulators
  - RMs have smaller driving voltage than MZM (~1V vs 2V)
  - RMs can be tuned for different wavelengths allowing WDM
    - single optical fibre
  - RMs are more sensitive to temperature variations
    - need tune circuits

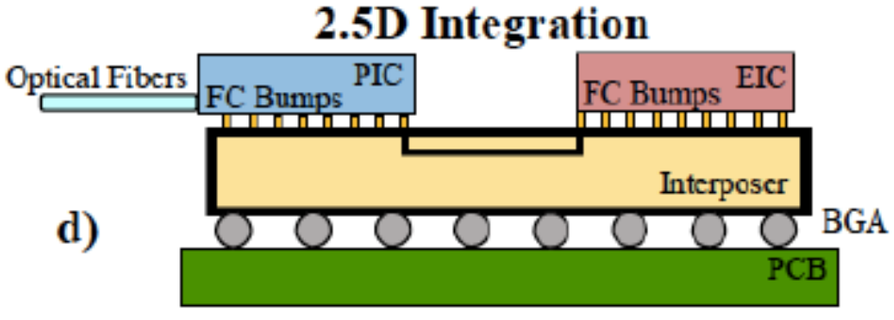
Challenges - II

- **Hybrid assembly of two chips**

  - **Parasitics:** 3D (flip chip) < 2.5D (interposer) < 2D (wire bonds)
  - Need careful **thermal management** (Synergy with AIDAInnova)
  - Interest to use DIAM (Development & Innovations on Additive Manufacturing) expertise (**INFN Padova**) on producing metallic additive manufacturing structures for heat removal



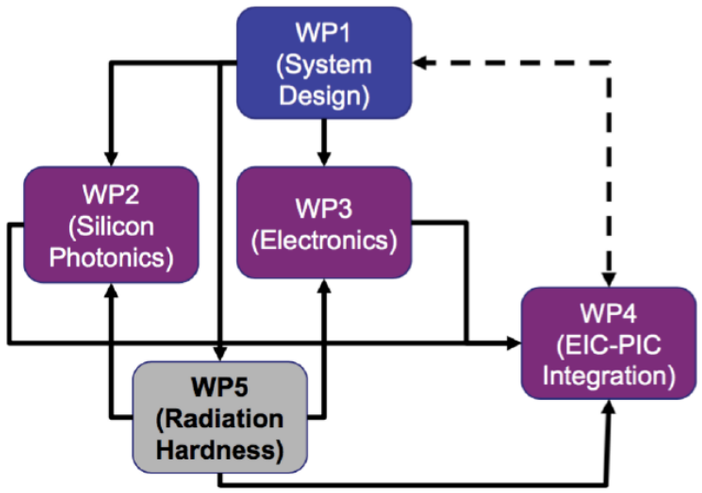




WP Structure

Table 3. Work Packages.

WP	Topic	Leader	Unit	Areas of work
1	System Design	Luigi Gaioni	INFN Pavia	Demonstrator design, system specifications and key performance indicators
2	Silicon Photonics	Stefano Faralli	Scuola Superiore S. Anna of Pisa	PIC blocks, Ring-Resonator Modulator, MachZehnder Modulator, WDM and SDM
3	Electronics	Gianluca Traversi (focus FE) and Guido Magazzu (focus IP cores)	INFN Pavia INFN Pisa	Serdes, Driver, PLL/CDR, DAC, Bandgap, Front-End
4	EIC-PIC Integration	Sergio Saponara	University of Pisa	Packaging and integration, thermal studies, prototyping and fabrication
5	Radiation hardness	Serena Mattiazzo	INFN Padova	Tests with X-rays, Heavy Ions, protons, neutrons
6	Project management and dissemination	Fabrizio Palla	INFN Pisa	Resource management, planning and coordination. Dissemination and exploitation of the results



Commitments for Pavia

- **WP1 (System Design)** defines the system specifications and key performance indicators (KPI) as inputs to WP 2 to 5 to outperform state of the art and benchmarking. Designs the final demonstrator together with WP4.
  - Who: L. Gaioni, V. Re, AdR#5
  - D1.1 System specifications and KPI
  - D1.2 Demonstrator design

- **WP3 (Electronics)** design of the fundamental rad-hard and high-speed electronics and test boards
  - Who: L. Ratti, G. Traversi, AdR#4, AdR#5
  - D3.2/3.2b Drivers and Tune circuit
  - D3.4/3.4b Front-End circuits
  - D3.5/3.5b DAC/Bandgap
  - D3.6 Final large area EIC submission

- **WP5 (Radiation Hardness)** will be in charge of the irradiation and radiation tolerance characterization of the EIC and PIC, and that of the integrated demonstrator
  - Who: E. Riceputi

Participants per research unit

Table 5. List of participant Units with their leaders, FTE/year, number of members and designers (MEC: Mechanical; ELE: Electronic; PHO: Silicon Photonics).

Research Unit	Leader	FTE/year	Members	Designers
INFN Pisa	Fabrizio Palla	1.9 + 3 (AdR)	8 + 3 (AdR)	ELE: 3 + 2 (AdR) PHO:1 (AdR) MEC: 2
INFN Pavia	Luigi Gaioni	1.6 + 2 (AdR)	5 + 2 (AdR)	ELE: 5 + 2 (AdR)
INFN Padova	Serena Mattiazzo	1.55 + 1 (AdR)	7 + 1 (AdR)	ELE: 7 + 1 (AdR)
University of Pisa	Sergio Saponara	1.05	3	ELE: 2 ELE/PHO: 1
SSSA	Stefano Faralli	0.80	3	PHO: 3
University of Milan	Valentino Liberali	0.15	3	ELE: 2 PHO: 1

Participant list - Pavia

Name	Role	Unit	WP1	WP2	WP3	WP4	WP5	Total
L. Gaioni	ELE	INFN PV	40					40
L. Ratti	ELE	INFN PV			30			30
V. Re	ELE	INFN PV	10					10
E. Riceputi	ELE	INFN PV					50	50
G. Traversi	ELE	INFN PV			30			30
AdR #4	ELE	INFN PV			100			100
AdR #5	ELE	INFN PV		50	50			100

Participant list Others

Name	Role	Unit	WP1	WP2	WP3	WP4	WP5	Total
M. Bagatin	ELE	INFN PD					15	15
A. Candelori	ELE	INFN PD					20	20
S. Gerardin	ELE	INFN PD					15	15
S. Mattiazzo	ELE	INFN PD					20	20
A. Paccagnella	ELE	INFN PD					15	15
M. Teng	ELE	INFN PD					50	50
D. Vogrig	ELE	INFN PD			20			20
AdR #6	ELE	INFN PD					100	100
L. Gaioni	ELE	INFN PV	40					40
L. Ratti	ELE	INFN PV			30			30
V. Re	ELE	INFN PV	10					10
E. Riceputi	ELE	INFN PV					50	50
G. Traversi	ELE	INFN PV			30			30
AdR #4	ELE	INFN PV			100			100
AdR #5	ELE	INFN PV	50		50			100
F. Di Pasquale	PHO	SSSA		10		10		20
S. Faralli	PHO	SSSA	5	20		10		35
P. Velha	PHO	SSSA	5	10		10		25
S. Cammarata	EIC/PHO	Univ. Pisa		20	10	10		40
D. Monda	EIC	Univ. Pisa	10		30	10		50
S. Saponara	EIC	Univ. Pisa			5	10		15
L. Frontini	PHO	Univ. Milan		5				5
V. Liberali	EIC	Univ. Milan			5			5
A. Stabile	EIC	Univ. Milan	5					5
			WP1	**WP2**	**WP3**	**WP4**	**WP5**	**Total**
TOTAL			**185**	**135**	**540**	**145**	**300**	**1305**

Budget

ITEM	WP	Year 1			Year 2			Year 3			TOTAL
		PD	PV	PI	PD	PV	PI	PD	PV	PI	
Travels		**2**	**2**	**2**	**8**	**5**	**5**	**7**	**5**	**5**	**41**
Irradiation and testing	5	0	0	0	6	3	3	6	3	3	24
Work between designers	6	1	1	1	1	1	1	0	1	1	8
General meetings / conferences	6	1	1	1	1	1	1	1	1	1	9
Consumables		**5**	**32**	**89**	**15**	**32**	**119**	**15**	**65**	**25**	**397**
EIC submission	3	0	17	34	0	17	34	0	50	0	152
PIC submission	2	0	0	25	0	0	50	0	0	0	75
Test boards EIC	3	0	5	10	0	5	10	0	5	0	35
Test boards PIC	2	0	0	0	0	0	5	0	0	5	10
X-ray tubes	5	0	0	0	5	0	0	5	0	0	10
Others (cables, fibers, glues, fluids, powder, renting equipment)	1,2,3, 4,5	5	10	20	5	10	20	5	10	20	105
Access to external irradiation facilities	5	0	0	0	5	0	0	5	0	0	10
External services		**0**	**0**	**10**	**0**	**0**	**15**	**0**	**0**	**25**	**50**
Demonstrator design and assembly	4	0	0	10	0	0	15	0	0	25	50
Licenses		**0**	**0**	**8**	**0**	**0**	**1**	**0**	**0**	**1**	**10**
PIC design	2	0	0	8	0	0	1	0	0	1	10
Equipment		**0**	**20**	**35**	**0**	**0**	**0**	**0**	**0**	**0**	**55**
FPGA	3	0	5	10	0	0	0	0	0	0	15
Power supply	3	0	5	0	0	0	0	0	0	0	5
Laser Source (DFB) x2	2	0	0	10	0	0	0	0	0	0	10
Workstations / HD / Screen	2	0	0	5	0	0	0	0	0	0	5
Workstations / HD / Screen	3	0	10	10	0	0	0	0	0	0	20
TOTAL w/o AdR		**7**	**54**	**144**	**23**	**37**	**140**	**22**	**70**	**56**	**553**
Assegni di Ricerca (AdR)		**0**	**60**	**85**	**25**	**60**	**72,5**	**25**	**12,5**	**12,5**	**352,5**
TOTAL		**7**	**114**	**229**	**48**	**97**	**213**	**47**	**83**	**69**	**905,5**

Assegni di Ricerca

Table 6. Requested AdR. Type: Junior (J) / Senior (S)

AdR #	Type	Unit	Months	Research Topic
1	J	PI	30	PIC design and test. PIC-EIC integration and test
2	S	PI	24	Driver design. PIC-EIC integration and test
3	J	PI	18	PLL/CDR design and test
4	J	PV	30	DAC design and test
5	S	PV	24	FE design, test and integration in the demonstrator
6	J	PD	24	Irradiation tests and analysis

INFN Pavia services requests

NONE

Gantt chart

Month		1 Jan	2 Feb	3 Mar	4 Apr	5 May	6 Jun	7 Jul	8 Aug	9 Sep	10 Oct	11 Nov	12 Dec	13 Jan	14 Feb	15 Mar	16 Apr	17 May	18 Jun	19 Jul	20 Aug	21 Sep	22 Oct	23 Nov	24 Dec	25 Jan	26 Feb	27 Mar	28 Apr	29 May	30 Jun	31 Jul	32 Aug	33 Sep	34 Oct	35 Nov	36 Dec
WP1 (System Design)	specibench/ver																																				
	Demonstrators																																				
WP2 (PIC)	PIC mini-block																																				
	PIC full-block																																				
WP3 (EIC)	IP and FE 1st																																				
	IP and FE 2nd																																				
	Final EIC																																				
WP4 (EIC-PIC Integration)	1st demo																																				
	final demo																																				
WP5 (Irradiation)																																					
WP6 (Project management & dissemination)																																					
MILESTONES		M1												M2												M3											
Deliverables		D1.1												D2.1												D3.1/5											

MILESTONES		M4					M5					M6					M7					M8				M9					M10						
Deliverables		D3.1/5	D5.1		D1.2	D2.2						D4.1					D5.1	D3.6				D5.1	D2.3	D4.1						D4.2						
																															D6.2						

Legenda

- Specifications/benchmark/verification
- PIC design & layout
- PIC fabrication
- EIC design & layout
- EIC fabrication
- Integration test
- Integration design
- EIC-PIC Integration
- EIC test
- PIC test
- Irradiation

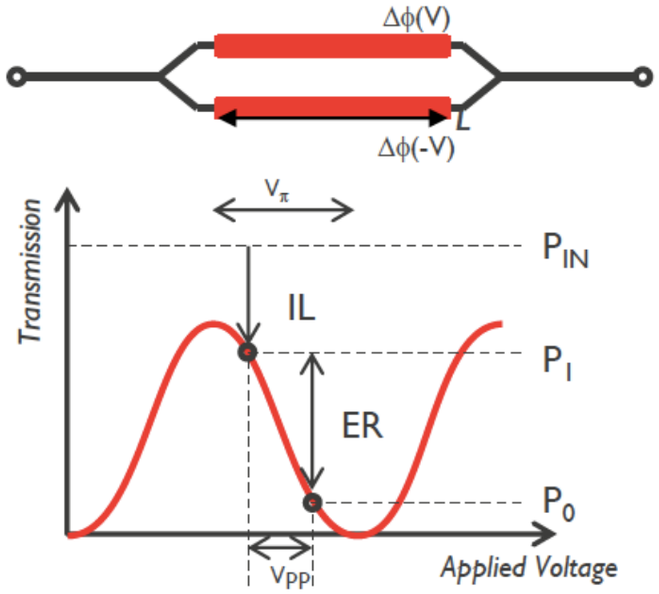
Milestones

M1 (Definitions of the specs and KPI) (T0+2)
M2 (Silicon Photonics PIC design for the submission of the mini-block chip fabrication) (T0+6)
M3 (1st submission of the High Speed rad-hard block design) (T0+10)
M4 (2nd submission of the High Speed rad-hard block design) (T0+16)
M5 (Final Silicon Photonics PIC design for the submission of the full block chip fabrication) (T0+18)
M6 (First integration EIC+PIC) (T0+21)
M7 (Final, large area EIC submission) (T0+25)
M8 (Qualification of rad-hardness of PIC and EIC) (T0+29)
M9 (Final demonstrator integration) (T0+32)
M10 (Final demonstrator qualification) (T0+36)

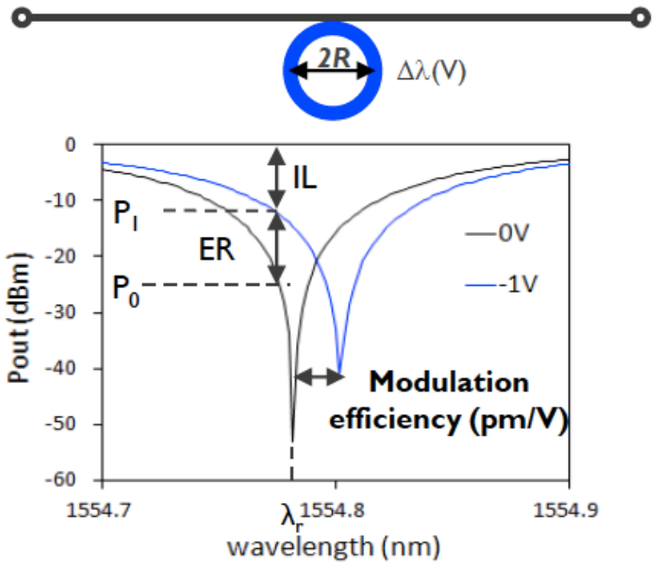
Backup slides

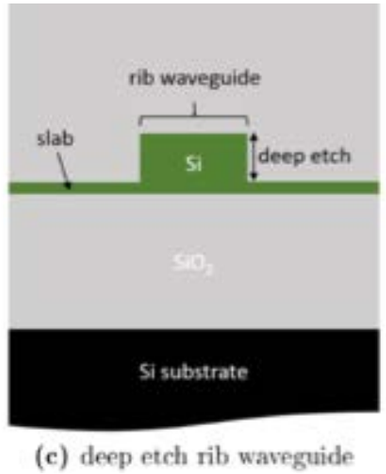
Silicon Photonics Modulators

Si Mach-Zehnder Modulator

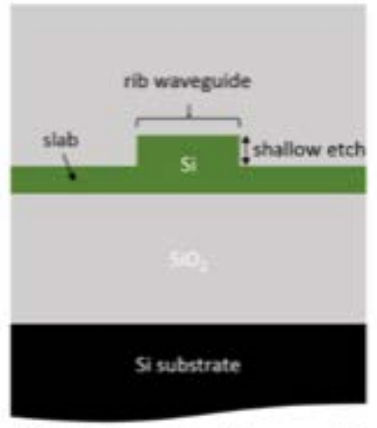


Si Ring Modulator

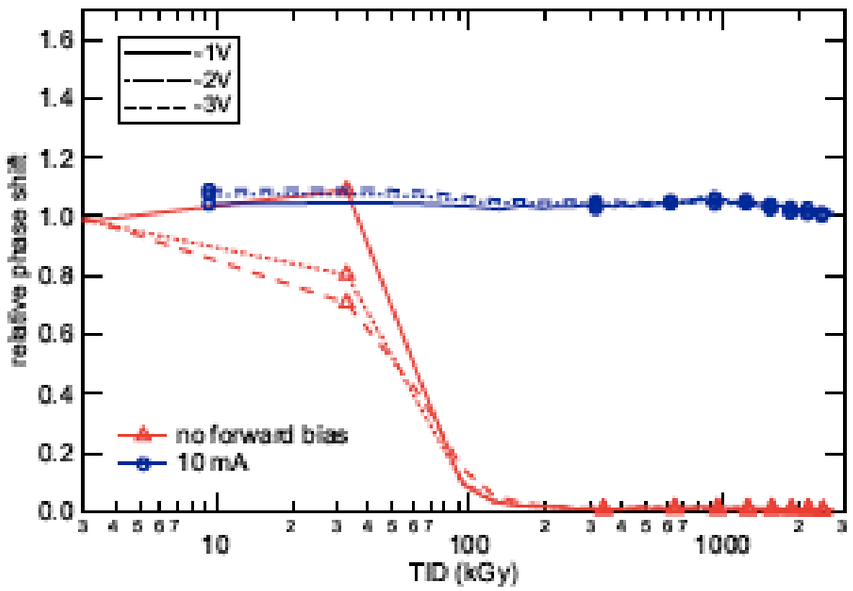




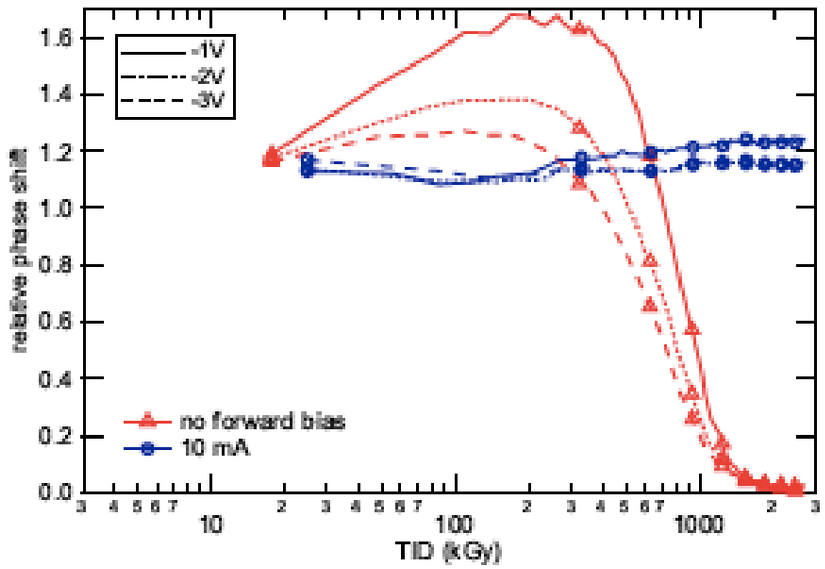
(c) deep etch rib waveguide



(d) shallow etch rib waveguide



(a) deep-etch

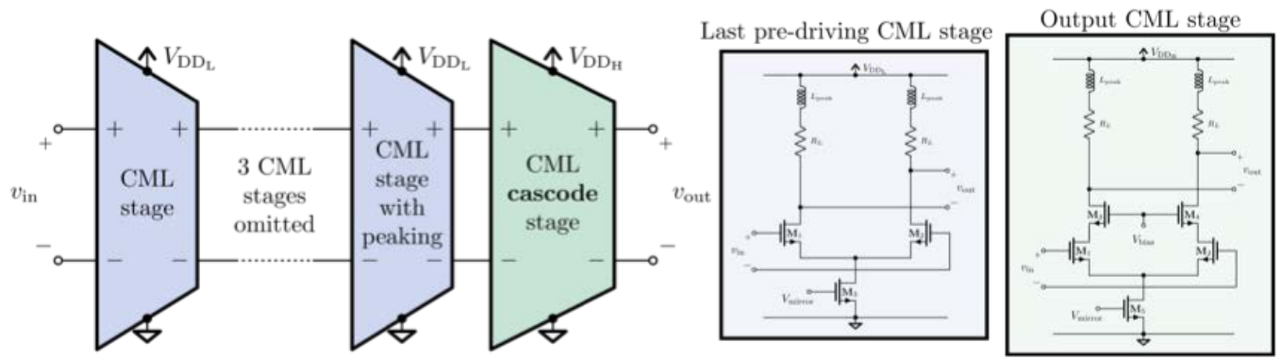


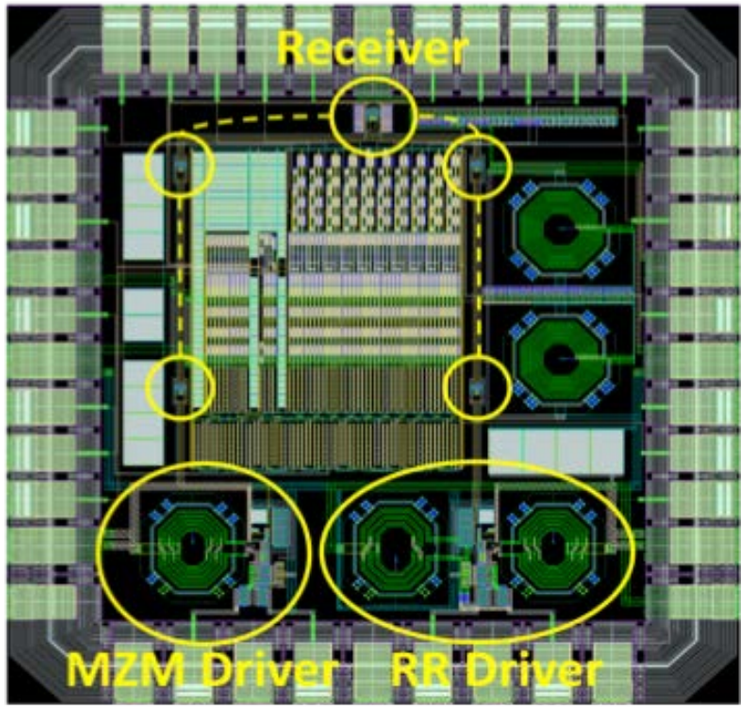
(b) shallow-etch

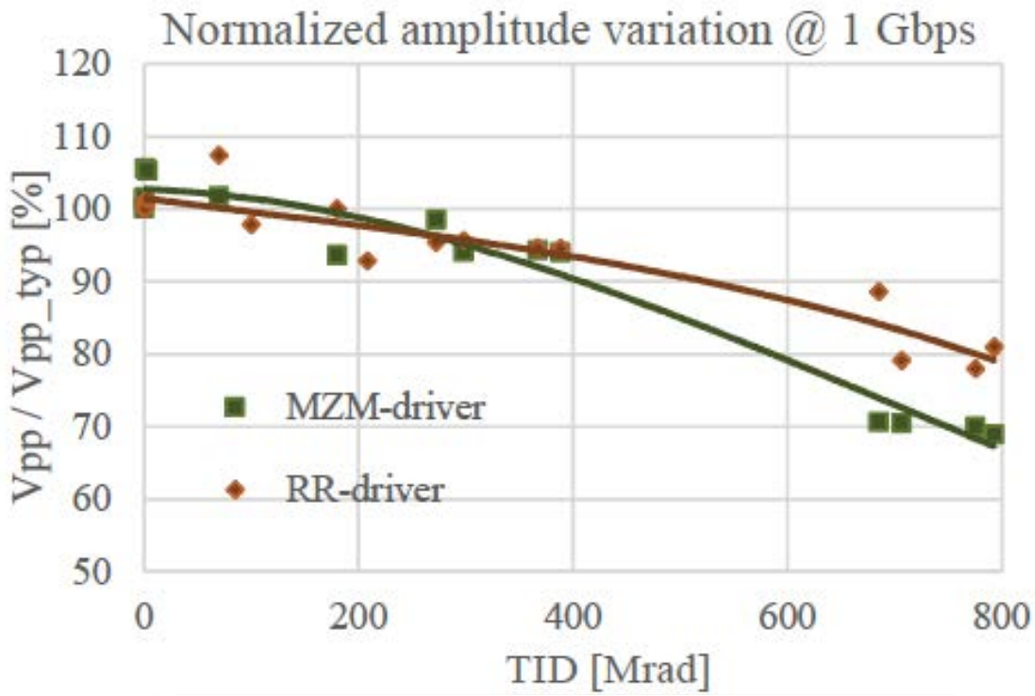
F. Vasey et al (CERN)

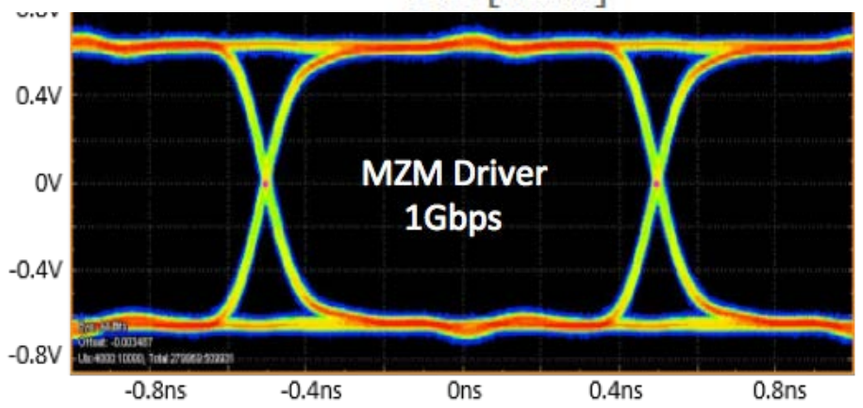
Driver in 65 nm TSMC technology

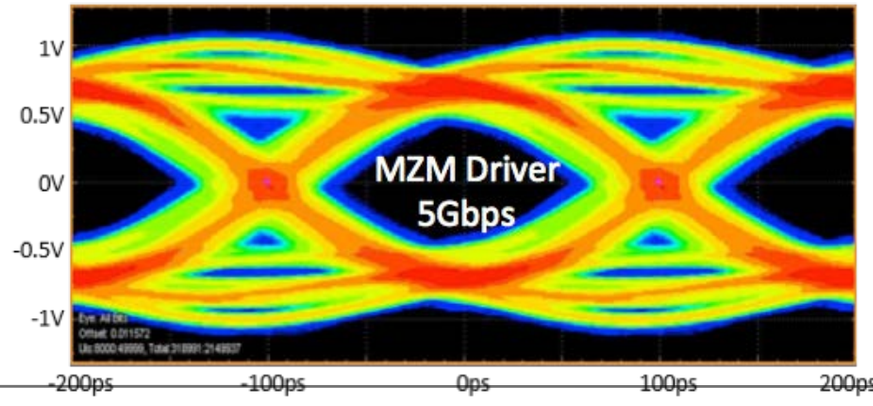
Driving voltage: above 1 V_{pp} for each arm of the MZM
Speed: 5 Gb/s
Rad Tolerance: HL-LHC compatible







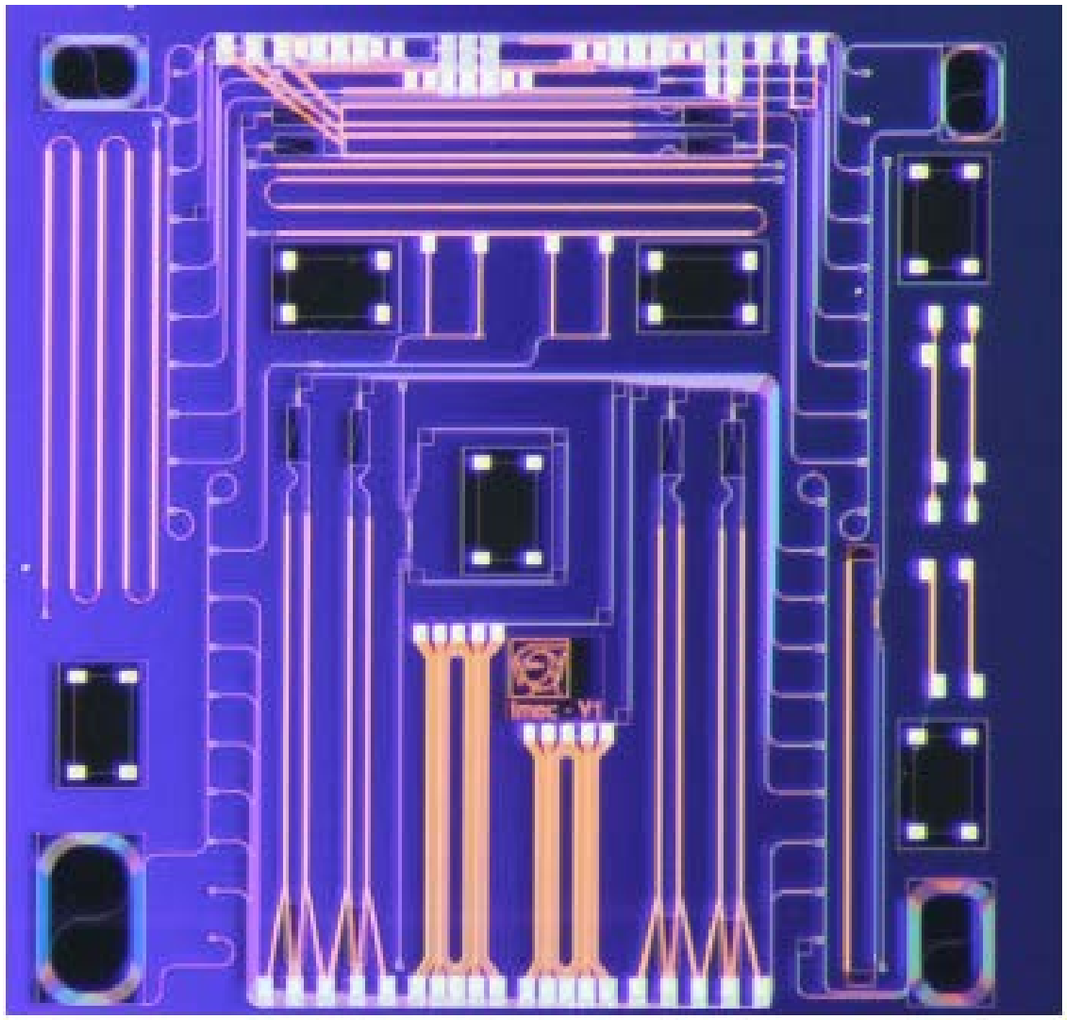


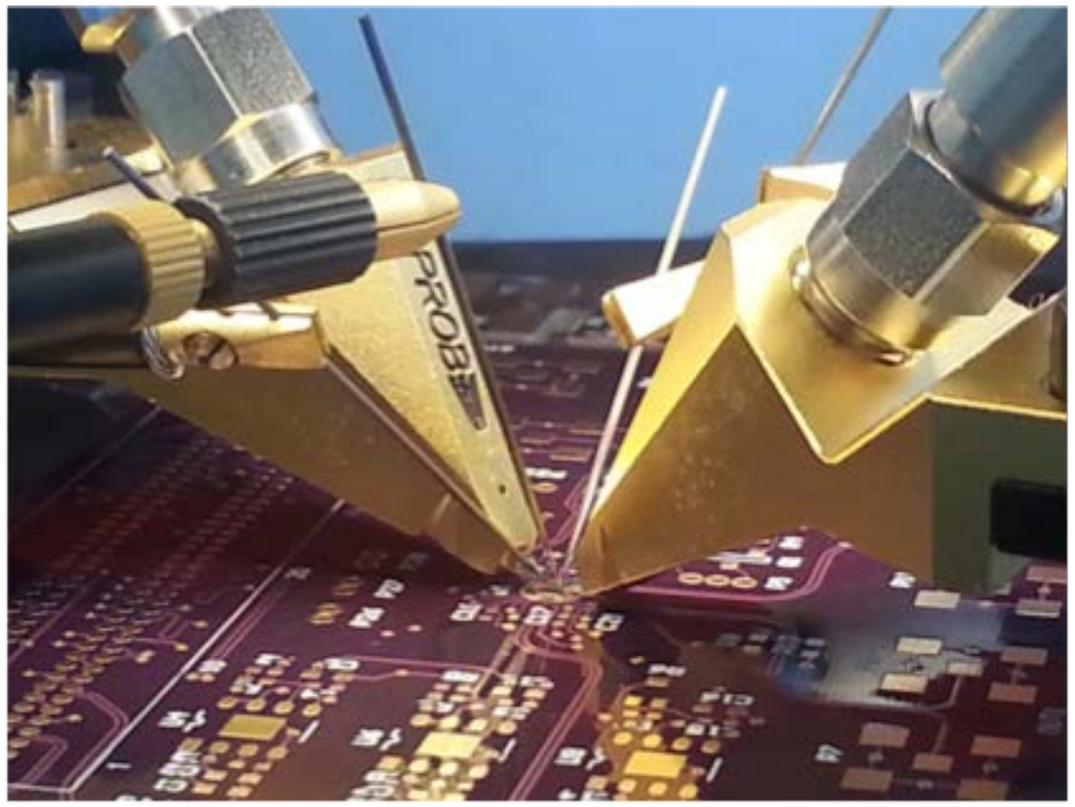


Driver chip fabricated with PHOS4BRAIN by IMEC in 2018

Integration and measurement

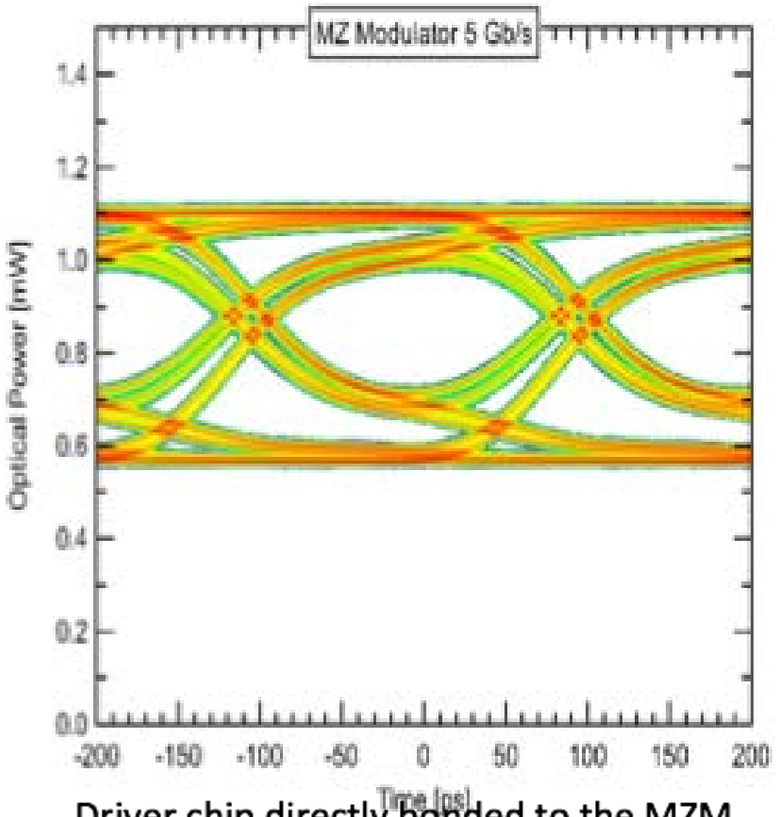
- Electrical and optical measurements of the system are done in typical and irradiated conditions for the drivers characterisation.
- We used a MZM and RR fabricated by IMEC under CERN's design in ISIPP25G technology.



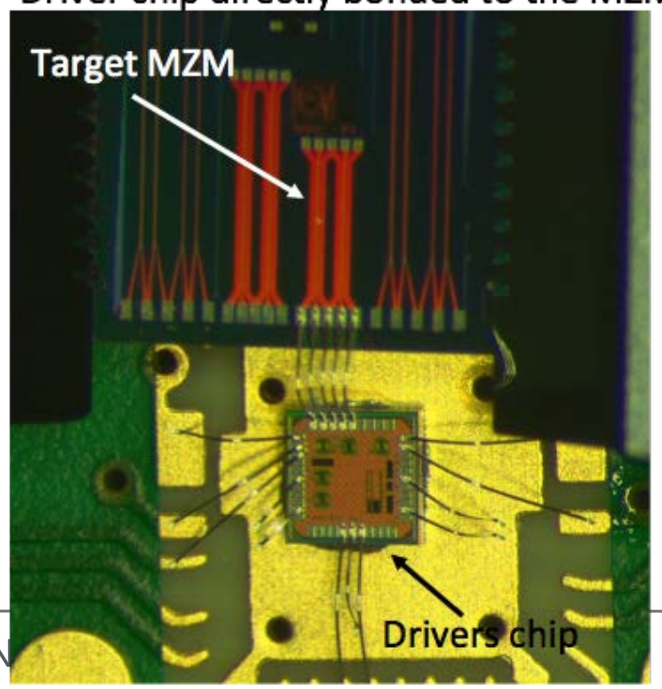


Results of the tests (Phos4brain)

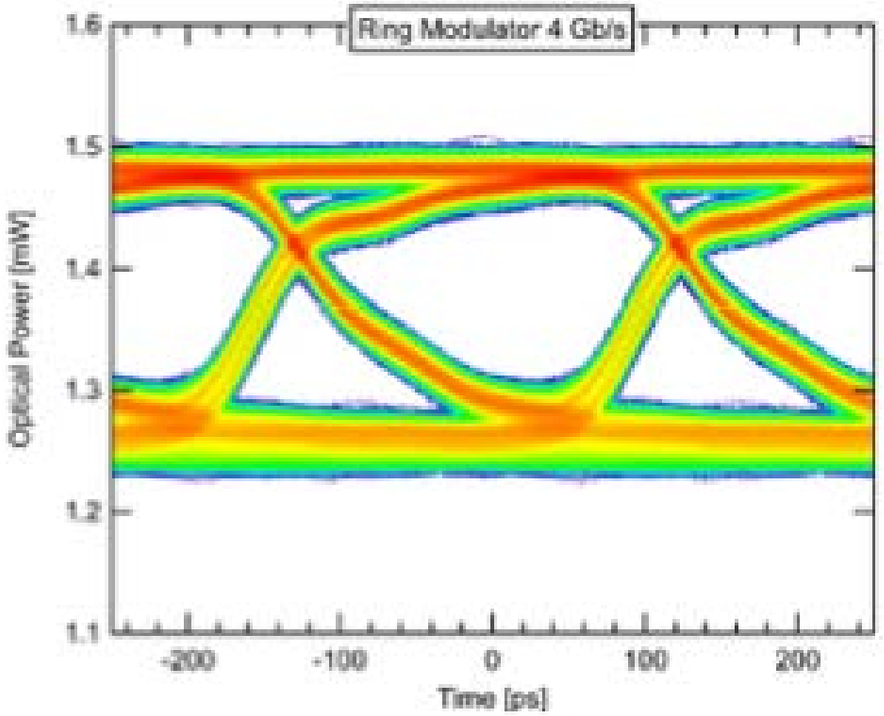
ISIPP25 MZM + Driver



Driver chip directly bonded to the MZM



ISIPP25 RR + Driver



Driver chip directly bonded to the RR