FaLaPHEL

Fast Links and RadHard Front End with Integrated Photonics and Electronics for Physics

Call aperta

Area di ricerca: Elettronica

Principal Investigator: F. Palla

INFN Units: Padova, Pavia, Pisa

External Units: Scuola Superiore S. Anna di Pisa, Dip. Ingegneria Informazione UniPisa, Dip. Fisica UniMilano

NB. The personnel from SSSA and UNIPI will be associated to INFN Pisa

Falafel

- The word “falafel” is used to refer to two distinct entities:
  - a round fritter of mashed chickpeas or other pulses
  - an Arab bread sandwich filled with those fritters and miscellaneous garnishes
    - Strangely enough in Israel the second usage prevails, while in Lebanon the first one prevails …
      - falafel has become one of the icons of Israeli culture, like wine is for France or rice for Japan and spaghetti or pizza for Italy
  - Our sandwich is composed of Silicon Photonics and Electronic dies …

Next generation HEP detectors

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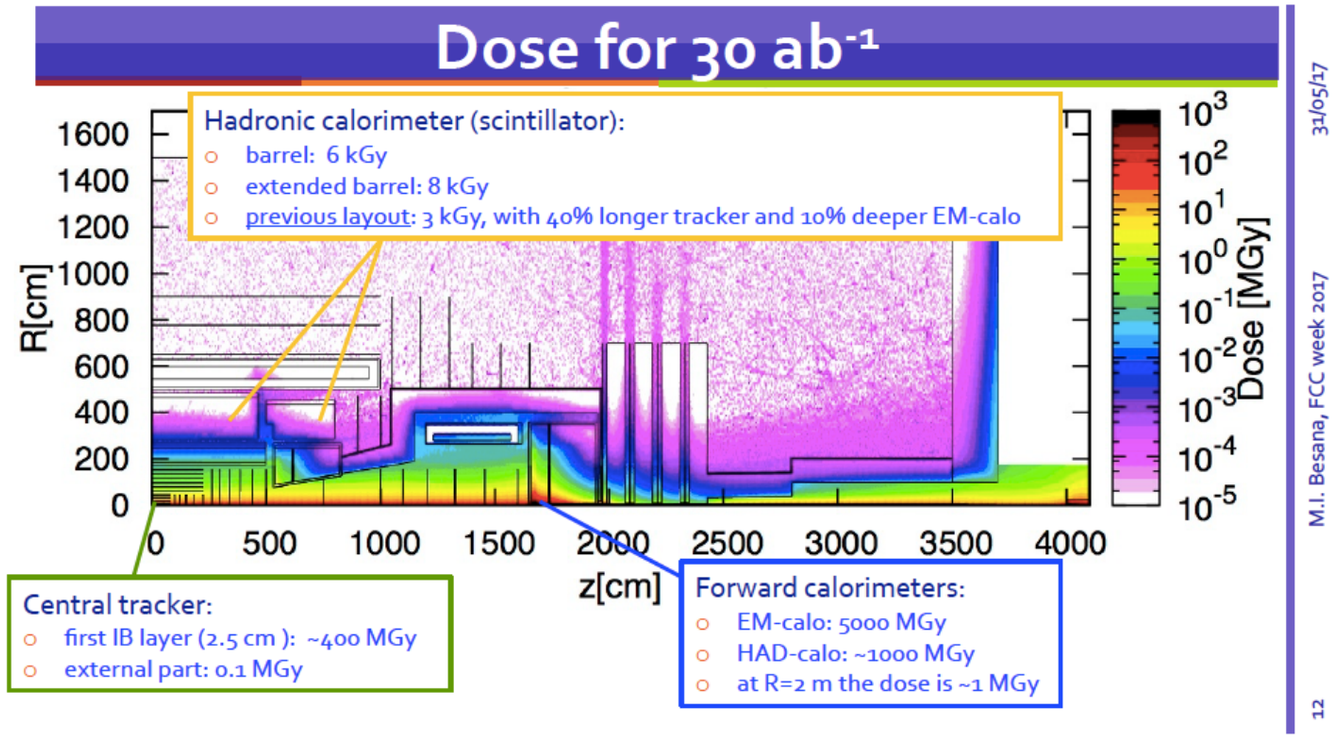
- High-Luminosity LHC
  - Increase of radiation levels
    - up to 6 MGy TID
    - up to 5x10^{16} n_{eq}/cm^2
  - Large data rates
    - Aggregate of 60 Tb/s
- FCC-hh
  - **0.5- 50 x 10^{16} n_{eq}/cm^2**
  - **0.1 to 400 MGy**
  - **Huge data rates**
    - **~6000 Tb/s outer tracker (untriggered)**
      - **150 Tb/s (triggered @ 1 MHz)**
    - **pixel module 10 Gb/s/cm^2 (triggered @ 1 MHz)**



1 MeV Neutron Equivalent Fluence for 30 ab^{-1}

Barrel calorimeter:
- EM-calo: 4 10^{15} cm^{-2} & HAD-calo: 4 10^{14} cm^{-2}
- higher values wrt previous layout

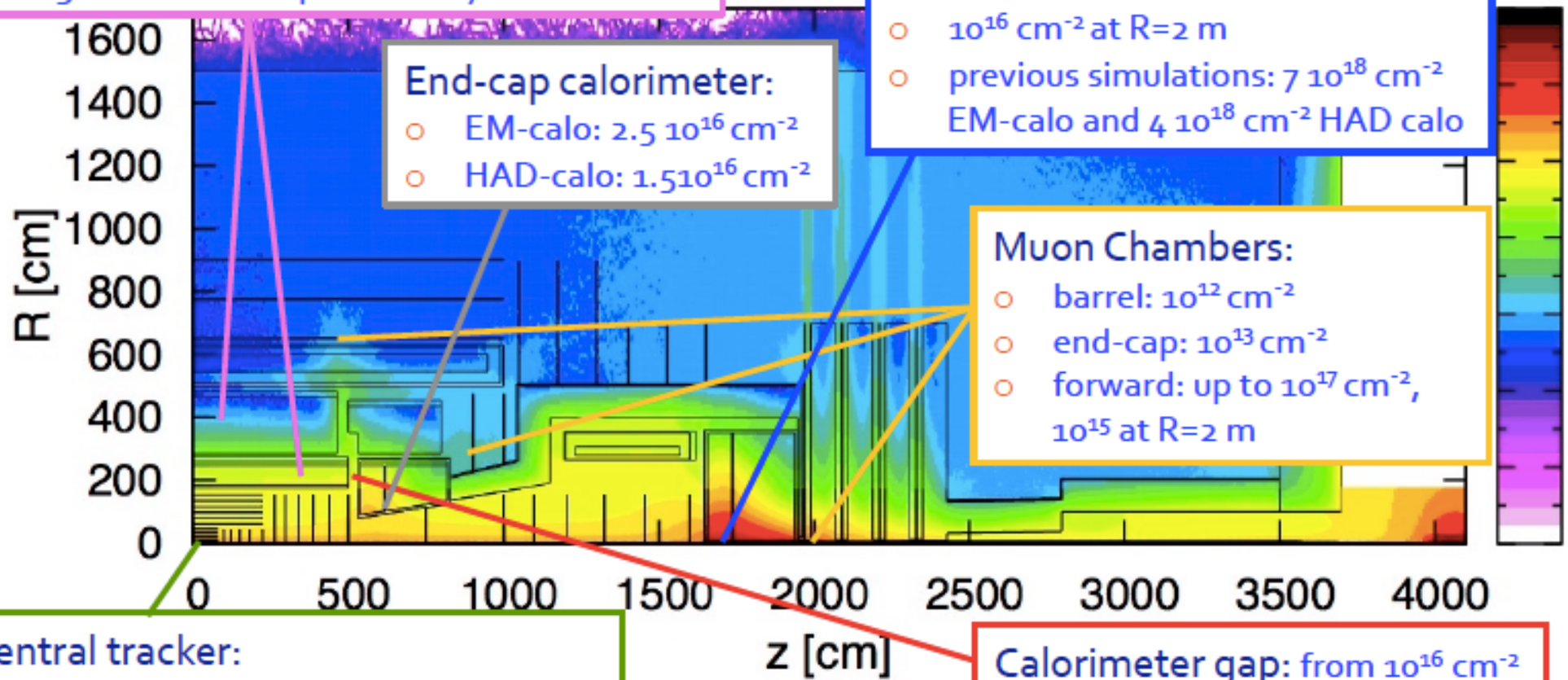
End-cap calorimeter:
- EM-calo: 2.5 10^{16} cm^{-2}
- HAD-calo: 1.5$10^{16}$ cm^{-2}

Forward calorimeters:
- maximum at ~5 10^{18} cm^{-2} for both the EM and the HAD-calo
- 10^{16} cm^{-2} at R=2 m
- previous simulations: 7 10^{18} cm^{-2} EM-calo and 4 10^{18} cm^{-2} HAD calo

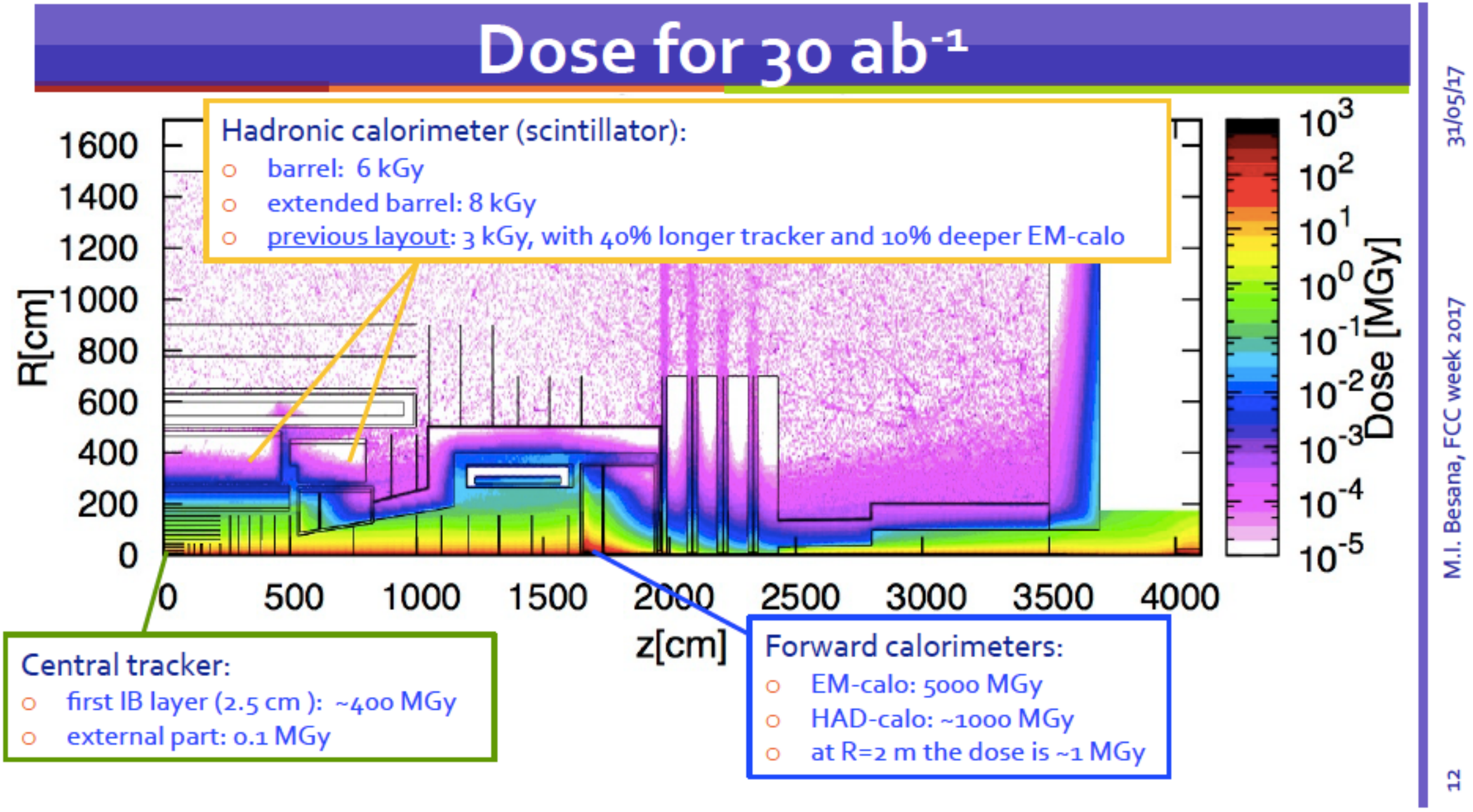
Muon Chambers:
- barrel: 10^{12} cm^{-2}
- end-cap: 10^{13} cm^{-2}
- forward: up to 10^{17} cm^{-2}, 10^{15} at R=2 m

Central tracker:
- first IB layer (2.5 cm): ~5-6 10^{17} cm^{-2}
- external part: ~5 10^{15} cm^{-2}

Calorimeter gap: from 10^{16} cm^{-2} to 10^{14} cm^{-2}



Dose for 30 ab^{-1}

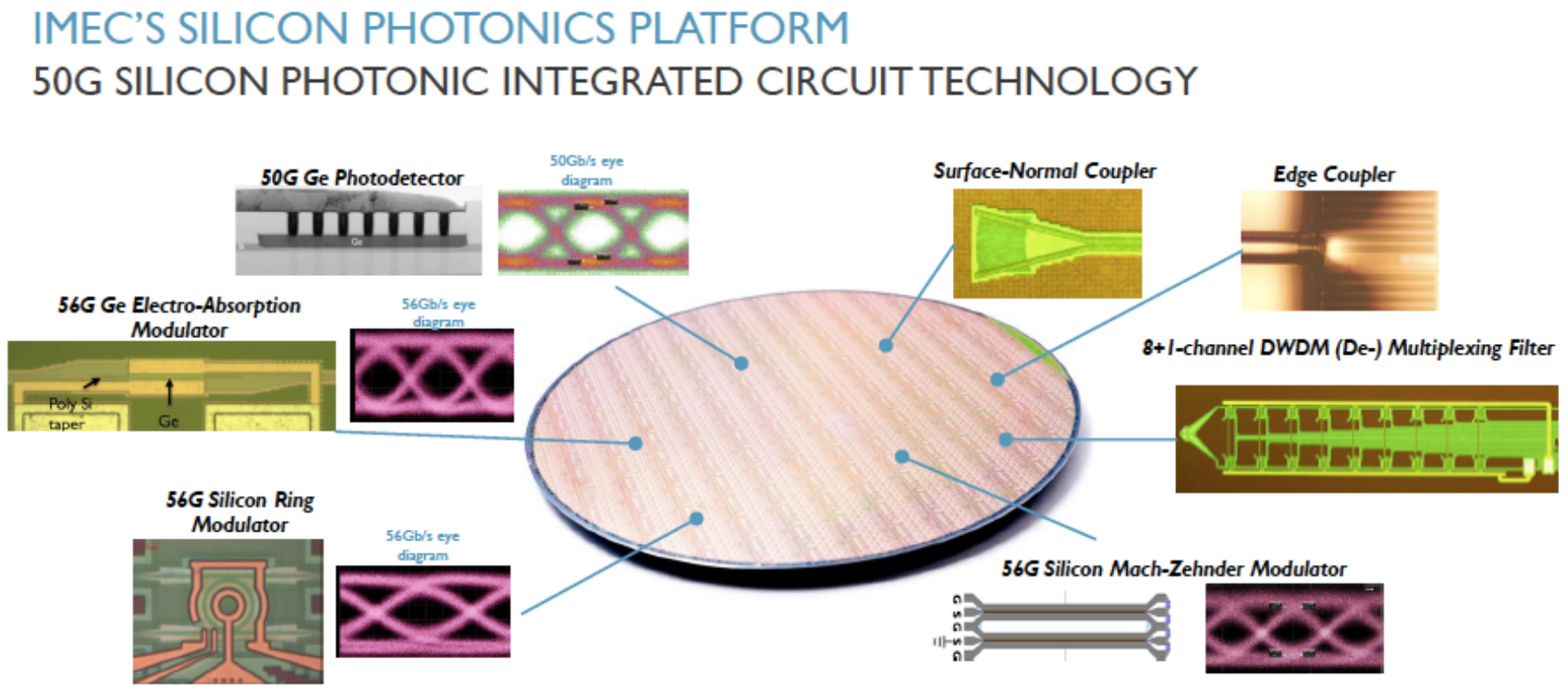


State of the Art

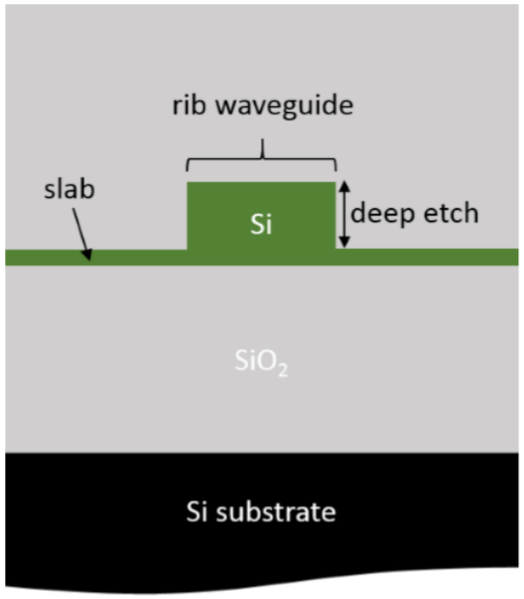
- LpGBT and Versatile Link +
  - Based on 65 nm technology and VCSEL
  - Total dose 200 MRad
  - Total fluence 10^{15} n/cm^2
    - cannot be used at HL-LHC below ~20 cm radius
      - implies RD53 chips needs e-links to LpGBT (~1 meter away)
- Silicon Photonics demonstrated to be sufficient rad-hard (>10^{16} n/cm^2 and tested up to 300 Mrad)
- PHOS4BRAIN (CSN5) project showed 65 nm driver to to be rad-hard up to 800 MRad and reach ~5 Gb/s, limited by packaging (Aluminum wire bonds)

Silicon Photonics - CMOS platform

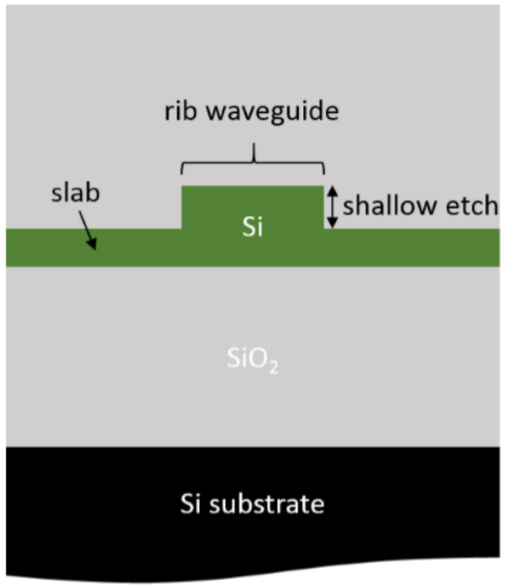
- Leverage maturity of existing CMOS infrastructure for Silicon Photonics
  - Fabrication in CMOS fabs (200mm, 300mm wafers)
  - Large Si/SiO2 refractive index contrast (dense PIC integration)
  - Advanced Si patterning capabilities (nm-scale accuracy)
  - Si(Ge) epitaxy (photodetectors, EAMs)
  - Ion implantation and low resistance contacts to Si (high-speed active devices)
  - Volume scalability and economies of scale (cost)
  - Wafer-scale 3D packaging and assembly
- Many structures can be made



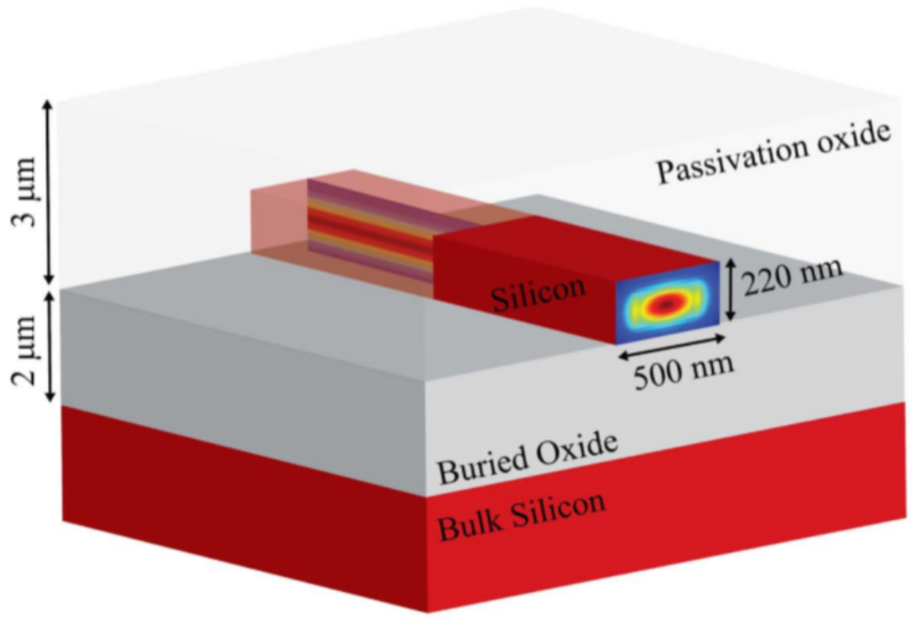
Silicon Photonics Wave Guides



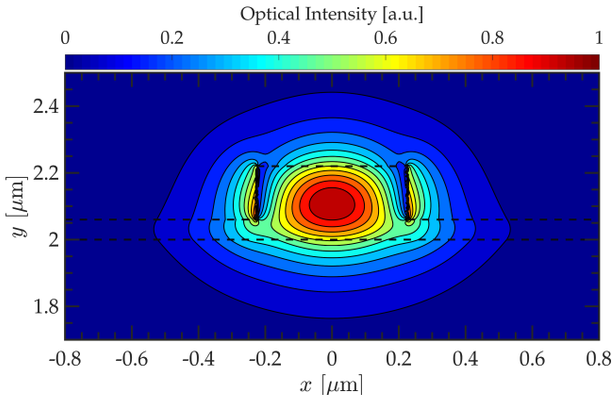
(c) deep etch rib waveguide



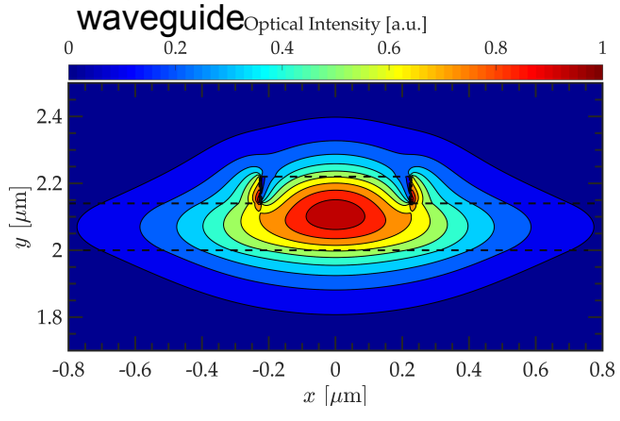
(d) shallow etch rib waveguide



TE_0 – **deep-etch rib** waveguide



TE_0 – **shallow-etch rib** waveguide



Each optical mode is characterised by the effective refractive index, which describes the propagation velocity along the waveguide (and the optical power losses)

***λ*=1550 nm (Near Infrared) NIC C-band**

Silicon Photonics Modulators

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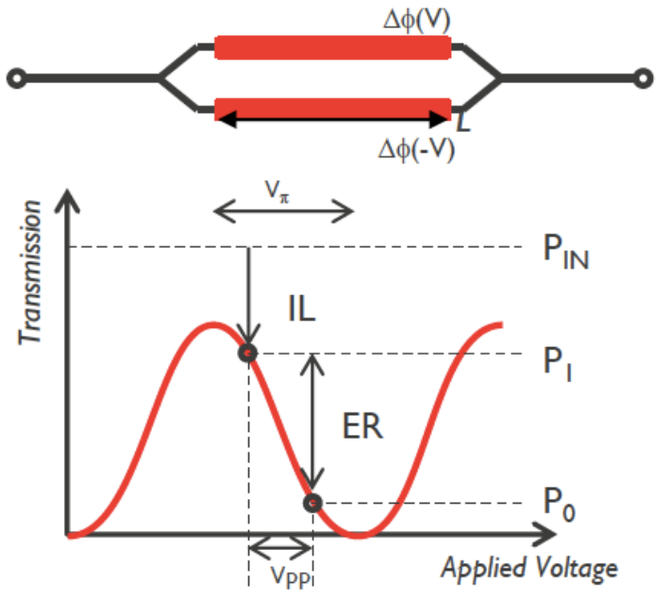
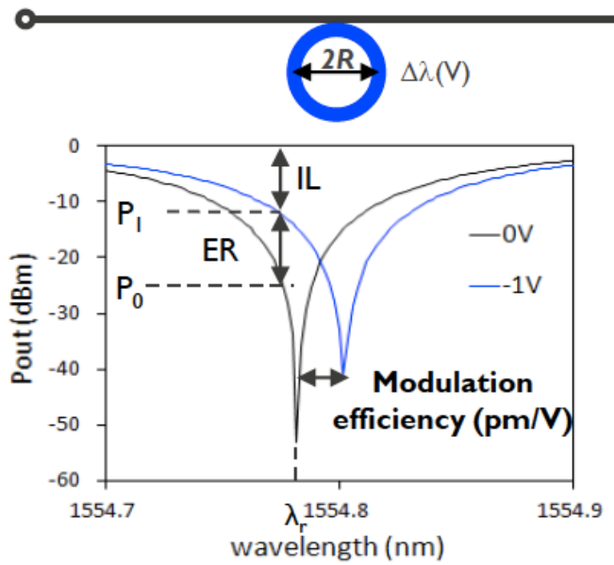
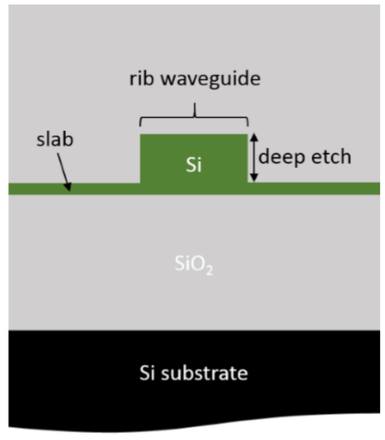
Si Mach-Zehnder Modulator

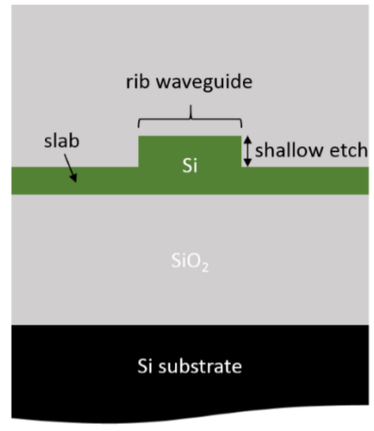


Si Ring Modulator

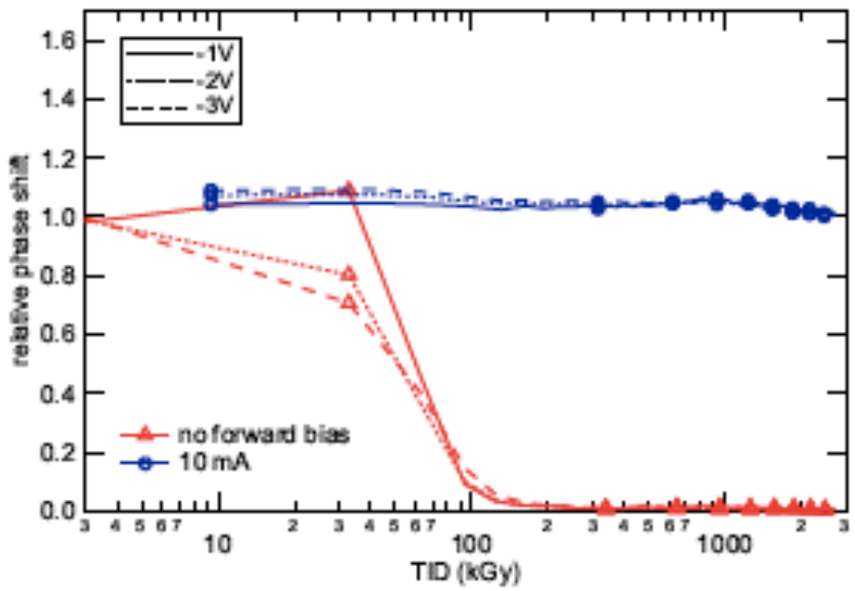




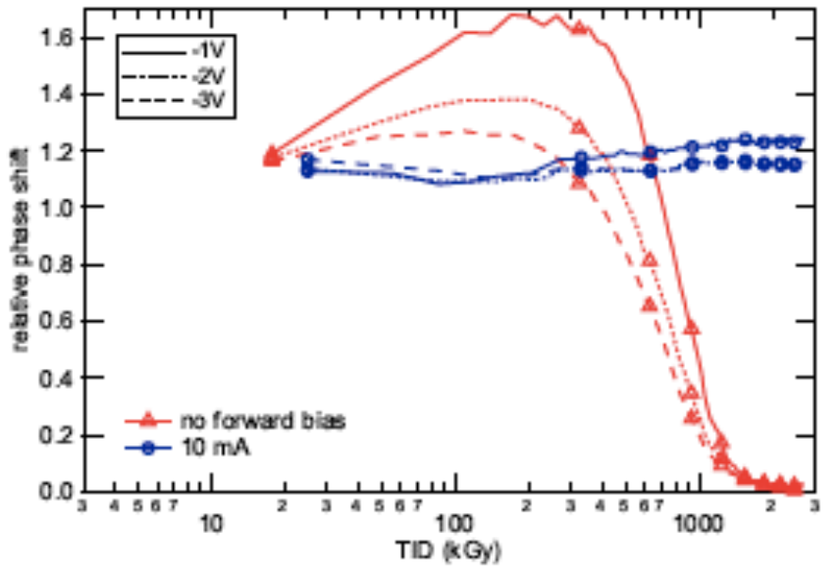
(c) deep etch rib waveguide



(d) shallow etch rib waveguide



(a) deep-etch

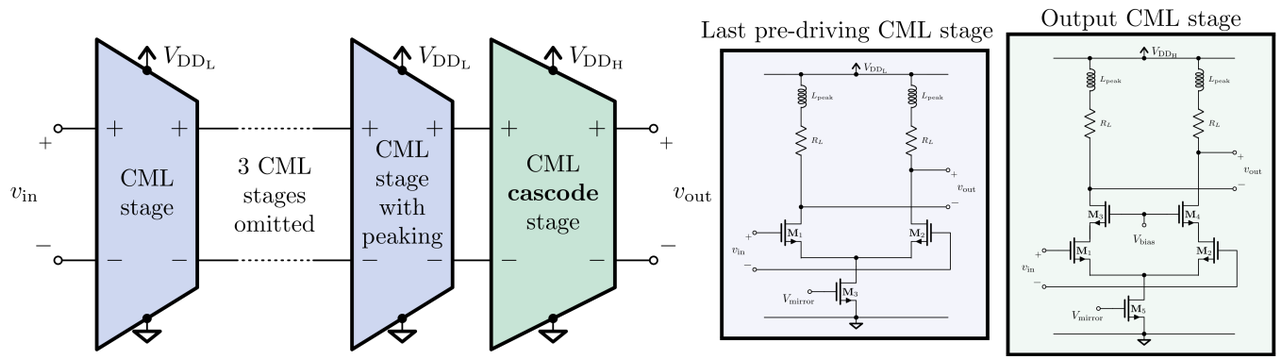


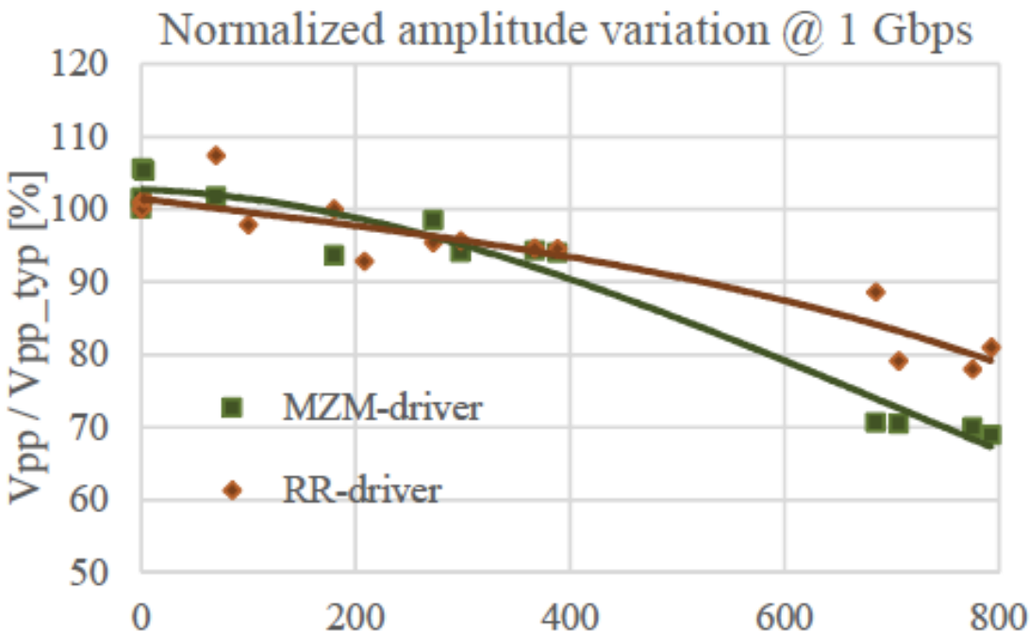
(b) shallow-etch

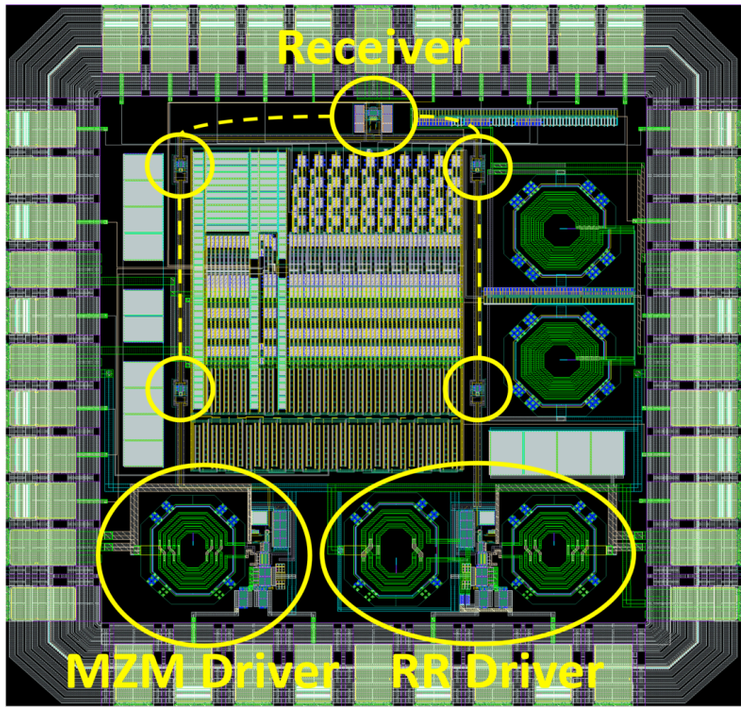
F. Vasey et al (CERN)

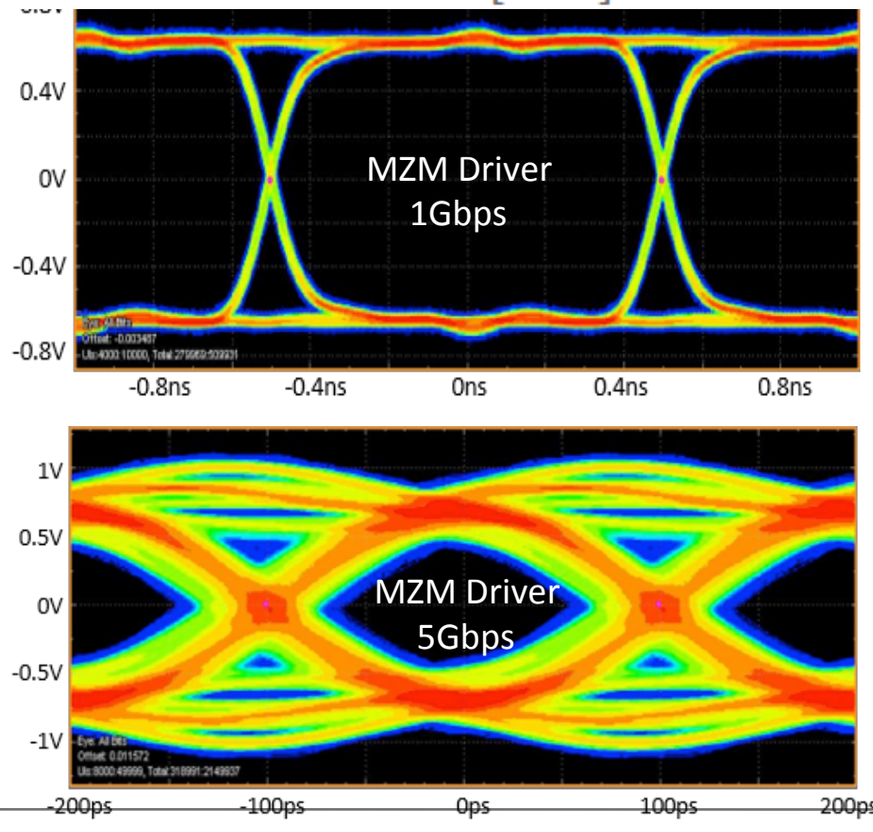
Driver in 65 nm TSMC technology

Driving voltage: above 1 V_{pp} for each arm of the MZM
Speed: 5 Gb/s
Rad Tolerance: HL-LHC compatible





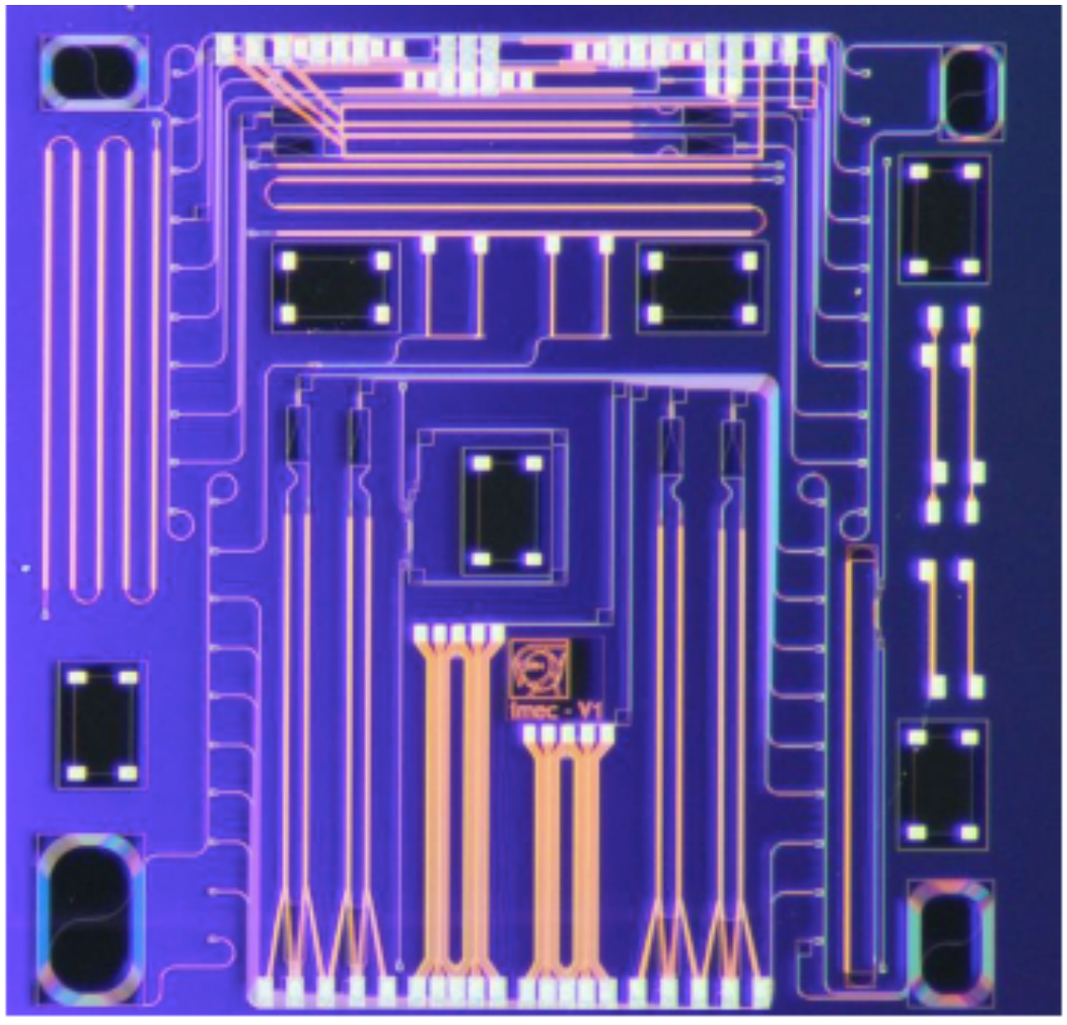


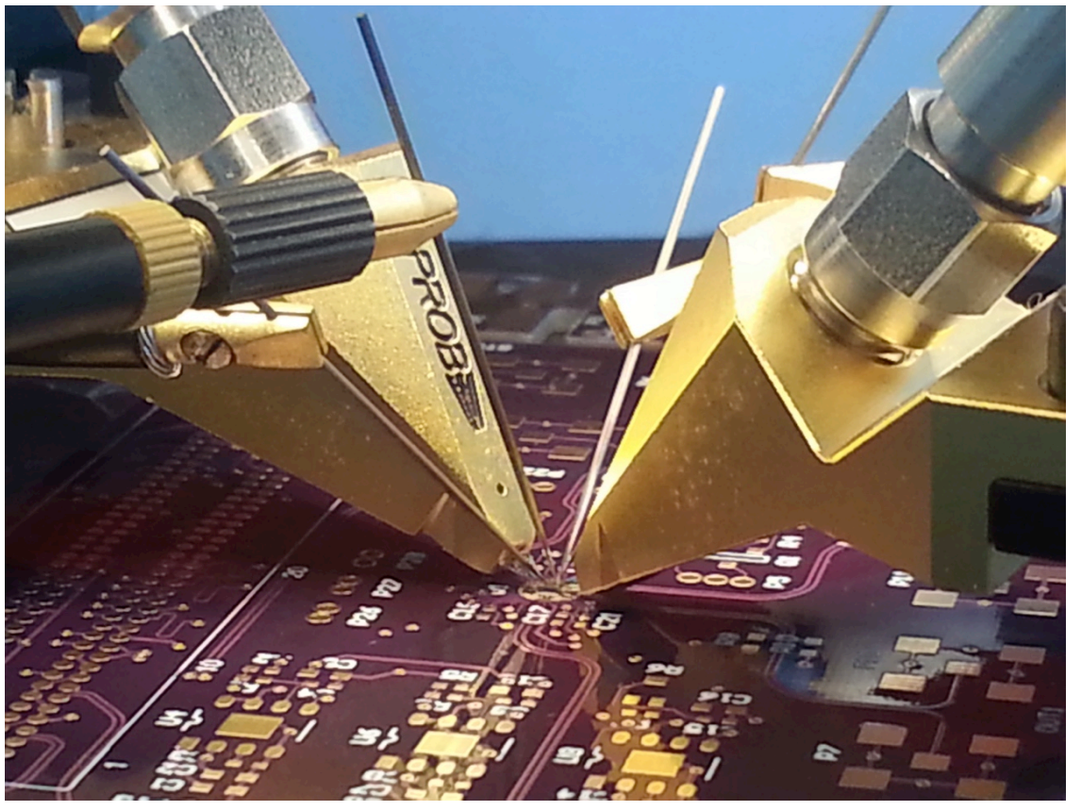


Driver chip fabricated with PHOS4BRAIN by IMEC in 2018

Integration and measurement

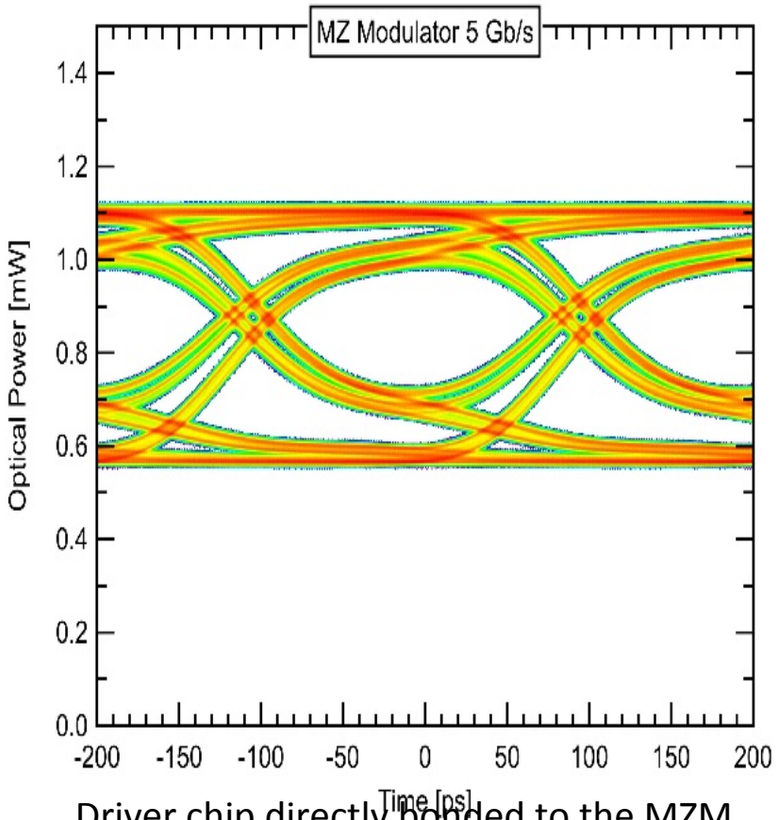
- Electrical and optical measurements of the system are done in typical and irradiated conditions for the drivers characterisation.
- We used a MZM and RR fabricated by IMEC under CERN's design in ISIPP25G technology.



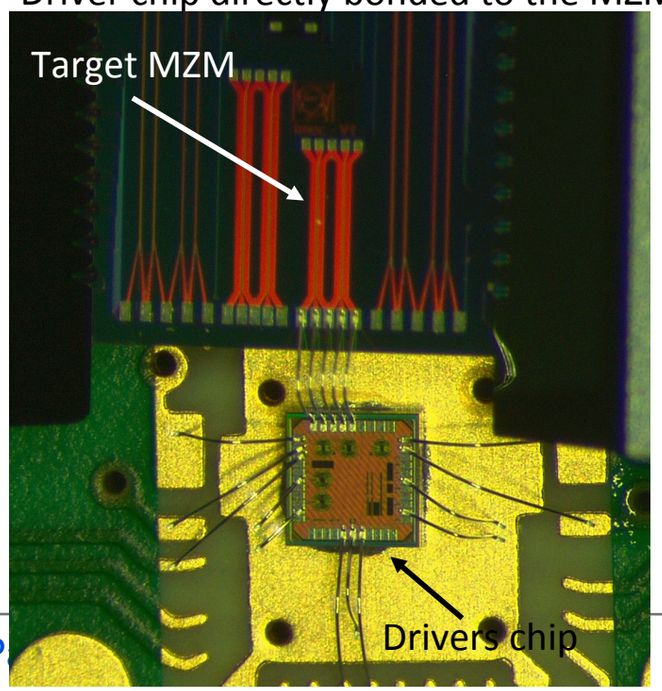


Results of the tests (Phos4brain)

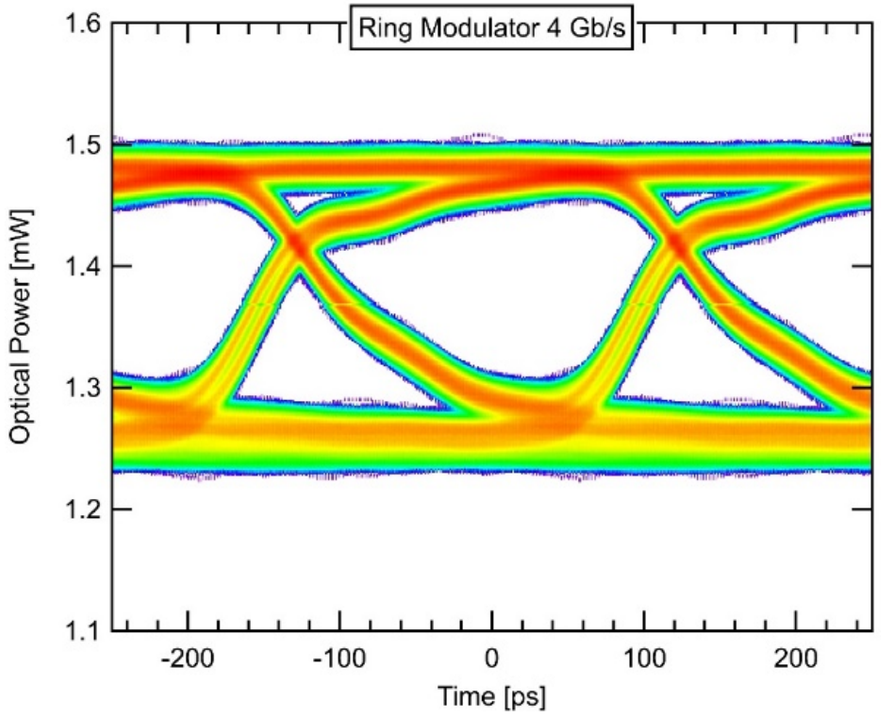
ISIPP25 MZM + Driver



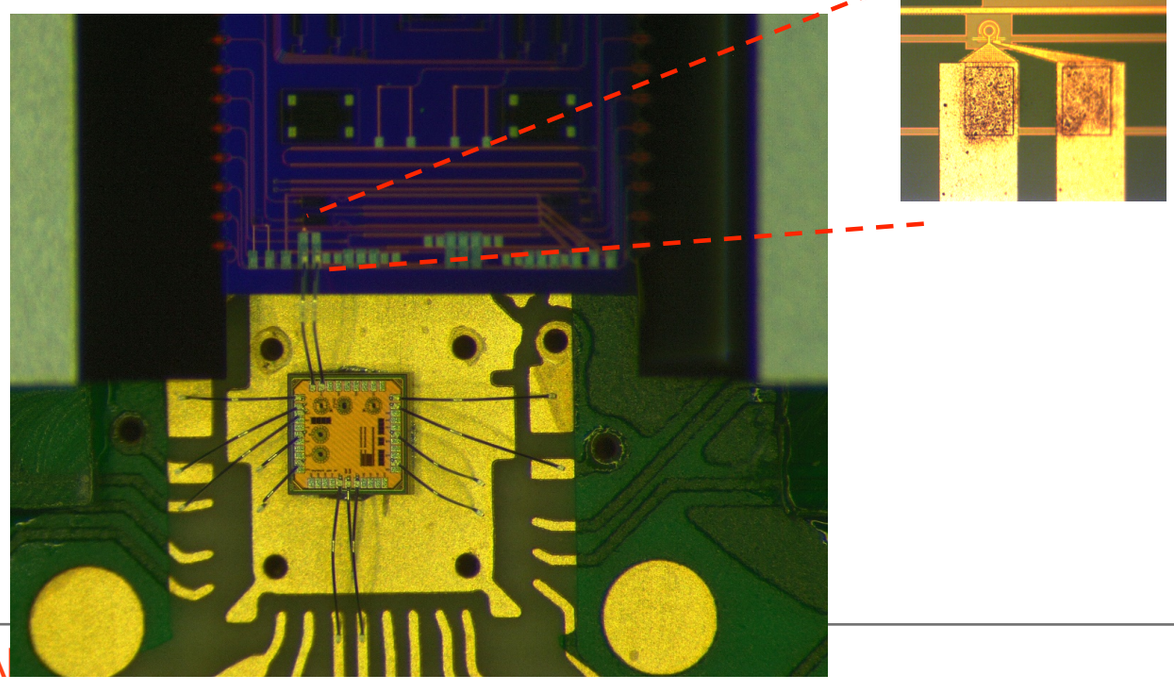
Driver chip directly bonded to the MZM



ISIPP25 RR + Driver



Driver chip directly bonded to the RR

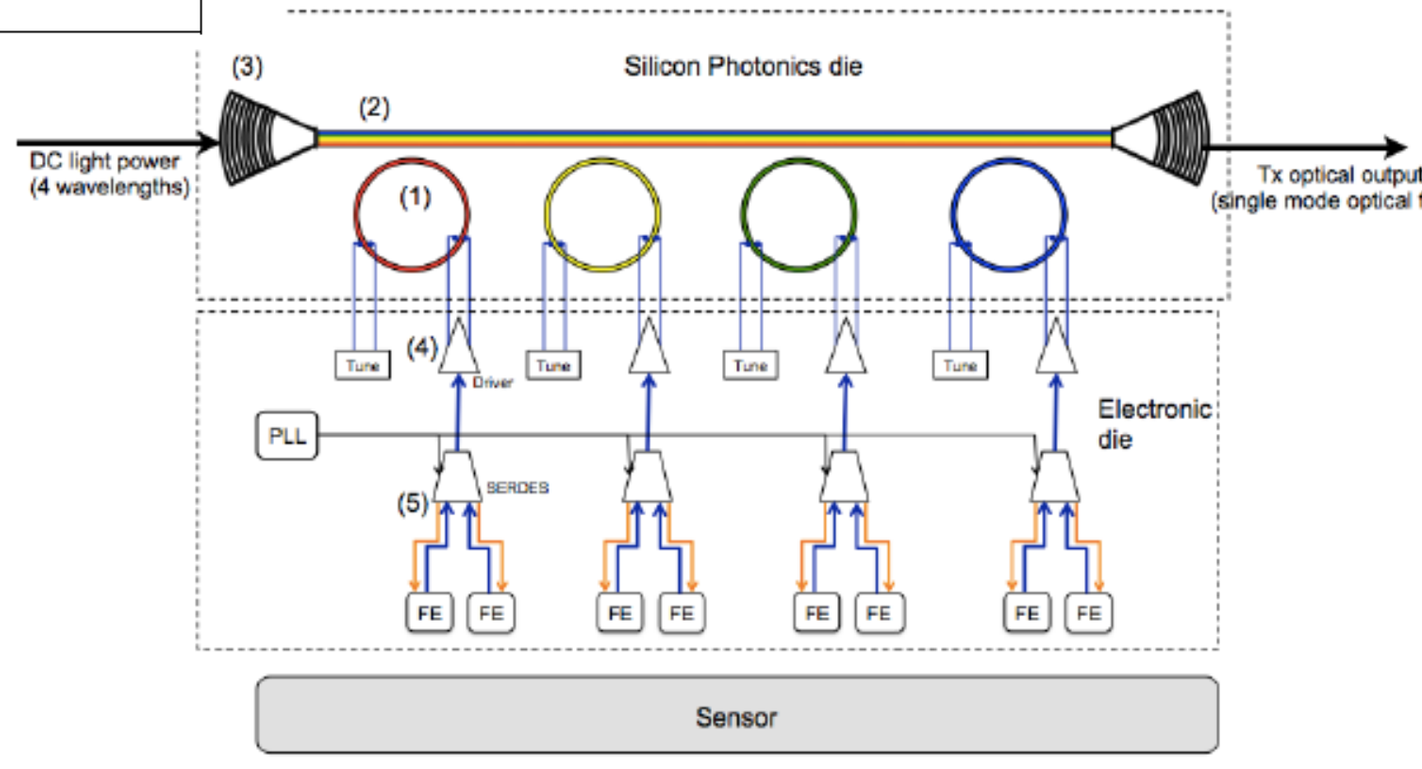


Goals of FALAPHEL

- Hybrid (3D or 2.5D) integration of Silicon Photonics modulators with high speed radiation hard (≥1 GRad) electronics in 28 nm
  - Aggregated 100 Gb/s links using wavelength division multiplexing (4 wavelength on a single optical fibre) and Integrated Front-End electronics

Table 1: Technology benchmarks and envisioned performance improvement with FALAPHEL

	State of the art – VCSEL+	**This project (FALAPHEL)**
Data rate	10 Gb/s	≥100 Gb/s
Radiation TID	200 Mrad (2 MGy)	≥1 Grad (10 MGy)
Total Fluence	10^{15}n/cm^2	>5 x 10^{16}n/cm^2



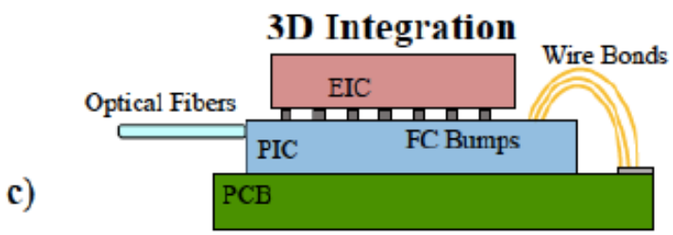
Challenges - I

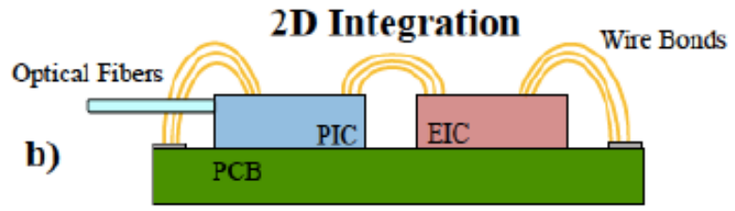
- ASIC: advantages of 28 nm wrt 65 nm
  - Allows to reach higher modulation speed at same power consumption
  - Higher radiation tolerance
  - Parasitic effects have larger impact
    - requires optimisation and study of bonding pads and interconnects
      - **Synergy with AIDAInnova**
- Front-End
  - allows to reach lower power and lower thresholds
- Photonics: Ring vs Mach-Zehnder Modulators
  - RM have smaller driving voltage than MZM
    - ~1V vs 2V
  - RM an be tuned for different wavelengths allowing WDM
    - single optical fibre
  - More sensitive to temperature variations
    - Need tune circuits

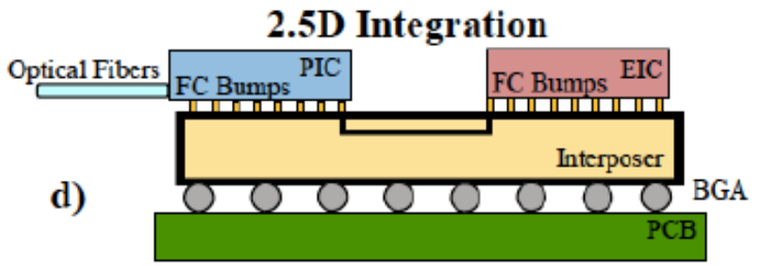
Challenges - II

- Hybrid assembly of two chips
  - parasitic 3D (flip chip) < 2.5D (interposer) < 2D (wire bonds)
    - Need careful thermal management
      - Pisa “Alte tecnologie” thermo-fluid Lab expertise

        Synergy with AIDAInnova
      - Interest to use DIAM expertise (INFN Padova) on producing metallic additive manufacturing structures for heat removal



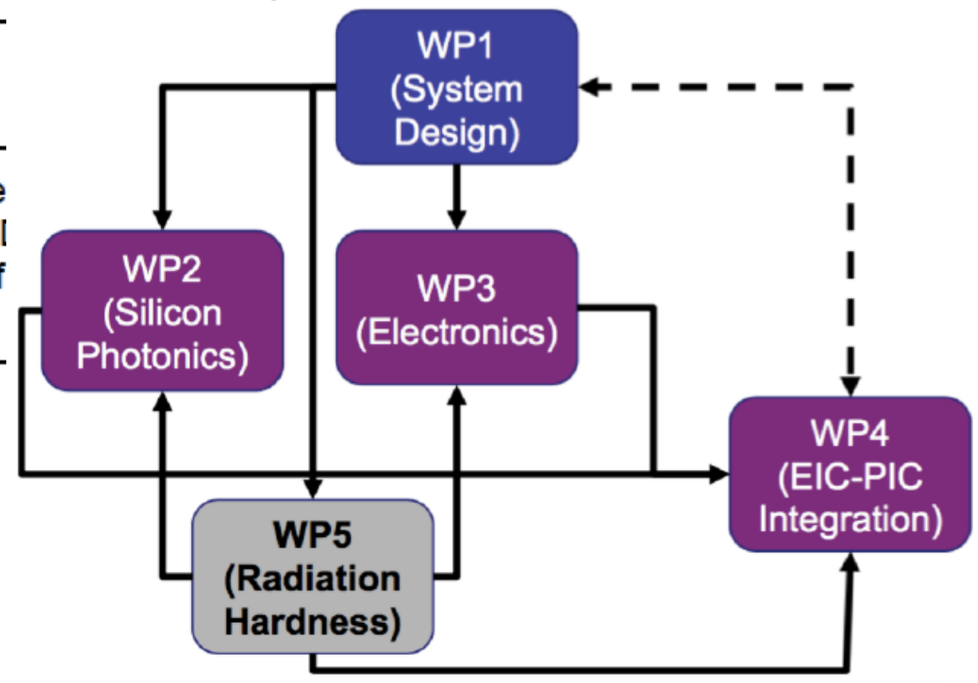




WP Structure

Table 3. Work Packages.

WP	Topic	Leader	Unit	Areas of work
1	System Design	Luigi Gaioni	INFN Pavia	Demonstrator design, system specifications and key performance indicators
2	Silicon Photonics	Stefano Faralli	Scuola Superiore S. Anna of Pisa	PIC blocks, Ring-Resonator Modulator, MachZehnder Modulator, WDM and SDM
3	Electronics	Gianluca Traversi (focus FE) and Guido Magazzu (focus IP cores)	INFN Pavia INFN Pisa	Serdes, Driver, PLL/CDR, DAC, Bandgap, Front-End
4	EIC-PIC Integration	Sergio Saponara	University of Pisa	Packaging and integration, thermal studies, prototyping and fabrication
5	Radiation hardness	Serena Mattiazzo	INFN Padova	Tests with X-rays, protons, neutrons
6	Project management and dissemination	Fabrizio Palla	INFN Pisa	Resource manage and coordination. I and exploitation of



Commitments for Pisa

- WP1 (System Design) defines the system specifications and key performance indicators (KPI) as inputs to WP 2 to 5 to outperform state of the art and benchmarking. Designs the final demonstrator together with WP4.
  - G. Ciarpi, S. Faralli (also SSSA), G. Magazzù, D. Monda (also UNIPI), F. Palla, P. G. Verdini, AdR#1, AdR2
- WP2 (Silicon Photonics) It will develop the SiPh building blocks.
  - D2.1 SiPh submissions for the MPW run of the first miniblock including the building blocks (SSSA, INFN PI, UNIPI, UNIMI) (T0+7)
  - D2.2 SiPh submission for the MPW run full final block (SSSA, INFN PI, UNIPI, UNIMI) (T0+19)
    - AdR#2, S. Faralli (also SSSA), S. Cammarata (also UNIPI)

Commitments for Pisa

- WP3 (Electronics) design of the fundamental rad-hard and high-speed electronics and test boards
  - D3.1/3.1b Serdes (INFN PI, UNIPI, UNIMI): 1st/2nd submissions (T0+10, T0+16)
  - D3.2/3.2b Drivers and Tune circuit (INFN PI and PV, UNIPI): 1st and 2nd submissions (T0+10, T0+16)
  - D3.3/3.3b PLL/CDR (UNIPI, INFN PD and PI): 1st/2nd submission (T0+10, T0+16)
    - S. Cammarata (also UNIPI), G. Magazzù, D. Monda (also UNIPI), G. Ciarpi, F. Morsani, AdR#2, AdR#3

- WP4 (EIC-PIC Integration) will develop the integration of the PIC and EIC (akaDemonstrator), together with an external company.
  - D4.1/4.1b Prototypes and final demonstrator system (All) (T0+22, T0+32)
  - D4.2 Demonstrator tests (All) (T0+36)
    - F. Bosi, G. Ciarpi, S. Faralli (also SSSA), M. Massa, D. Monda (also UNIPI), AdR#1, AdR#2

Participants per research unit

Table 5. List of participant Units with their leaders, FTE/year, number of members and designers (MEC: Mechanical; ELE: Electronic; PHO: Silicon Photonics).

Research Unit	Leader	FTE/year	Members	Designers
INFN Pisa	Fabrizio Palla	1.9 + 3 (AdR)	8 + 3 (AdR)	ELE: 3 + 2 (AdR) PHO:1 (AdR) MEC: 2
INFN Pavia	Luigi Gaioni	1.6 + 2 (AdR)	5 + 2 (AdR)	ELE: 5 + 2 (AdR)
INFN Padova	Serena Mattiazzo	1.55 + 1 (AdR)	7 + 1 (AdR)	ELE: 7 + 1 (AdR)
University of Pisa	Sergio Saponara	1.05	3	ELE: 2 ELE/PHO: 1
SSSA	Stefano Faralli	0.80	3	PHO: 3
University of Milan	Valentino Liberali	0.15	3	ELE: 2 PHO: 1

Participant list - Pisa

Name	Role	Unit	WP1	WP2	WP3	WP4	WP5	Total
F. Bosi	MEC	INFN PI				10		10
G. Ciarpi	ELE	INFN PI	10		70	20		100
R. Dell'Orso	PHY	INFN PI					5	5
G. Magazzù	ELE	INFN PI	5		25			30
M. Massa	MEC	INFN PI				10		10
F. Morsani	ELE	INFN PI			5	5		10
F. Palla	PHY	INFN PI	20					20
P. G. Verdini	PHY	INFN PI	5					5
AdR #1	PHO	INFN PI	10	70		20		100
AdR #2	ELE	INFN PI	10		70	20		100
AdR #3	ELE	INFN PI			90		10	100

Participant list Others

M. Bagatin	ELE	INFN PD				15	15
A. Candelori	ELE	INFN PD				20	20
S. Gerardin	ELE	INFN PD				15	15
S. Mattiazzo	ELE	INFN PD				20	20
A. Paccagnella	ELE	INFN PD				15	15
M. Teng	ELE	INFN PD				50	50
D. Vogrig	ELE	INFN PD			20		20
AdR #6	ELE	INFN PD				100	100
L. Gaioni	ELE	INFN PV	40				40
L. Ratti	ELE	INFN PV			30		30
V. Re	ELE	INFN PV	10				10
E. Riceputi	ELE	INFN PV				50	50
G. Traversi	ELE	INFN PV			30		30
AdR #4	ELE	INFN PV			100		100
AdR #5	ELE	INFN PV	50		50		100
F. Di Pasquale	PHO	SSSA		10		10	20
S. Faralli	PHO	SSSA	5	20		10	35
P. Velha	PHO	SSSA	5	10		10	25
S. Cammarata	EIC/PHO	Univ. Pisa		20	10	10	40
D. Monda	EIC	Univ. Pisa	10		30	10	50
S. Saponara	EIC	Univ. Pisa			5	10	15
L. Frontini	PHO	Univ. Milan		5			5
V. Liberali	EIC	Univ. Milan			5		5
A. Stabile	EIC	Univ. Milan	5				5
			WP1	**WP2**	**WP3**	**WP4**	**WP5**	**Total**
TOTAL			**185**	**135**	**540**	**145**	**300**	**1305**

Budget

ITEM	WP	Year 1			Year 2			Year 3			TOTAL
		PD	PV	PI	PD	PV	PI	PD	PV	PI	
Travels				**2**			**5**			**5**	
Irradiation and testing	5			0			3			3	
Work between designers	6			1			1			1	
General meetings / conferences	6			1			1			1	
Consumables				**89**			**119**			**25**	
EIC submission	3			34			34			0	
PIC submission	2			25			50			0	
Test boards EIC	3			10			10			0	
Test boards PIC	2			0			5			5	
X-ray tubes	5			0			0			0	
Others (cables, fibers, glues, fluids, powder, renting equipment)	1,2,3, 4,5			20			20			20	
Access to external irradiation facilities	5			0			0			0	
External services				**10**			**15**			**25**	
Demonstrator design and assembly	4			10			15			25	
Licenses				**8**			**1**			**1**	
PIC design	2			8			1			1	
Equipment				**35**			**0**			**0**	
FPGA	3			10			0			0	
Power supply	3			0			0			0	
Laser Source (DFB) x2	2			10			0			0	
Workstations / HD / Screen	2			5			0			0	
Workstations / HD / Screen	3			10			0			0	
TOTAL w/o AdR				**144**			**140**			**56**	
Assegni di Ricerca (AdR)				**85**			**72,5**			**12,5**	
TOTAL				**229**			**213**			**69**	**905,5**

Assegni di Ricerca

Table 6. Requested AdR. Type: Junior (J) / Senior (S)

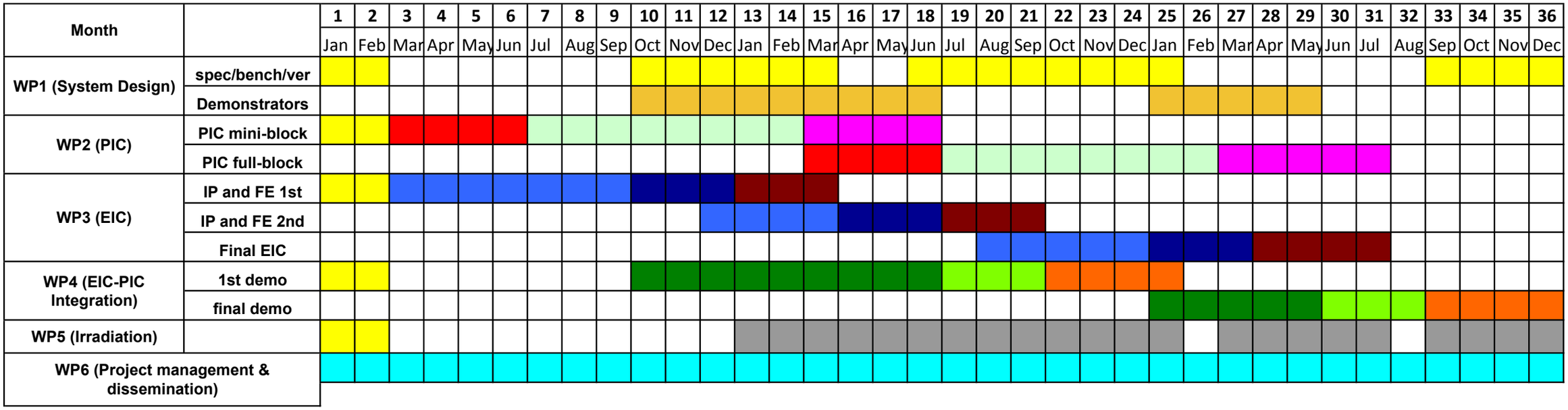
AdR #	Type	Unit	Months	Research Topic
1	J	PI	30	PIC design and test. PIC-EIC integration and test
2	S	PI	24	Driver design. PIC-EIC integration and test
3	J	PI	18	PLL/CDR design and test
4	J	PV	30	DAC design and test
5	S	PV	24	FE design, test and integration in the demonstrator
6	J	PD	24	Irradiation tests and analysis

INFN Pisa services requests

Electronics service: Two designers (G. Magazzù 30%, F. Morsani 10%), one technician (10%), electronics lab: 8 GHz band oscilloscope for serial bus analysis and a 18 GHz band Time Domain Reflectometer; a pattern generator/logic analyzer with probes at programmable levels both single-ended and differential.

High Technology service: two mechanical engineers (M. Massa 10%, F. Bosi 10% , one technician (20%), thermo-fluid-dynamics and clean rooms.

Gantt chart



MILESTONES
Deliverables

M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
D1.1	D2,1	D3.1/5	D3.1b D5.1	D1.2 D2.2	D4.1	D5.1 D3.6	D5.1 D2.3	D4.1	D4.2 D6.2

Legenda

- Specifications/benchmark/verification
- PIC design & layout
- PIC fabrication
- EIC design & layout
- EIC fabrication
- Integration test
- Integration design
- EIC-PIC Integration
- EIC test
- PIC test
- Irradiation

Milestones

M1 (Definitions of the specs and KPI) (T0+2)
M2 (Silicon Photonics PIC design for the submission of the mini-block chip fabrication) (T0+6)
M3 (1st submission of the High Speed rad-hard block design) (T0+10)
M4 (2nd submission of the High Speed rad-hard block design) (T0+16)
M5 (Final Silicon Photonics PIC design for the submission of the full block chip fabrication) (T0+18)
M6 (First integration EIC+PIC) (T0+21)
M7 (Final, large area EIC submission) (T0+25)
M8 (Qualification of rad-hardness of PIC and EIC) (T0+29)
M9 (Final demonstrator integration) (T0+32)
M10 (Final demonstrator qualification) (T0+36)

ID	Task Name	Start	Finish
1	Definition of the Specs and KPI	Fri 01/01/21	Sun 28/02/21
2	M1 - Definition of the Specs and KPI	Sun 28/02/21	Sun 28/02/21
3	PIC mini-block design	Mon 01/03/21	Wed 30/06/21
4	M2 - PIC mini-block ready for submiss	Wed 30/06/21	Wed 30/06/21
5	PIC mini-block fabrication	Thu 01/07/21	Mon 28/02/22
6	PIC mini-block test	Tue 01/03/22	Thu 30/06/22
7	PIC mini-block irradiation tests	Tue 01/03/22	Thu 30/06/22
8	PIC full-block design	Tue 01/03/22	Thu 30/06/22
9	M5 - PIC full-block ready for submissic	Thu 30/06/22	Thu 30/06/22
10	PIC full-block fabrication	Tue 05/07/22	Tue 28/02/23
11	PIC full-block test	Wed 01/03/23	Wed 31/05/23
12	PIC full-block final characterization	Thu 01/06/23	Mon 31/07/23
13	PIC full-block irradiation tests	Wed 01/03/23	Mon 31/07/23
14	EIC Run1 design	Mon 01/03/21	Thu 30/09/21
15	M3 EIC Run1 ready for submission	Thu 30/09/21	Thu 30/09/21
16	EIC Run1 fabrication	Fri 01/10/21	Thu 30/12/21
17	EIC Run1 test	Fri 31/12/21	Thu 31/03/22
18	EIC Run 1 irradiation tests	Mon 03/01/22	Thu 31/03/22
19	EIC Run2 design	Wed 01/12/21	Thu 31/03/22
20	M4 EIC Run2 ready for submission	Thu 31/03/22	Thu 31/03/22
21	EIC Run2 fabrication	Fri 01/04/22	Thu 30/06/22
22	EIC Run2 test	Fri 01/07/22	Fri 30/09/22
23	EIC Run 2 irradiation tests	Fri 01/07/22	Fri 30/09/22
24	EIC Final Run design	Mon 01/08/22	Fri 30/12/22
25	M7 - EIC Final Run ready for submissic	Sat 31/12/22	Sat 31/12/22
26	EIC Final Run fabrication	Sun 01/01/23	Fri 31/03/23
27	EIC Final Run test	Sat 01/04/23	Wed 31/05/23
28	EIC Final Run final characterization	Thu 01/06/23	Mon 31/07/23
29	EIC Final Run irradiation tests	Sat 01/04/23	Mon 31/07/23
30	M8 - RH qualification of EIC and PIC completed	Wed 31/05/23	Wed 31/05/23
31	EIC-PIC 1st Demo Integration Design	Fri 01/10/21	Thu 30/06/22
32	EIC-PIC 1st Demo Integration	Fri 01/07/22	Fri 30/09/22
33	M6 - EIC-PIC 1st DEMO integrated	Fri 30/09/22	Fri 30/09/22
34	EIC-PIC 1st Demo Integration Test	Sat 01/10/22	Tue 31/01/23
35	EIC-PIC 1st Demo Irradiation Test	Sat 01/10/22	Tue 31/01/23
36	EIC-PIC Final Demo Integration Design	Sun 01/01/23	Tue 30/05/23
37	EIC-PIC Final Demo Integration	Thu 01/06/23	Wed 30/08/23
38	M9 - EIC-PIC Final Demo integrated	Thu 31/08/23	Thu 31/08/23
39	EIC-PIC Final Demo Integration Test	Fri 01/09/23	Sun 31/12/23
40	EIC-PIC Final Demo Irradiation tests	Thu 31/08/23	Fri 29/12/23
41	M10 - EIC-PIC Final Demo qualified	Sun 31/12/23	Sun 31/12/23