FALAPHEL

(**Fa**st **L**inks and R**a**dHard Front End with Integrated **Ph**otonics and **El**ectronics for Physics)

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CdS 16/6/2020

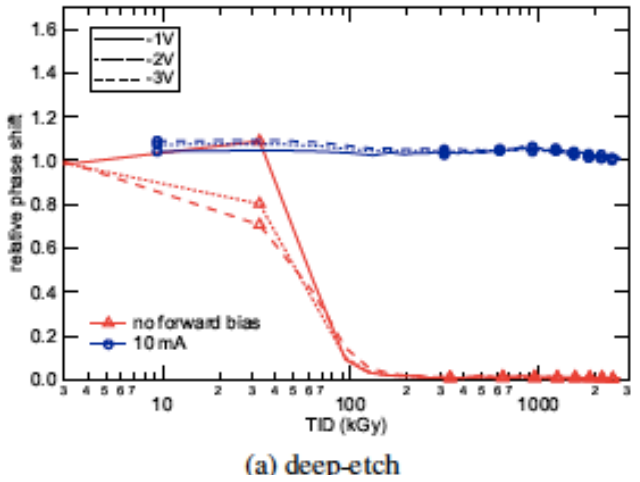
Abstract

- This project has the goal of improving the state of the art of **high speed data links** for future high rate pixel detector applications, and of studying the integration of these data links and of analog/digital front-end blocks in a prototype readout circuit.

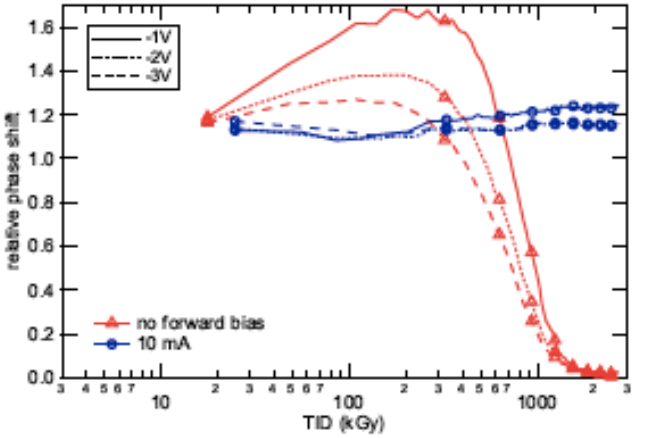
- This project will investigate innovative circuit and system solutions for the **integration of SiPh optical devices and subsystems** and **high-speed electronics for high rate data transmission**, designed to be radiation hard for HEP applications.

State of the art

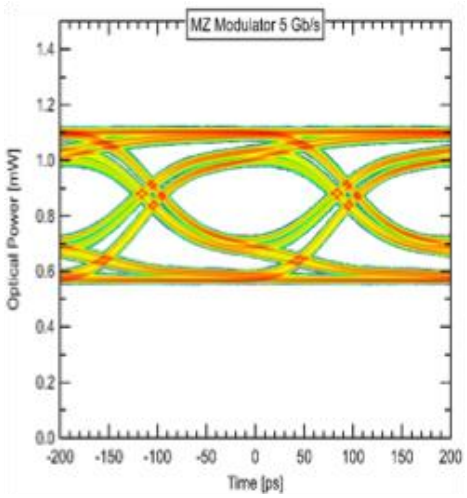
- LpGBT and Versatile Link +
  - Based on 65 nm technology and VCSEL
  - Total dose 200 MRad
  - Total fluence 10^{15} n/cm^2
    - cannot be used at HL-LHC below ~20 cm radius
      - implies RD53 chips needs e-links to LpGBT (~1 meter away)
- Silicon Photonics demonstrated to be sufficient rad-hard (>10^{16} n/cm^2 and tested up to 300 Mrad)
- PHOS4BRAIN (CSN5) project showed 65 nm driver to be rad-hard up to 800 MRad and reach ~5 Gb/s, limited by packaging (Aluminum wire bonds)

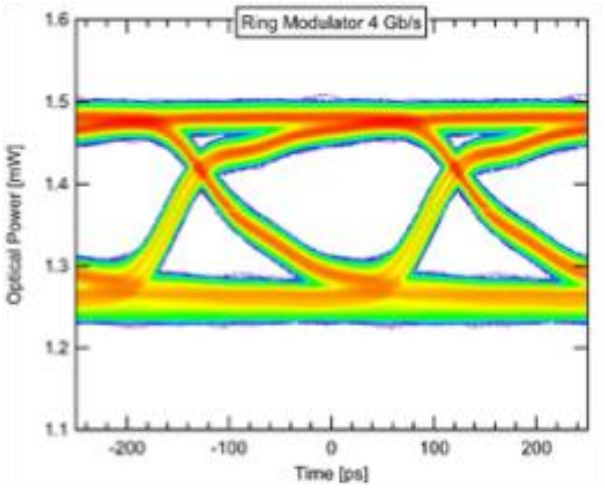


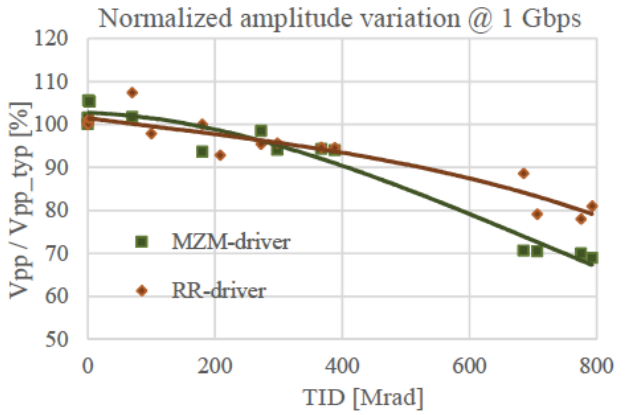
(a) deep-etch



(b) shallow-etch

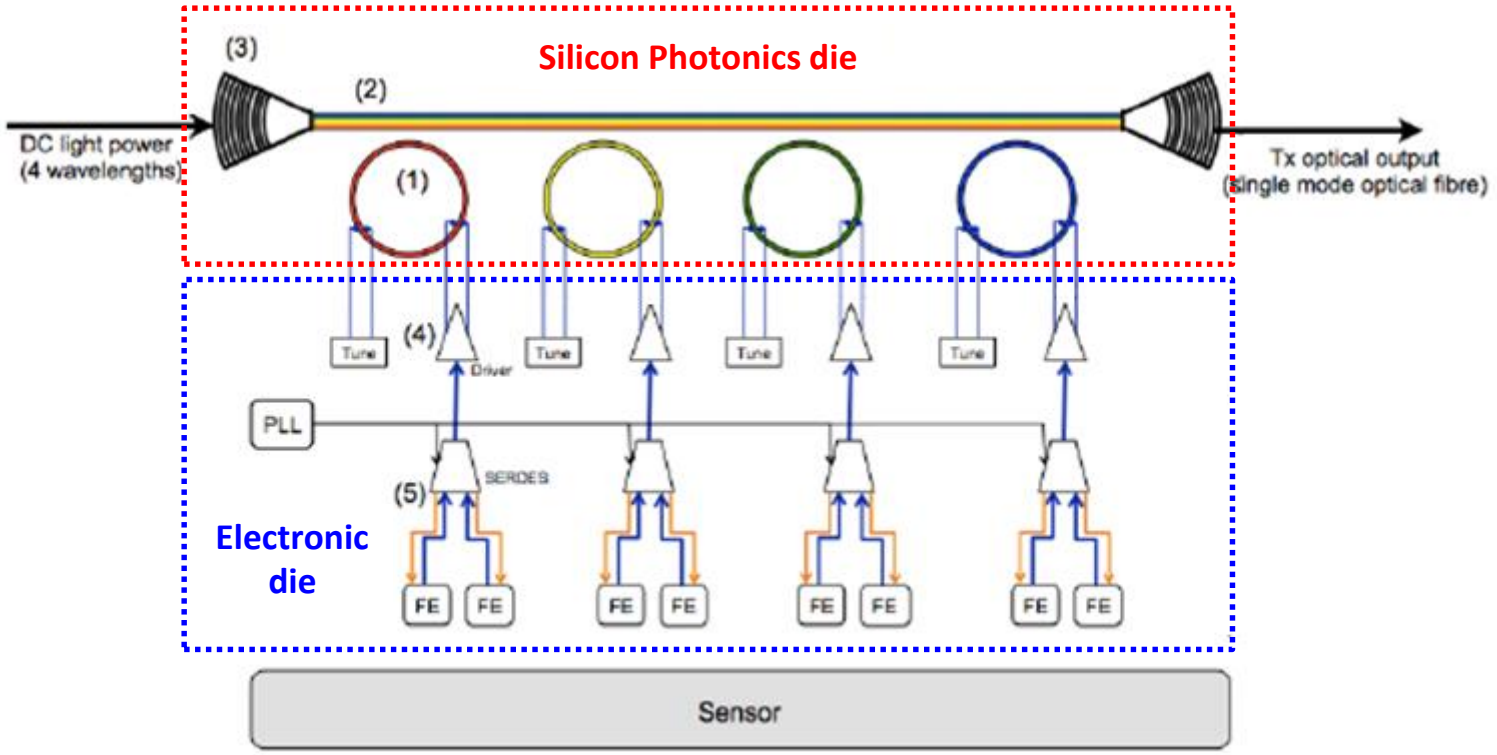






Goal

- Hybrid (3D or 2.5D) **integration** of Silicon Photonics modulators with high speed radiation hard (≥1 GRad) electronics in 28 nm
  - Aggregated 100 Gb/s links using wavelength division multiplexing (4 wavelength on a single optical fibre) and Integrated Front-End electronics
- **Design and fabrication of a demonstrator**



Objectives and research methodologies

- This project will investigate
  - Innovative circuit and system solutions for system-in-package integration of **SiPh optical devices** and subsystems (high-speed Mach-Zehnder modulators and ring resonator modulators)

PIC

  - **High-speed electronics** for high rate data transmission (SerDes, Drivers, PLL-based frequency synthesis and data/clock recovery and Front-End) designed to be radiation hard for HEP applications.
  - Moreover, the project will develop **front-end blocks** (preamplifier, discriminator for A/D conversion, buffering and readout logic) in view of the integration of a matrix of pixel cells in a readout ASIC where data are transmitted off–chip by the high-speed data links.

EIC

  - Finally, we will study the **integration** of these data links and of analog/digital front-end blocks in a prototype readout circuit

PIC + EIC

	State of the art – VCSEL+	This project (FALAPHEL)
Data rate	10 Gb/s	≥100 Gb/s
Radiation TID	200 Mrad (2 MGy)	≥1 Grad (10 MGy)
Total Fluence	10^{15}n/cm^2	>5 x 10^{16}n/cm^2

Challanges: EIC

- **The EIC will be developed in 28nm TSMC CMOS technology**, which is at the frontier of technology in High Energy Physics where the state-of-the-art is represented by the 65nm technology node

- **Expected benefits of 28 nm wrt 65 nm**
  - Allows to reach higher modulation speed at same power consumption
  - Higher radiation tolerance

- The collaboration will develop:
  - multi-Gbps SerDes
  - PLL-based frequency synthesizer and clock/data recovery (CDR) units
  - MZM driver, generating driving signals of ~2V/3V while being supplied at about ~1V
  - RM driver, generating signals of ~1V
  - Bandgap/DAC circuits,
  - Front-End analog and digital circuits (pixel matrix of 64 x 64 or 64 x 128 elements with a 50 x 25 μm^2 area, compatible with the pitch of currently available planar and 3D silicon detectors).

Challanges: PIC

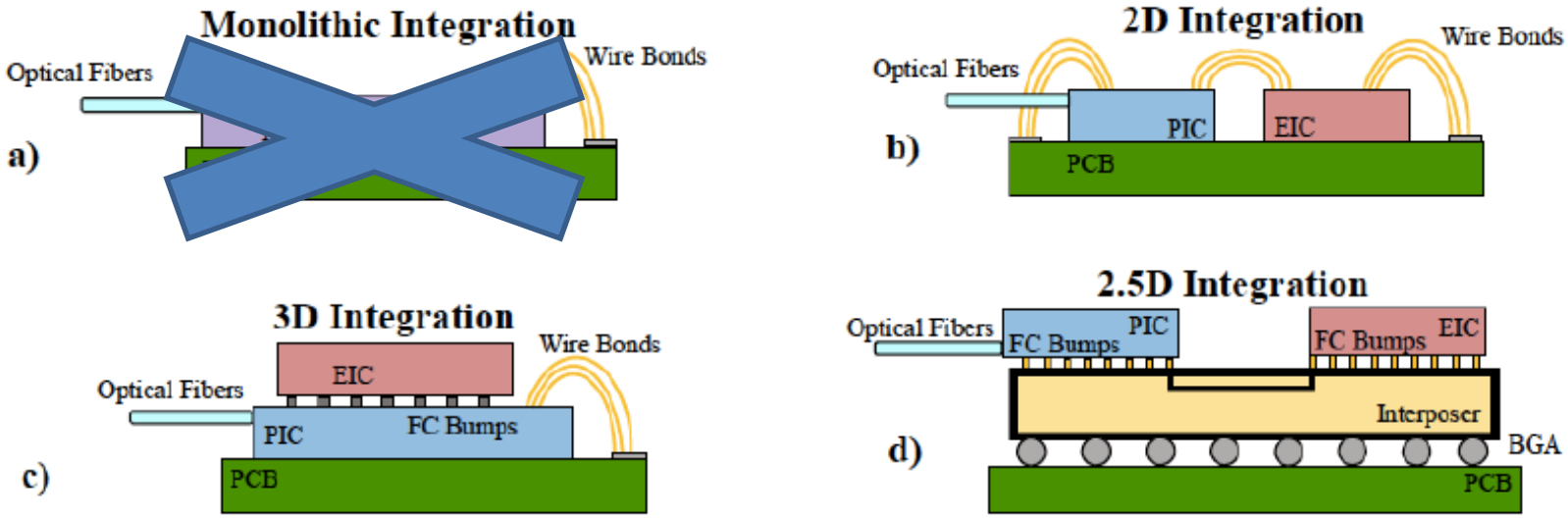
- The project will use innovative circuits and system solutions for **system-in-package integration of SiPh components**.

- Two kinds of SiPh modulators will be studied: Ring Modulators (RM) and Mach-Zehnder Modulators (MZM).

- **Ring Modulators vs Mach-Zehnder Modulators**
  - RM have smaller driving voltage than MZM
  - can be tuned for different wavelengths allowing wavelength division modulation (WDM)
  - More sensitive to temperature variations → need tune circuits

Challanges: integration

- Hybrid assembly of two chips
  - parasitic 3D (flip chip) < 2.5D (interposer) < 2D (wire bonds)
    - Need careful thermal management
      - Interest to use DIAM expertise on producing metallic additive manufacturing structures for heat removal



Organizzazione

- **Sigla**: FALAPHEL
- **Gruppo: 5** (elettronica)
- **Durata:** 3 anni (Call APERTA)
- **Sezioni convolte**:
  - INFN Pisa (Responsabile Nazionale: Fabrizio Palla)
  - INFN Pavia (Responsabile Locale: Luigi Gaioni)
  - INFN Padova (Responsabile Locale: Serena Mattiazzo)
- **Unità esterne**
  - Scuola Superiore S. Anna (SSSA) – Pisa
  - Dipartimento di Ingegneria dell'Informazione (DII) – Università di Pisa (UNIPI)
  - Dipartimento di Fisica, Università di Milano (UNIMI)

Project implementation

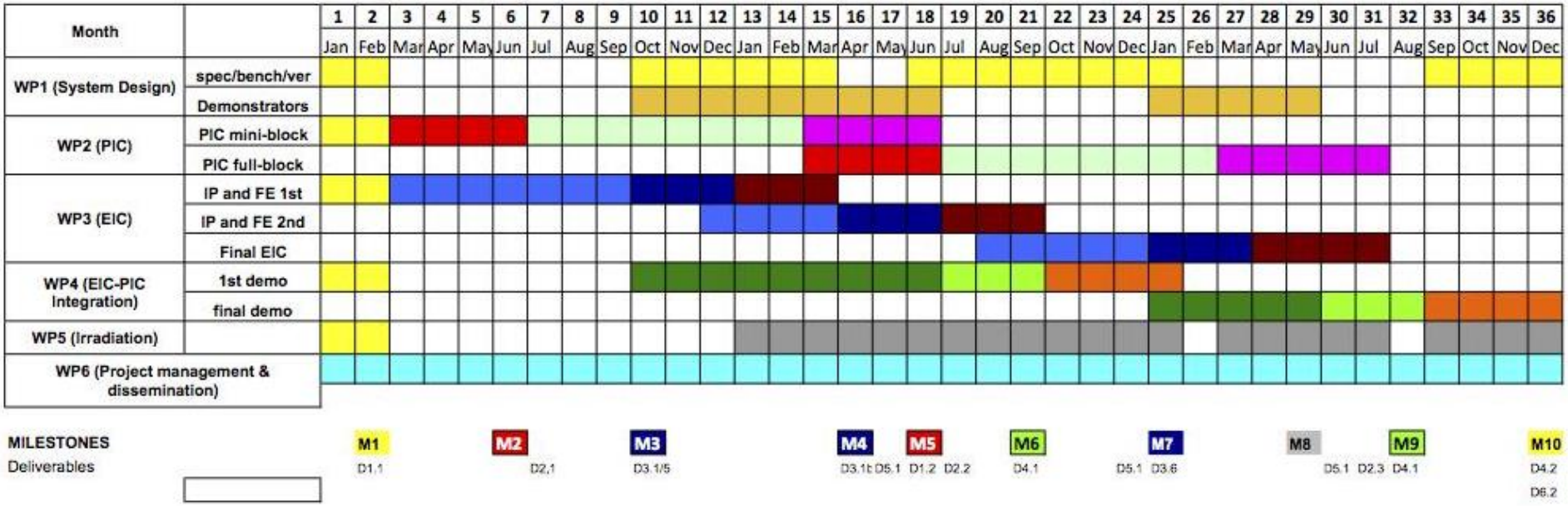
Work Package		Leader	Unit	Activity
WP1	System Design	Luigi Gaioni	INFN Pavia	Demonstrator design, system specifications and key performance indicators
WP2	Silicon Photonics	Stefano Faralli	Scuola Superiore S. Anna of Pisa	PIC blocks, Ring-Resonator Modulator, MachZehnder Modulator, WDM and SDM
WP3	Electronics	Gianluca Traversi (focus FE) and Guido Magazzu (focus IP cores)	INFN Pavia INFN Pisa	Serdes, Driver, PLL/CDR, DAC, Bandgap, Front-End
WP4	EIC-PIC Integration	Sergio Saponara	University of Pisa	Packaging and integration, thermal studies, prototyping and fabrication
WP5	Radiation hardness	Serena Mattiazzo	**INFN Padova**	Tests with X-rays, Heavy Ions, protons, neutrons
WP6	Project management and dissemination	Fabrizio Palla	INFN Pisa	Resource management, planning and coordination. Dissemination and exploitation of the results

Proposed activity for Padova section

- **WP3: Electronics**
  - The group will participate in the PLL design effort, specifically in development of the clock recovery part of the circuit.
- **WP5: Radiation hardness:**
  - The group has a long experience in radiation hard electronics and detectors, especially silicon pixel sensors, both for high energy physics and for space applications. The group has recently participated in the CHIPIX65 and RD53 collaborations (65 nm TSMC process), as well as in the INFN Scaltech28 project (28 nm TSMC process).
  - The group will coordinate the radiation hardness studies on the electronic and photonic chip, including the final large area demonstrator. The equipment at Padova (X-ray tube) will be used for the Total Ionizing Dose (TID) studies. We will explore the possibility to use the SIRAD facility at INFN LNL Laboratories for heavy ions irradiations.

- WP5: EIC-PIC integration (no formal commitment in the proposal)
  - The group will also investigate a possible involvement of the additive manufacturing laboratory (DIAM) of INFN Padova, for prototyping 3D metallic structures for heat removal for the demonstrator.

GANT chart



Legenda

- Specifications/benchmark/verification
- PIC design & layout
- PIC fabrication
- EIC design & layout
- EIC fabrication
- Integration test
- Integration design
- EIC-PIC Integration
- EIC test
- PIC test
- Irradiation

Milestones

M1 (Definitions of the specs and KPI) (T0+2)
M2 (Silicon Photonics PIC design for the submission of the mini-block chip fabrication) (T0+6)
M3 (1st submission of the High Speed rad-hard block design) (T0+10)
M4 (2nd submission of the High Speed rad-hard block design) (T0+16)
M5 (Final Silicon Photonics PIC design for the submission of the full block chip fabrication) (T0+18)
M6 (First integration EIC+PIC) (T0+21)
M7 (Final, large area EIC submission) (T0+25)
M8 (Qualification of rad-hardness of PIC and EIC) (T0+29)
M9 (Final demonstrator integration) (T0+32)
M10 (Final demonstrator qualification) (T0+36)

Richieste Finanziarie

ITEM	WP	Year 1			Year 2			Year 3			TOTAL
		PD	PV	PI	PD	PV	PI	PD	PV	PI	
Travels		2	**2**	**2**	8	**5**	**5**	7	**5**	**5**	**41**
Irradiation and testing	5	0	0	0	6	3	3	6	3	3	24
Work between designers	6	1	1	1	1	1	1	0	1	1	8
General meetings / conferences	6	1	1	1	1	1	1	1	1	1	9
Consumables		5	**32**	**89**	15	**32**	**119**	15	**65**	**25**	**397**
EIC submission	3	0	17	34	0	17	34	0	50	0	152
PIC submission	2	0	0	25	0	0	50	0	0	0	75
Test boards EIC	3	0	5	10	0	5	10	0	5	0	35
Test boards PIC	2	0	0	0	0	0	5	0	0	5	10
X-ray tubes	5	0	0	0	5	0	0	5	0	0	10
Others (cables, fibers, glues, fluids, powder, renting equipment)	1,2,3, 4,5	5	10	20	5	10	20	5	10	20	105
Access to external irradiation facilities	5	0	0	0	5	0	0	5	0	0	10
External services		0	**0**	**10**	0	**0**	**15**	0	**0**	**25**	**50**
Demonstrator design and assembly	4	0	0	10	0	0	15	0	0	25	50
Licenses		0	**0**	**8**	0	**0**	**1**	0	**0**	**1**	**10**
PIC design	2	0	0	8	0	0	1	0	0	1	10
Equipment		0	**20**	**35**	0	**0**	**0**	0	**0**	**0**	**55**
FPGA	3	0	5	10	0	0	0	0	0	0	15
Power supply	3	0	5	0	0	0	0	0	0	0	5
Laser Source (DFB) x2	2	0	0	10	0	0	0	0	0	0	10
Workstations / HD / Screen	2	0	0	5	0	0	0	0	0	0	5
Workstations / HD / Screen	3	0	10	10	0	0	0	0	0	0	20
TOTAL w/o AdR		7	**54**	**144**	23	**37**	**140**	22	**70**	**56**	**553**
Assegni di Ricerca (AdR)		0	**60**	**85**	25	**60**	**72,5**	25	**12,5**	**12,5**	**352,5**
TOTAL		7	**114**	**229**	48	**97**	**213**	47	**83**	**69**	**905,5**

Anagrafica

Cognome	Nome	Ruolo	% in FALAPHEL	WP
Bagatin	Marta	Ricercatore	0.15	WP5
Candelori	Andrea		0.20	WP5
Gerardin	Simone	Prof. Associato	0.15	WP5
Mattiazzo	Serena	Ricercatore	0.20	WP5
Paccagnella	Alessandro	Prof. Ordinario	0.15	WP5
Teng	Ma	Dottorando	0.50	WP5
Vogrig	Daniele	Prof. Associato	0.20	WP3
			TOT 1.55	
AdR			1	

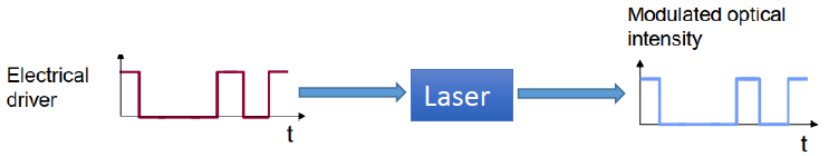
Richieste di Servizi alla Sezione (2021)

- Facilities: X-ray irradiation facility.
- One technician from the electronics lab for the facility maintenance (1 s.u.) and one technician from the mechanical workshop (1 s.u.) for mechanical support systems for irradiations.

Photonic Integrated Circuit (PIC)

- The project will use innovative circuits and system solutions for system-in-package integration of SiPh components.
- Two kinds of SiPh modulators will be studied: Ring Modulators (RM) and Mach-Zehnder Modulators (MZM).

Signal modulation in Laser based Transmitter:



Signal modulation in SiPh based Transmitter: