HiDRA2 Calibration mode

Eugenio and Lorenzo, XX YYY 2020

Outline

PURPOSE Test calibration mode on the HiDRA board 6

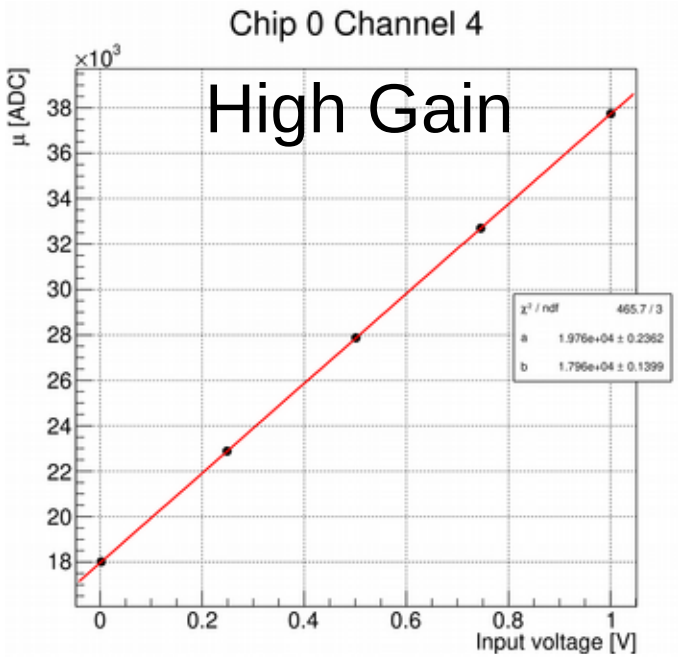
METHOD Data acquired in three different configurations:

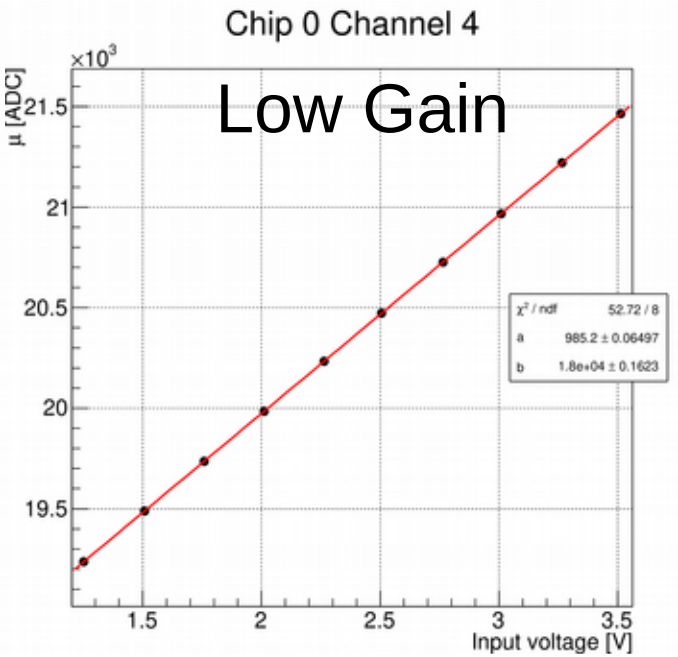
- For High Gain - V_{cal} in [0.00, 1.00] V
- For Low Gain - V_{cal} in [1.25, 3.50] V
- For Forced Low Gain (G2SEL on) - V_{cal} in [1.25, 3.50] V

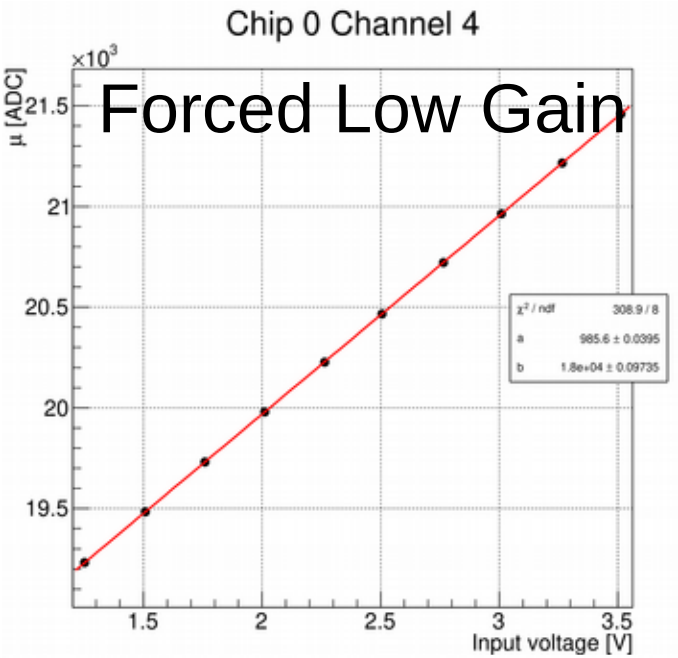
SETUP V_{cal} was supplied by a TTi voltage generator, but, due to its limited accuracy, it was measured using a Keithley multimeter.

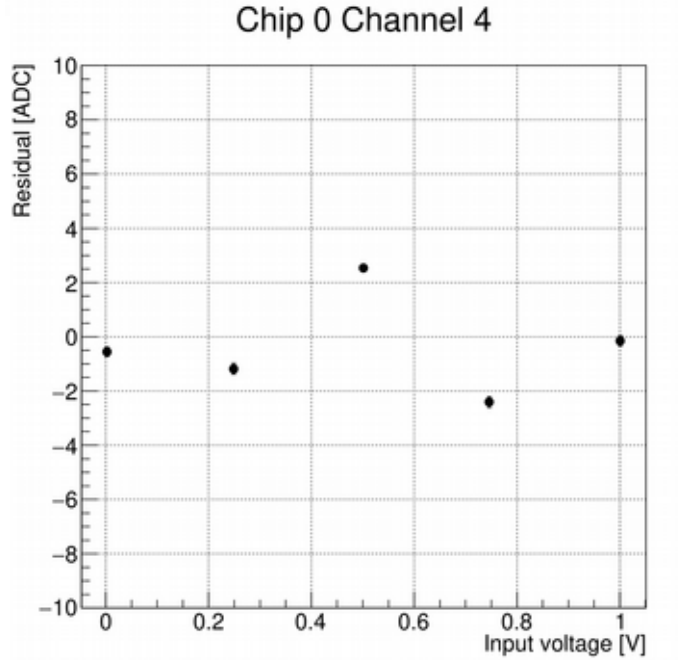
CAVEAT Among the four chips mounted on the board, the first two work correctly, whereas strange a behavior was found on the last two (both in acquisition and calibration mode): for this reason we present here the results relative to the channels of the **first chip** only.

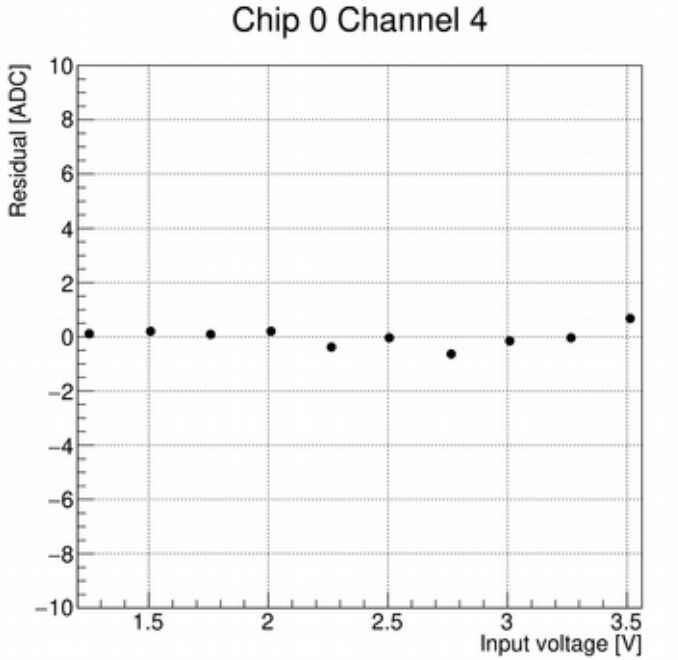
HiDRA Gain - Chip 0 Channel 4

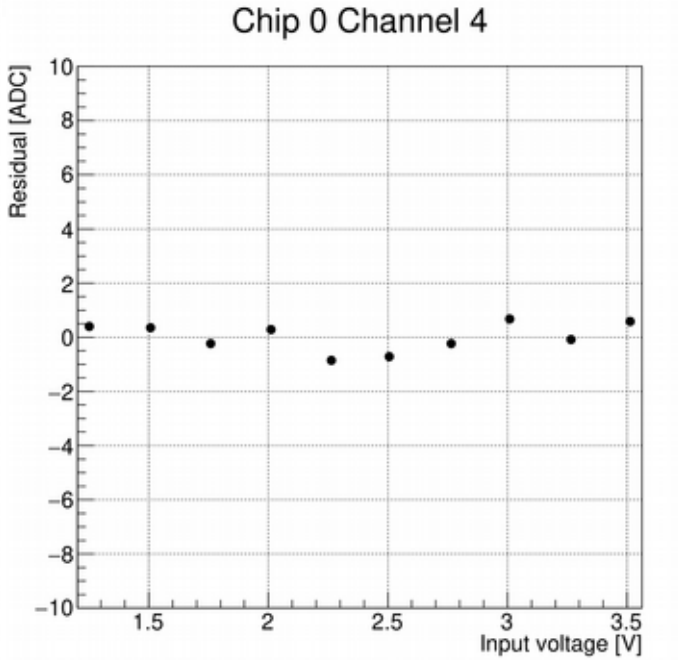






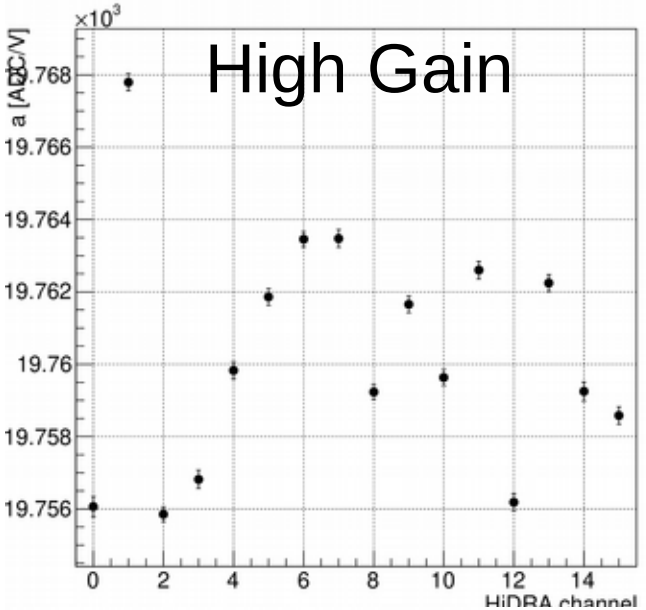


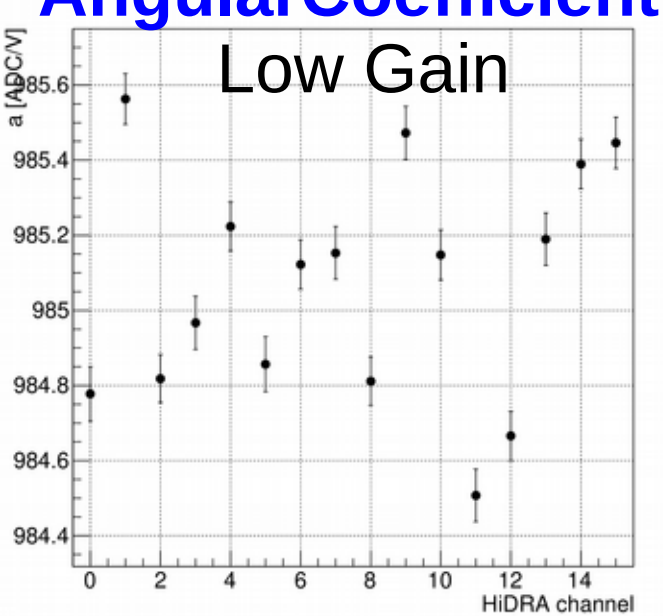


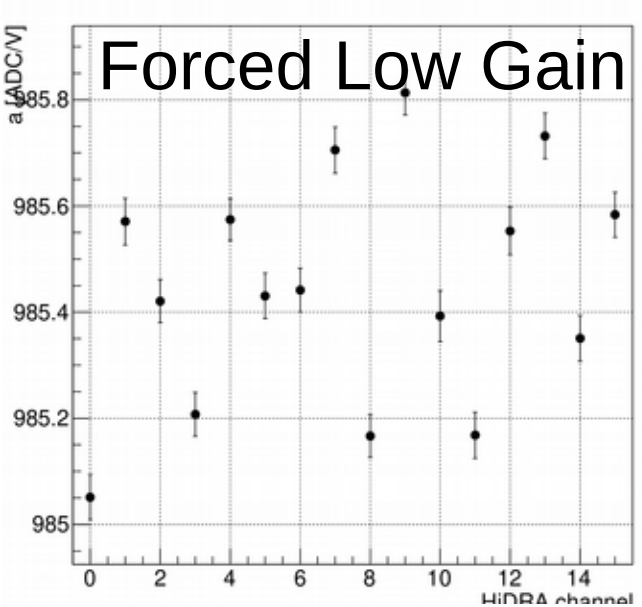


Linear Coefficient - Chip 0

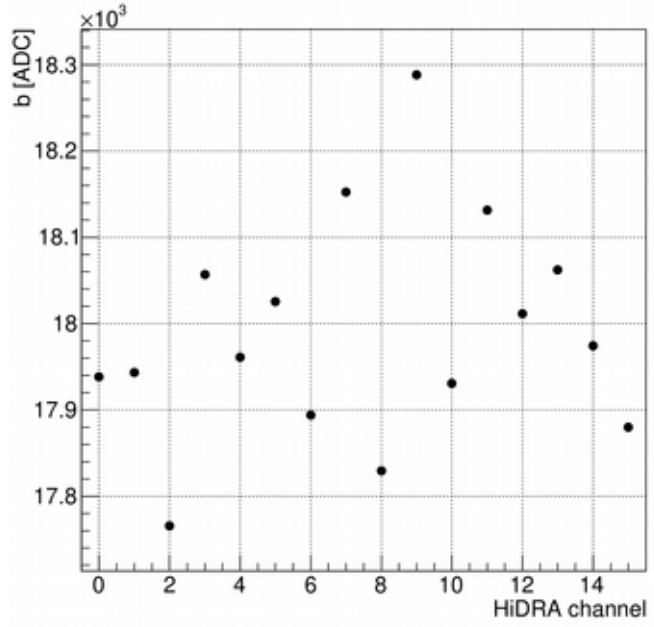
AngularCoefficient

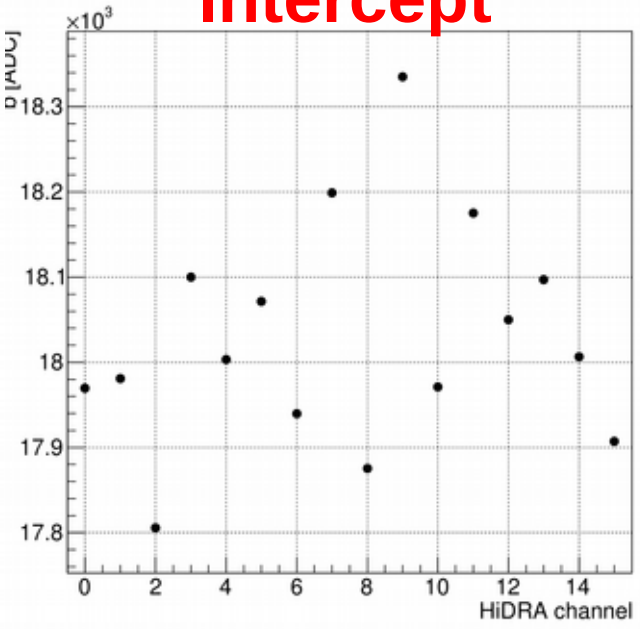


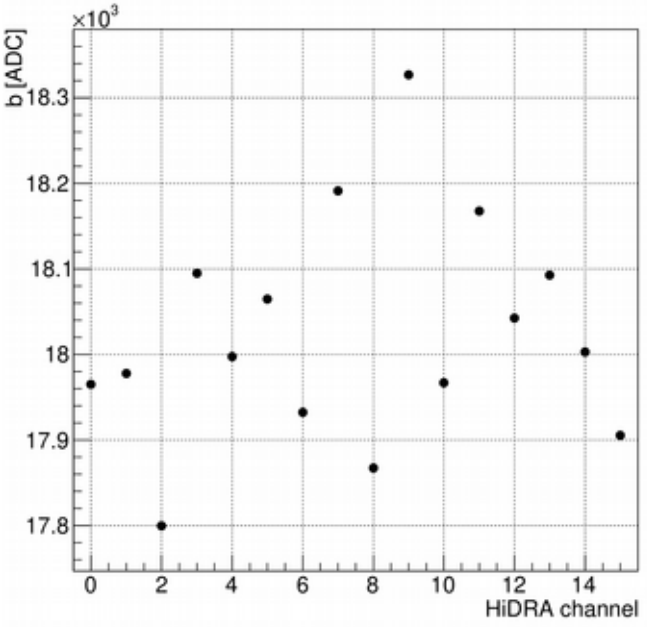




Intercept





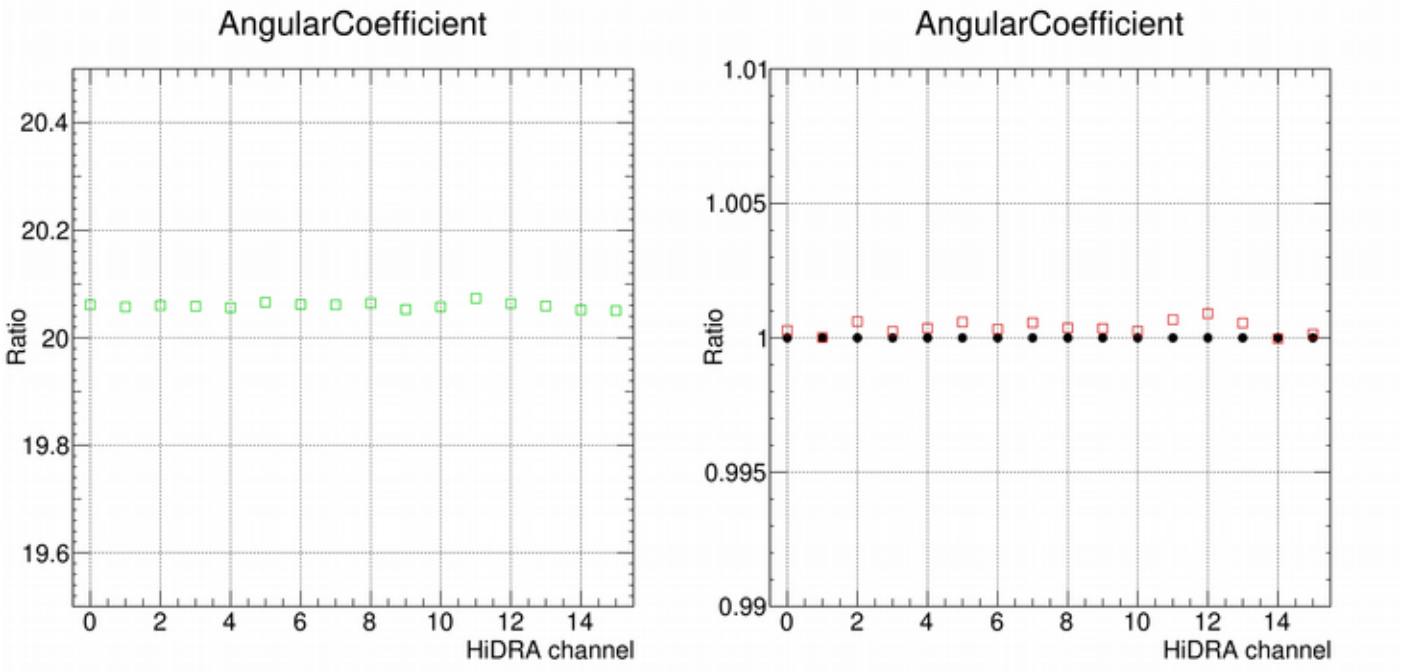


Angular Coefficient Ratio - Chip 0

High Gain

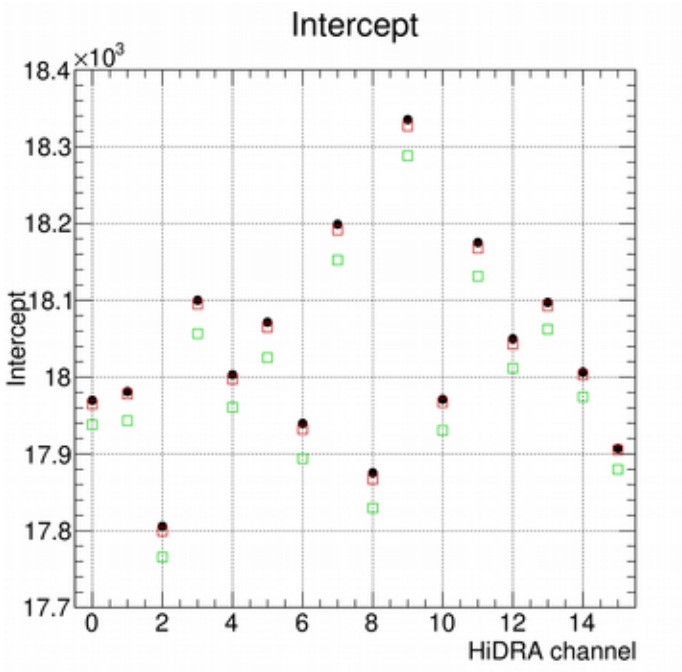
Low Gain

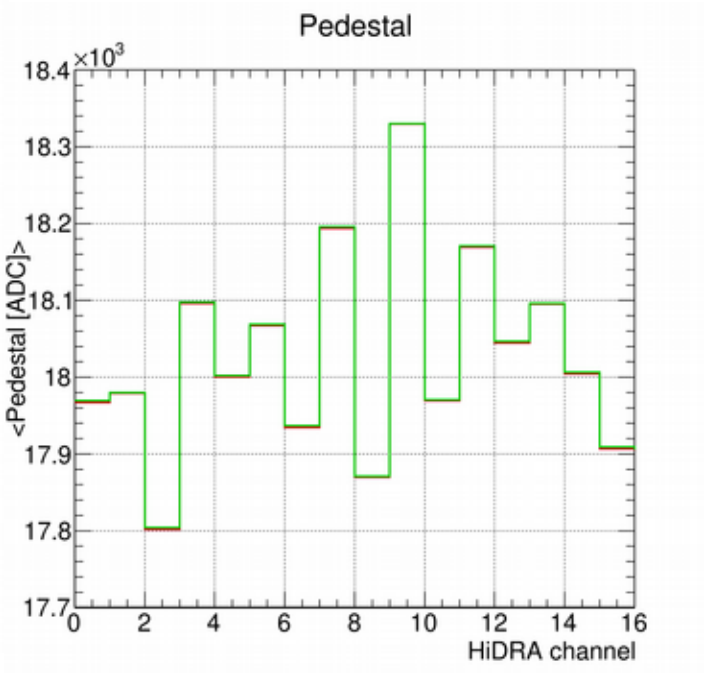
Forced Low Gain



The results on the angular coefficient are compatible with the ones presented by Jorge on 11/04/2019

Intercept - Chip 0





High Gain

Low Gain

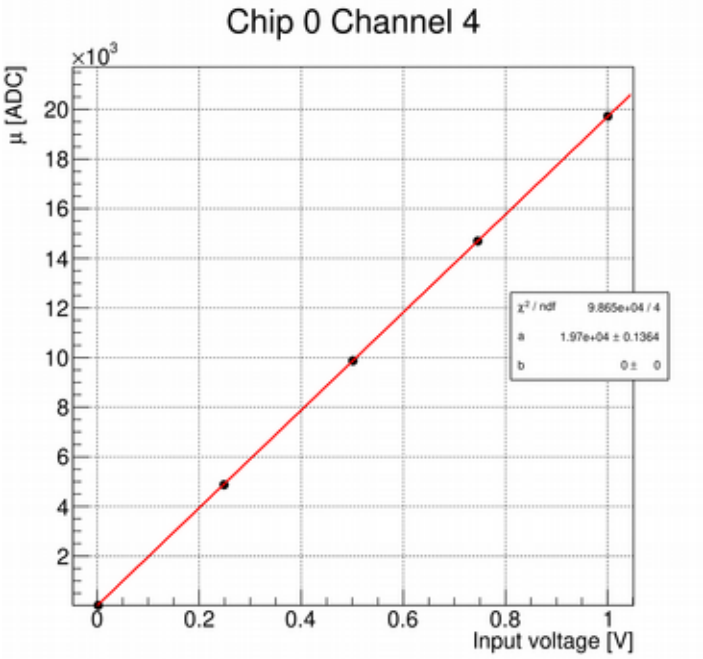
Forced Low Gain

The results on the intercept shows an offset of about 50 ADC between High Gain and Low Gain intercept values (2 mV).

If we check the pedestals distribution we found that the mean has the same value in High Gain and Low Gain (Gain Forced).

This pedestal mean is consistent with the intercept extrapolated from the calibration curve in Low Gain (not High Gain!).

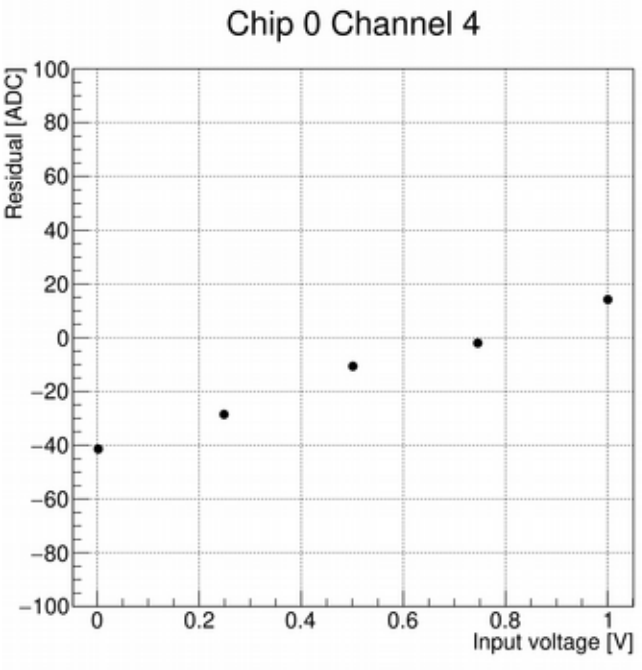
Force Intercept to Zero - Chip 0

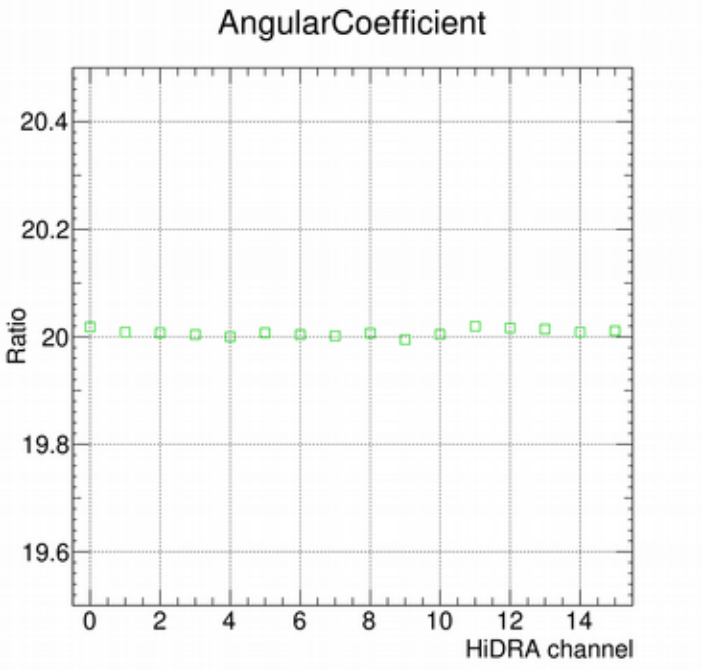


If we subtract pedestal value and we force the calibration curve to have zero intercept, the fit is vary bad and the residual very high...

However, if we check again the gain ratio we found that, under this condition, this moves from 20.05 to 20, as expected...

Is this offset a feature of the chip?





High Gain

Low Gain

Forced Low Gain

How much electron is the noise?

$\sigma \sim 15$ ADC

$C_{Cal} \sim 10$ pF

$e \sim 1.6 * 10^{-19}$ C

$a \sim 19760$ ADC/V

$ENC = (C*\sigma)/(a*e) = 4744\ e^-$

Given the expression $ENC = 2280\ e^- + 7.5\ e^-/pF*C_{in}$, this value correspond to a input capacitance of 708 pF.

If we force C_{in}=0 pF, we expect an equivalent output noise of about $\sigma = a\ (2280 * e) / C_{cal} = 4.5$ ADC

Summary

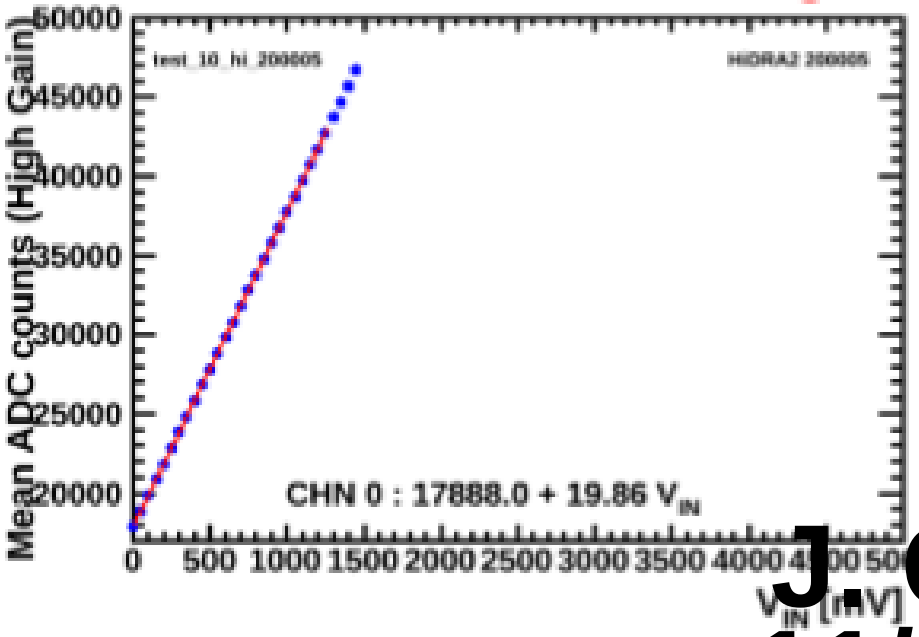
Calibration mode works well (at least on first two chips).

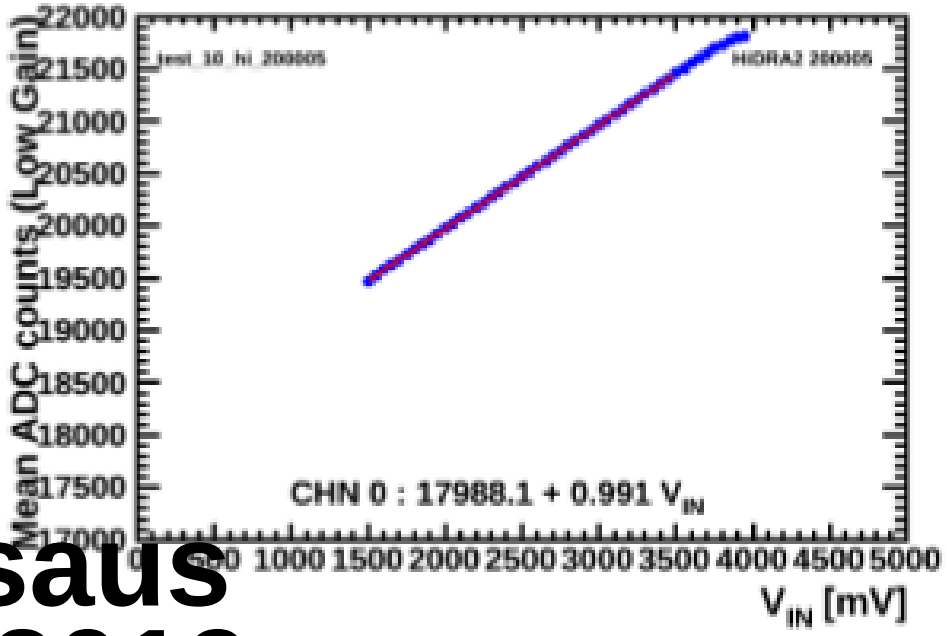
Respect to our knowledge on the previous version of the CASIS chip we found two **unexpected behaviors**:

- We did **not** observe an offset of about 100 ADC channels between the free gain curve and the forced gain curve when the chip is in Low Gain
- We observed an *offset of about 50 ADC between the High Gain and the Low Gain curves*, indicating that 0 V at the input generates a signal at the output that is 2 mV below the pedestal value in High Gain (!?)

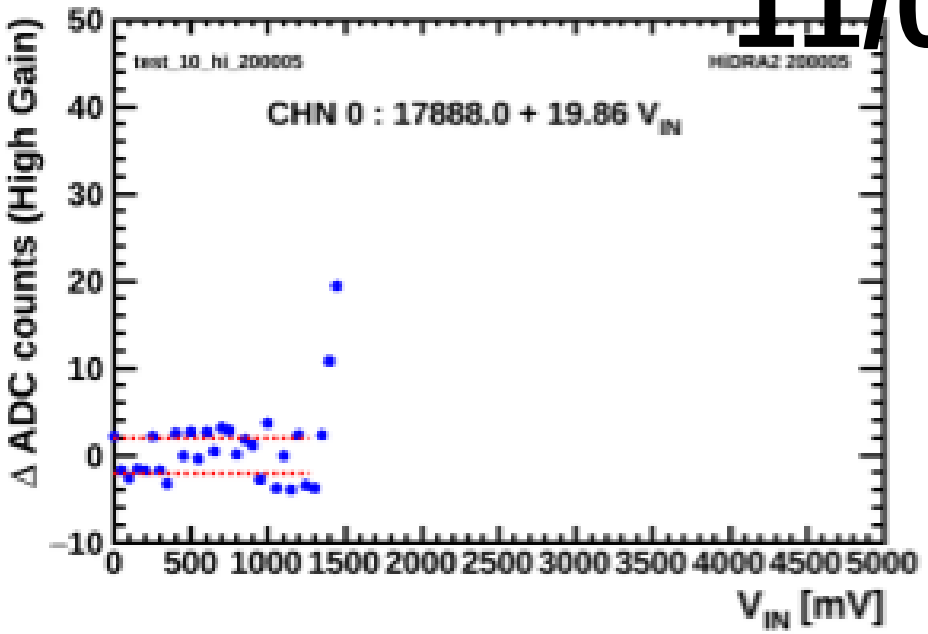
Back Up

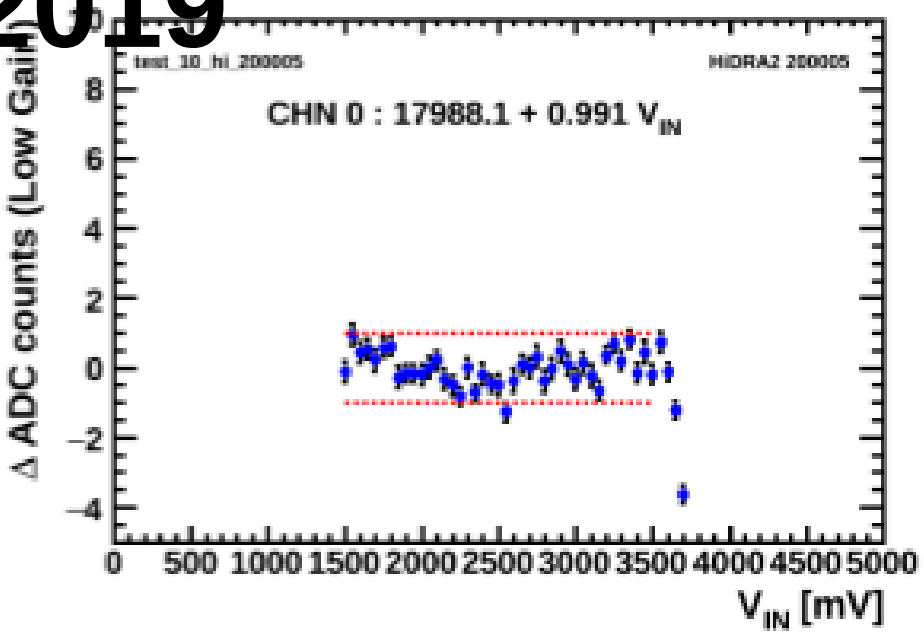
Gain Calibration: Linearity Range in High & Low Gain



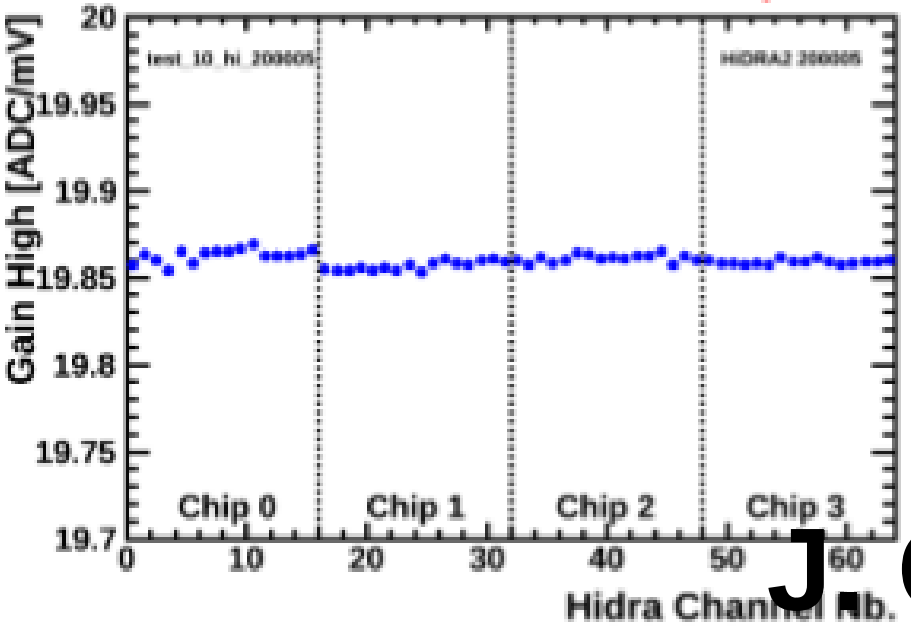


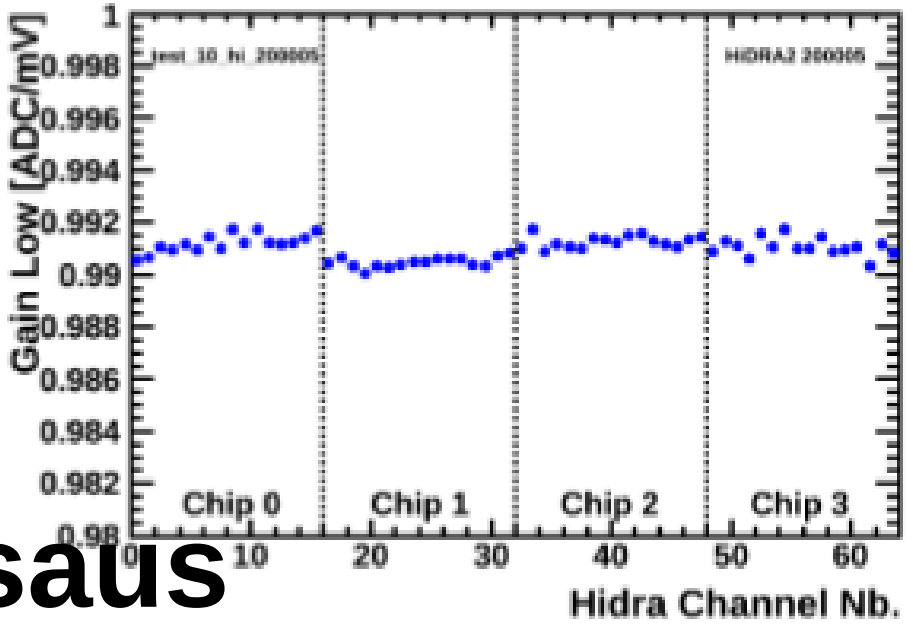
J.Casaus
11/04/2019





Gain Calibration: Channel Uniformity in High & Low Gain





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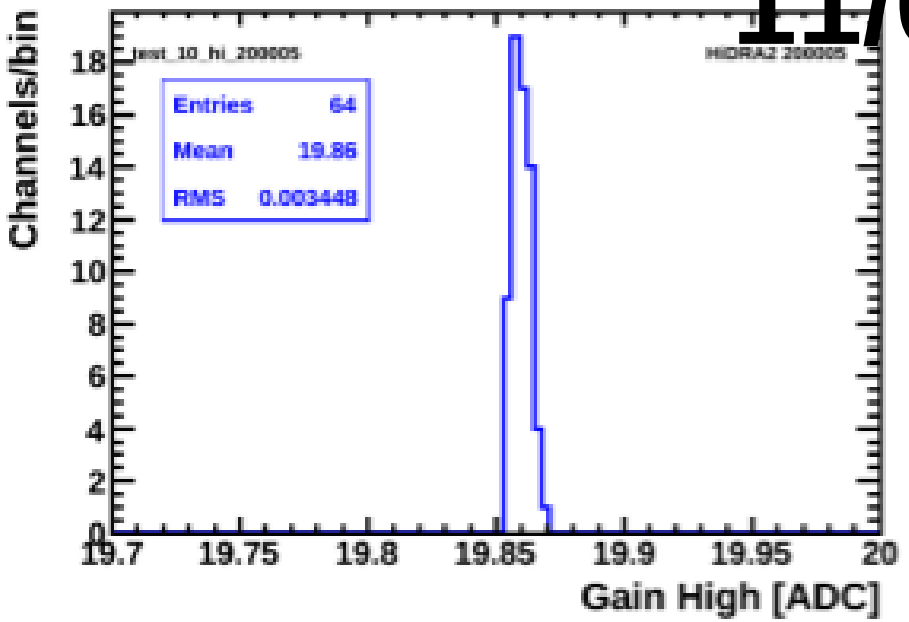
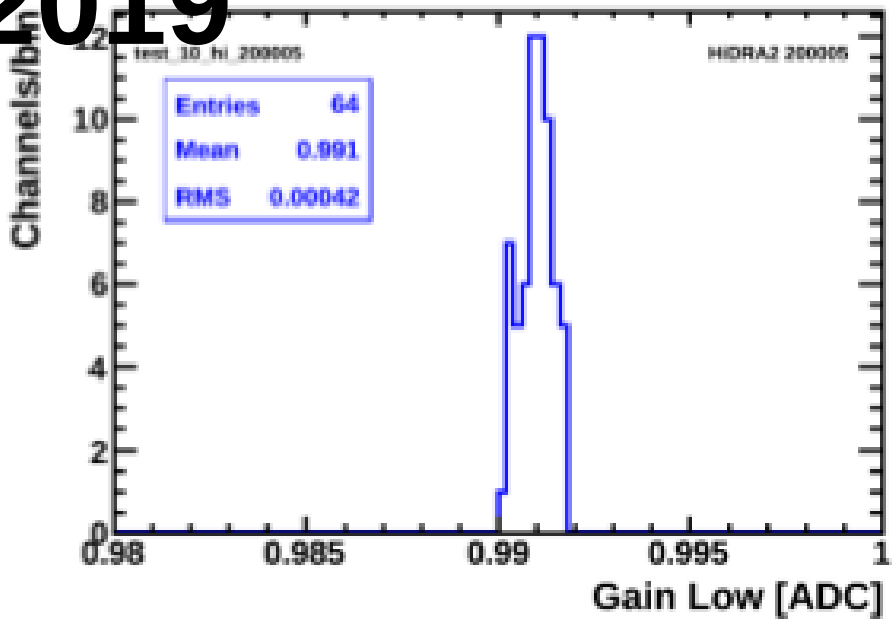
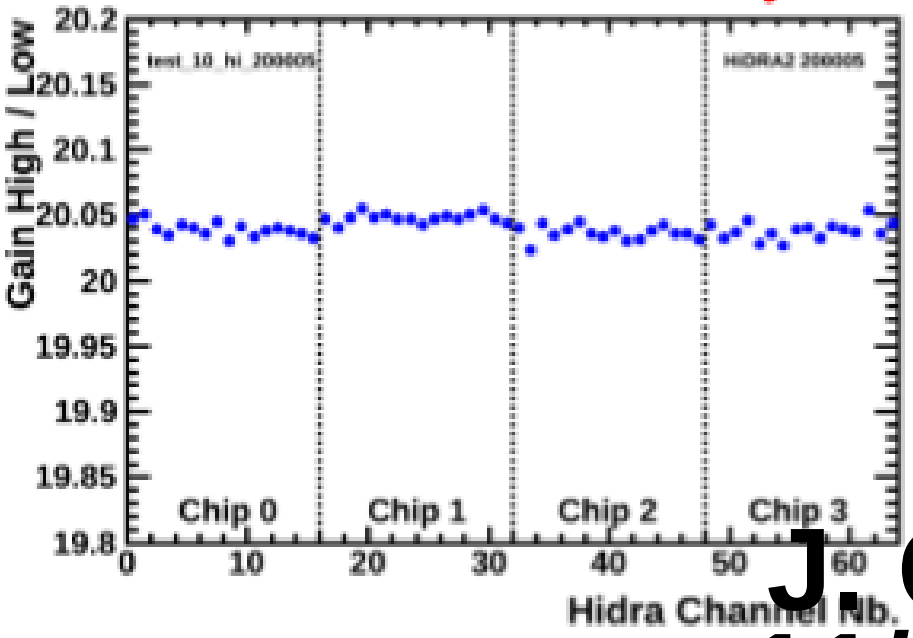
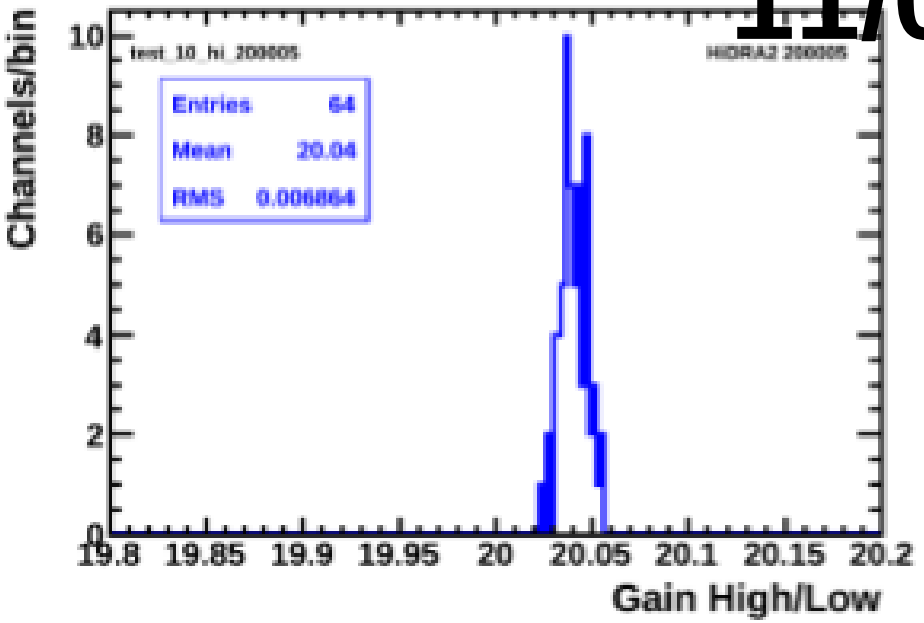
11/04/2019





Gain Calibration: Channel Uniformity in High & Low Gain





Results on HiDRA2 Board 200005

Pedestals & Noise :

- Pedestal values in the 17500 – 18200 range
- Noise in the range 10 – 14 ADC with a clear odd-even channel structure

Gain

- Average High Gain 19.86 ADC/mV
- Average Low Gain 0.991 ADC/mV
- Average High/Low 20.04
- All channels within 0.1% of the average

J. Casaus
11/04/2019